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Towards near-zero-power logic gates based on capacitive MEMS devices operating in adiabatic regime

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Abstract/Résumé

We introduce an architecture of logic gates based on capacitive MEMS devices in a differential architecture, operated in the adiabatic regime and aiming at reaching ultra-low power operation. The tunable capacitances, which are the fundamental component of our MEMS devices are realized using comb-drive actuators. Their design was a result of an extensive FEM analysis and had to satisfy criteria for sufficient logic differentiation and cascadability of individual gates. Microfabrication tests were performed on silicon wafers as optimization of the fabrication process for the realization of full logic gates on SOI wafers.

1 Introduction

Logic gates are devices that act as building blocks for digital circuits. Based on the combination of digital signals coming from their inputs, logic gates perform logical functions based on Boolean algebra that are fundamental to digital circuits. In modern practice, most gates, e.g. in microprocessors, are made from MOSFETs (metal–oxide–semiconductor field-effect transistors) [1]. In current technology, the combinatorial logic is based on abrupt charging and discharging of the capacitors for moving from one logic state to the other. The logic state is determined by the quantity of the charge stored in a capacitor. Abrupt charging and discharging of these capacitors (changing of the logic state) is realized with MOSFETs that act as switches.

In the sixties in the last century Rolf Landauer has proposed the principle describing the smallest amount of energy that is used to switch between two logic states – "0" and "1", that is, to erase one bit of information. This principle is now known as the Landauer's limit and claims that the energy requirement, at room temperature for one operation, should be of the order of magnitude of zepto (10^{-21}) joules. However, this limit is still far from being reached. The state-of-the-art MOSFET transistors dissipate ~1000 k_BT (~10^{-18} joules) even in advanced CMOS nodes during a single logic operation and remain therefore orders of magnitude above Landauer's limit [1][2]. The energy dissipation of digital circuits has been widely studied and can be explained by three different aspects:

1. Dynamic losses which occur during abrupt switching between two logic states,
2. Static losses which are due to the non-zero leakage currents when the switch is "off"
3. In order to be able to distinguish two different states their energetic difference has to be well above the thermal noise level (k_BT), which in turn increases the dynamic losses.

In our work, we aim to eliminate static *and* dynamic losses from logic circuits and therefore approach zero power dissipation during the logic operations. Overcoming such a challenge requires hardware- and system-level shifts in the paradigm used for logic circuits. Lower dynamic losses however come at a cost of lower processing speed as this approach requires operating at low frequencies (speed limit comes from the device's time constant). At lower frequencies static losses become dominant. Their elimination requires devices with zero-leakage.

Some previous works in the field have made use of nano/micro-electro-mechanical system (N/MEMS) relays to pursue this goal [3-6]. However, their limited mechanical reliability, relatively high operating voltages and low operating frequencies have already been discussed and elaborated [7][8]. Here, we propose capacitive MEMS

devices based on comb-drive actuators for storing and transmission of the logic information in a differential architecture. Such capacitive devices are contactless, which strongly limits leakage current and therefore static losses which are usually met by ohmic M/NEMS relays.

2 Contactless capacitive MEMS device – Principle of operation

The architecture of our device basically relies on a four-terminal MEMS device forming a mechanically-variable capacitor whose terminals are electrically isolated and which is moved by an actuator. The variation of the capacitor, here an interdigitated comb, could be realized with several actuation technologies like e.g. magnetic or piezoelectric. However, our choice of electrostatic MEMS actuation has been driven by their better scaling properties and ease of fabrication. The four-terminal MEMS capacitors are thereby realized with pairs of interdigitated combs - one input comb actuating the second one and varying its capacitance value. The proposed electromechanical logic gate consists of the moving mass combined with two moveable, grounded electrodes and two fixed electrodes. The voltage across the gate-input allows us to control the capacitance of the gate-output.

The capacitance between the interdigitated combs is governed by their physical position and controlled by the electrostatic forces that act between two electrically conductive combs. In our approach, by using a capacitive divider instead of a resistance divider to define the logic level like in CMOS logic (Figure 1a and 1b), the electrical connection between the power and the ground is omitted – therefore avoiding leakage currents through a direct resistive connection. Furthermore, using the AC power supply - acting as the power-clock (V_{PC}), allows for recovery of the electrical charges invested in the encoding of the logic state. Such adiabatic operation is described in references [1] and [9]. The cascade between gates and the propagation of logic states are not covered in the scope of this article, but are clearly described in reference [10].

The proposed geometry (architecture) of the device is shown in Figure 1c. This differential architecture consists of two pairs of comb-drive actuators – input and output pair. Each pair consists of a fixed (active) and a movable (passive) electrode while the movable electrodes are connected by a mechanical spring of a stiffness *k*. Active and passive electrodes are connected to the power-clock V_{PC} and to the ground, respectively. They are electrostatically coupled by *n* interdigitated fingers separated by an air gap *g*. The architecture being differential, the input and output are driven by complementary voltages V_{in} and $\bar{V}_{in}$and V_{out} and $\bar{V}_{out}$, respectively (Figure 1b and 1c), defining a so-called dual-rail logic.

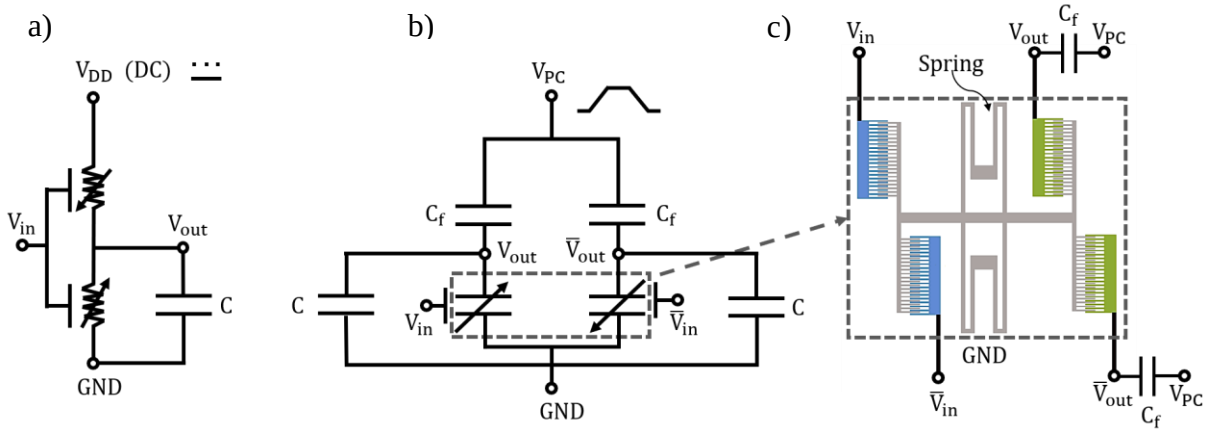

Figure 1: a) Resistor-based (CMOS) logic with V_{DD} being the DC supply voltage, V_{in} and V_{out} being the input and output voltages, respectively, and C being the input load of the next gate; b) Adiabatic contactless logic based on variable capacitors with V_{PC} being the power clock – a variable power supply capable of energy recovery and C_f being the fixed capacitance; c) Implementation of variable capacitors with comb-drive actuators in a differential configuration. V_{out} can then be read through a capacitive divider formed with the fixed capacitor C_f and the input load C.

The input voltage that is set on the fixed comb in the input pair (blue in Figure 1c) causes the movement of the "input"-movable comb and therefore the "output" movable comb as well. The consequential movement of the output comb, coding the logic state, results in a changed capacitance between the combs of the output actuator (green in Figure 1c) which can then be read through a capacitive divider formed with the fixed capacitor (C_f in Figure 1b and 1c) and the load *C* (from the interconnection and the next gate). The output voltages V_{out} and $\bar{V}_{out}$ serve as the input voltages for the control of the next device.

Our proposed system follows the adiabatic logic style [1][9]. The information encoding and reading is done in four phases governed by the power clock V_{PC} which has a trapezoidal waveform for the sake of energy efficiency and recovery of the electrical charges. Dissipation in the adiabatic logic is governed by the ramping time T of the power clock signal. Figure 2 shows the waveform of the main signals needed to drive a single logic gate as well as the corresponding position of the device during the information encoding and reading. As an example, the four phases of the transportation of the logic state "1" (high state) are shown.

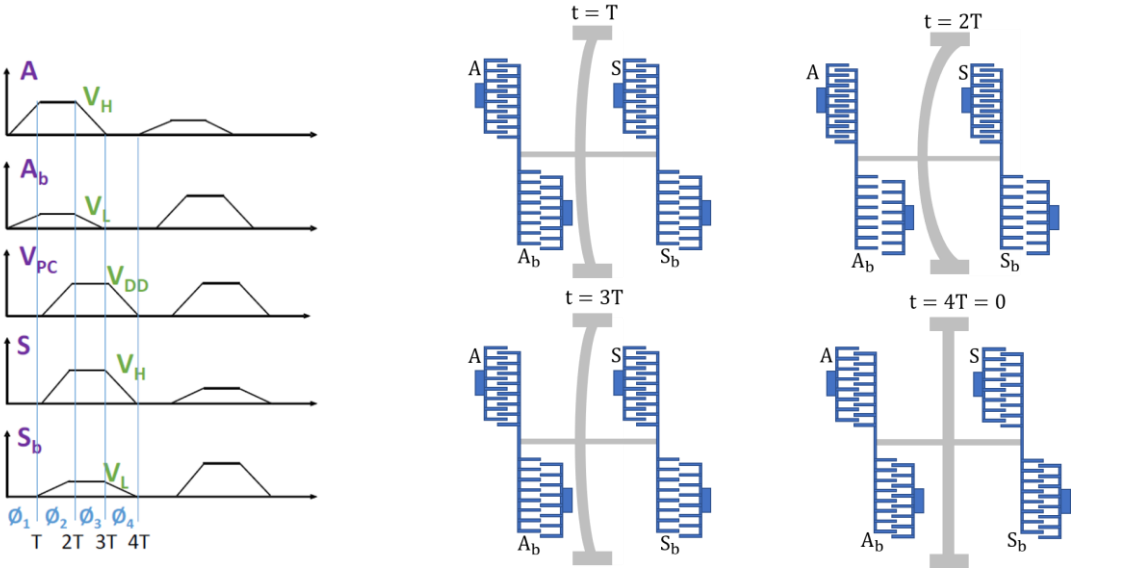

Figure 2: The applied signals and the position of the device during the information transportation (the example of logic state "1") from the input to the output stage of the logic gate. The operation is performed in four stages: ***phase 1****(set) – application of signals A and A_b and movement of the beam towards electrode experiencing greater force (here A);* ***phase 2*** *(evaluate) – application of V_{PC} signal, establishment of the output signals S and S_b;* ***phase 3*** *(hold) – lowering of the signals A and A_b to the ground, maintenance of the states through V_{PC};* ***phase 4*** *(recovery) – reduction of V_{PC} signal, return of the moveable part to the initial position.*

In **phase 1** (known as *set*) the signals A and A_b of respective amplitudes V_H and V_L are applied, corresponding to a logic signal in the high state and in the low state, respectively. Two electrostatic forces act on the beam. The beam undergoes a greater force by the electrode A because $V_H > V_L$. At the end of phase 1 (at t=T), the beam has moved to the left.

In **phase 2** (known as *evaluate*), the V_{PC} signal is applied via the capacitive bridge formed by the fixed capacitance and the equivalent capacitance of the nodes S and S_b. The beam continues to move. The output voltage S is established at a value V_H corresponding to a high logic state (t=2T).

In **phase 3** (called *maintenance* or *hold*), the input signals A and A_b are gradually lowered to ground (t=3T). The maintenance of the position is due to the output electrodes that are still polarized via V_{PC} which is maintained.

In **phase 4** (known as *recovery*) the V_{PC} signal is gradually reduced, leading the position of the beam towards the center – the "resting" position (t=4T).

3 FEM analysis of capacitive behaviour of the combs with low overlap

Our device is based on electrostatic actuation of the comb-drives and requires fine knowledge and control of the capacitance between the opposing combs. The variation of the capacitance is realized through the change of the finger overlap. Deep understanding of the comb-drive behavior and the impact of their geometry and displacement is required for the design of a logic gate that can provide sufficient logic differentiation between "0" and "1" states at the output stage (V_{out} in Figure 1c). Furthermore, the logic state should be preserved during propagation through a cascade of several gates and ultimately a complex logical circuit where multiple inputs are being driven by a single output should be feasible. System level modeling and optimization showed us that some critical phases of the device operation require controlling of the combs in an arrangement where the finger overlap is close to a zero. Such a model is neither covered by the usual analytical modeling of electrostatic comb-drives nor in the literature.

As a consequence, behavioral modeling and extensive FEM analysis (using COMSOL Multiphysics) of the device, including the comb-drive actuators, have been done in order to better understand this regime. The analysis provided the information about capacitance and generated force - necessary for the design of the comb-pairs and for enabling the operation of logic functions in cascaded gates. In particular, geometrical parameters as the length of the fingers,

their width *d* and thickness *h*, gap between consecutive fingers *g*, their overlap x_r and number *N* were investigated. The influence of these parameters on the variable, fixed and parasitic capacitances of the actuator, including fringe effects, and the induced force between the combs were analyzed in detail. As an example, Figure 3 shows the FEM modeling of an electrostatic comb and the simulation of the electric field between fingers of the corresponding combs.

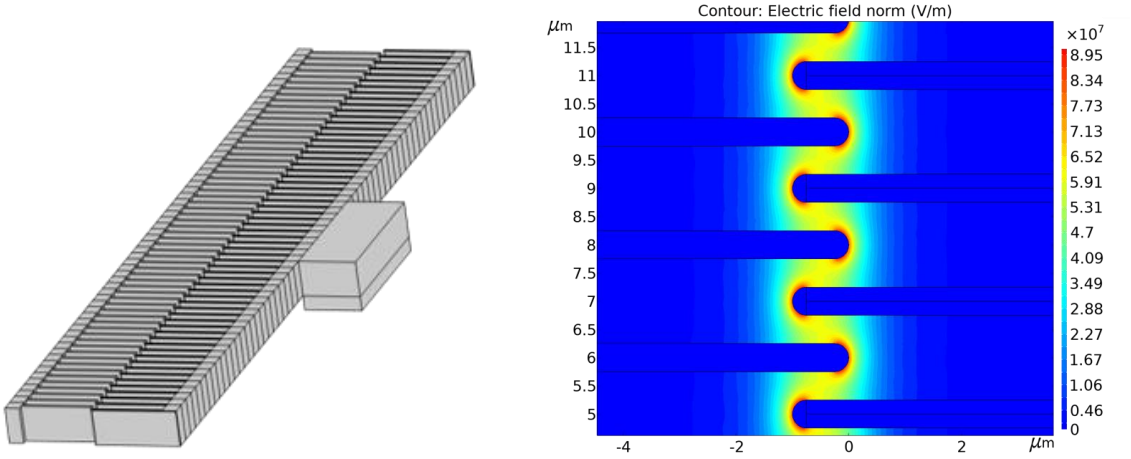

Figure 3: FEM modeling of an electrostatic comb-pair: a) 3D model, b) simulated electrical field between the combs.

4 Microfabrication process flow

The extensive FEM analysis provided sufficient data for the design of a full logic gate that could be fabricated using standard microfabrication technologies. As the devices include moveable parts, they require fabrication on silicon-on-insulator (SOI) wafers, the buried oxide layer being used as the sacrificial layer during the releasing step.

Figure 4 illustrates the main steps of the fabrication process. We use 4-inch (100 mm) (1-0-0) SOI wafers with the device layer of 5 µm and buried oxide of 2 µm thickness. Device layer has resistivity of 0.001-0.005 Ohm·cm, it is n-doped with As with concentration 10^{19} - 10^{20} cm^{-3}.

Before the beginning of the fabrication wafers are cleaned in the standard RCA procedure. This step ensures removal of all the organic and ionic contaminants from the wafer surfaces. Cleaned wafers are first coated with bottom anti reflective coating (BARC) and baked at 200°C for 60s. On top of the cooled-down BARC a positive ECI (MicroChemicals) photoresist is applied and soft-baked for 90s using EVG120 (EVG Group) automatic resist processing system. Exposure is done on Canon FPA 3000i4/i5 Stepper (Figure 4b), which allows photoresist exposure at 365 nm (i-line), followed by a development in MF-CD-26 (Microposit) developer with EVG120 system (Figure 4c). Pattern transfer into silicon is performed with Alcatel AMS4200, a high-density plasma reactor (Figure 4d). The reactor is ICP-RIE (Inductively Coupled Plasma) and is used for treatment of 4-inch wafers. The top silicon layer is etched in a DRIE procedure (Bosch process) with cycle 2.2s/2s (SF_6/CH_2F_2). Backside etching is performed bellow unfixed device parts in order to reduce the parasitic capacitance (Figure 4e). Moveable parts are finally released in the hydrofluoric acid that etches the buried oxide beneath the structures (Figure 4f).

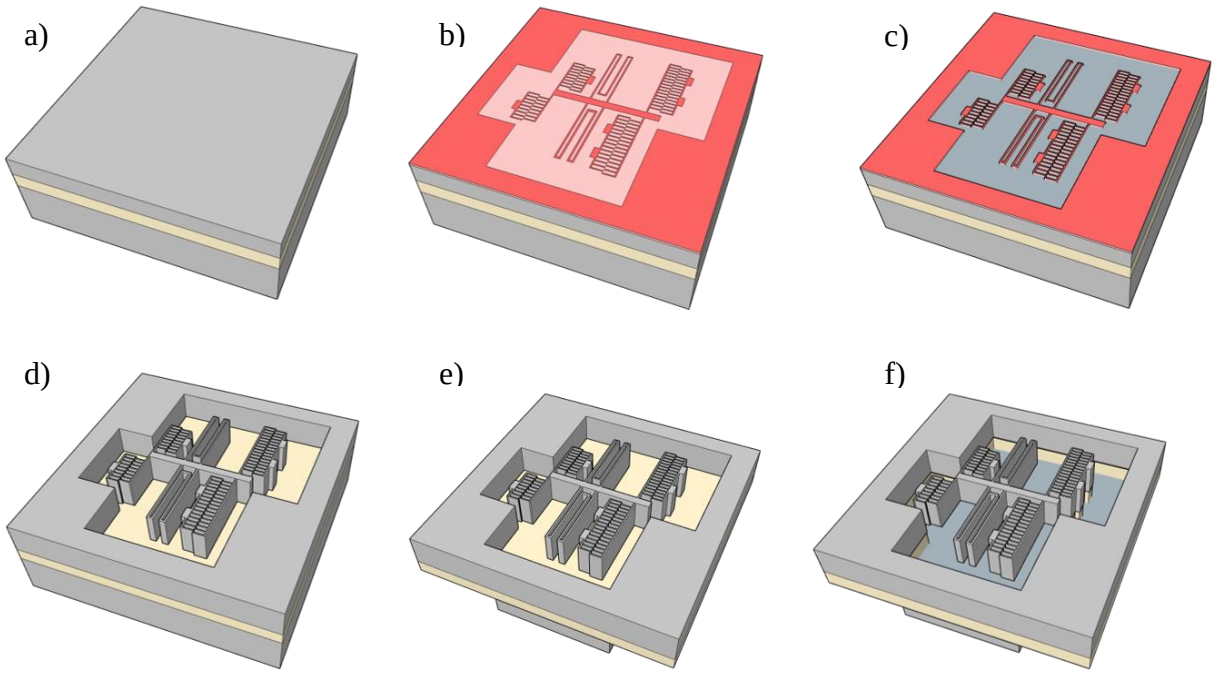

Figure 4: Process flow for the microfabrication of the contactless capacitive MEMS device: a) SOI wafer; b) coating with the ECI photoresist and mask exposure; c) pattern development in MF-CD-26; d) Bosch process – pattern transfer in the top silicon layer; e) backside etching of bulk silicon; f) releasing of the moveable structures in hydrofluoric acid – wet etching of buried oxide.

The preliminary tests for the determination of optimal photolithography and etching parameters were performed on pure silicon wafers. The fabricated test-patterns included sets of identical parallel lines. The sets were varying in line widths and gaps between them. These test structures were used to determine the smallest line width that could be used as the width of the fingers in comb-drive structures. The narrower the fingers are in the comb-drive, the smaller is the footprint of the entire gate. Exposure dose for 1.1 µm thick ECI photoresist was varied from $700\,\frac{\mathrm{mJ}}{\mathrm{cm}^2}$ to $1600\,\frac{\mathrm{mJ}}{\mathrm{cm}^2}$ in $100\,\frac{\mathrm{mJ}}{\mathrm{cm}^2}$ steps, whereas the focus was varied from -1 µm to 0.3 µm in 0.1 µm steps. The etching was performed for 65 s using Bosch procedure. The combination of exposure dose and focus that yielded the structures closest in size to the ones on the mask. Underetching was measured to be about 20 nm. This can be compensated at the design level or considered in our modeling in order to ensure a proper operation of the devices.

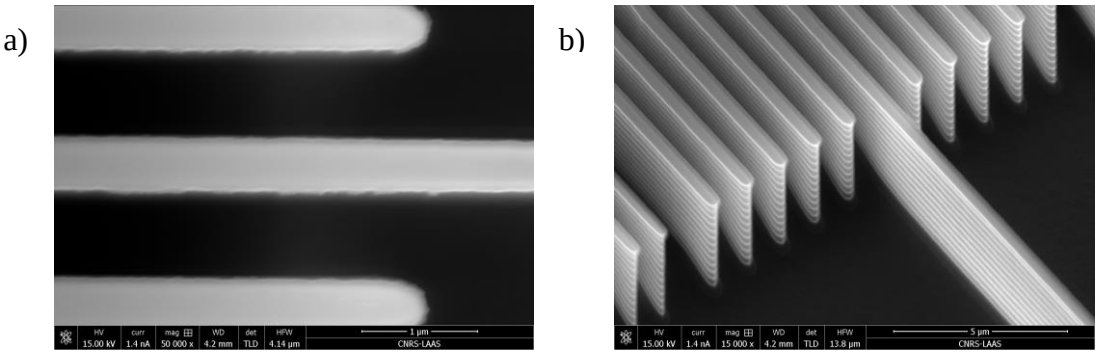

Figure 5: SEM images of the test structures consisting of sets of parallel 0.5µm wide lines separated by 0.5 µm gaps. The structures were exposed with the dose of 700 $\frac{mJ}{cm^2}$ and with the focus of -0.3 µm.

5 Conclusion

In this paper we introduce an architecture of logic gates and circuits aiming to reach ultra-low power operation, with lower energy dissipation than any CMOS circuit. The paradigm is based on capacitive MEMS devices in a differential architecture, operated in the adiabatic regime. Several design considerations and trade-offs have to be considered to reach the goal, in particular to ensure that a logic differentiation of the output voltage is high enough to enable complex circuits cascading multiple gates. In the current state of research, the devices are realized with MEMS-based tunable capacitors using comb drive actuators and foremost a very fine knowledge of their behavior is necessary. The FEM analyses provided the fundamental information that was necessary for the design of the

logic gate and the subsequent floor planning for the device fabrication on SOI wafers. From the microfabrication tests performed in the cleanroom we managed to identify the most optimal fabrication conditions. The next steps in the project would be realization of the devices, i.e. single logic gates and more complex digital circuits, in LAAS followed by their electrical and electromechanical characterizations.

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References

[1] H. Fanet, Ultra Low Power Electronics and Adiabatic Solutions. Hoboken, NJ, USA: *Wiley*, 2016, doi: 10.1002/9781119006541

[2] R. Landauer, "Irreversibility and heat generation in the computing process," *IBM J. Res. Dev*., vol. 5, no. 3, pp. 183–191, 1961, doi: 10. 1147/rd.53.0183

[3] H. Samaali, Y. Perrin, A. Galisultanov, H. Fanet, G. Pillonnet and P. Basset, « MEMS four-terminal variable capacitor for low power capacitive adiabatic logic with high logic state differentiation », *Nano Energy*, vol. 55, p. 277-287, 2019, doi: 10.1016/j.nanoen.2018.10.059.

[4] Z. A. Ye et al., "Demonstration of 50-mV digital integrated circuits with microelectromechanical relays," in *IEDM Tech. Dig*., 2018, pp. 411–414, doi: 10.1109/IEDM.2018.8614663.

[5] G. Pillonnet, H. Fanet and S. Houri, "Adiabatic capacitive logic: A paradigm for low-power logic," *2017 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2017, pp. 1-4, doi: 10.1109/ISCAS.2017.8050996.

[6] Y. Perrin, A. Galisultanov, L. Hutin, P. Basset, H. Fanet and G. Pillonnet, "Contact-Free MEMS Devices for Reliable and Low-Power Logic Operations," in *IEEE Transactions on Electron Devices*, vol. 68, no. 6, pp. 2938-2943, 2021, doi: 10.1109/TED.2021.3070844.

[7] O. Loh and H. D. Espinosa, "Nanoelectromechanical contact switches," *Nature Nanotechnology*, vol. 7, No. 5, pp. 283-295, 2012.

[8] C. Pawashe K. Lin, K.J. Kuhn, "Scaling limits of electrostatic nanorelays," *IEEE Trans. Electron Devices*, vol. 60, pp. 2936–2942, 2013.

[9] P. Teichmann, "Adiabatic Logic: Future Trend and System Level Perspective," *Springer*, 2012, DOI. 10.1007/978-94-007-2345-0.

[10] A. Galisultanov, Y. Perrin, H. Samaali, H. Fanet, P. Basset and G. Pillonnet, "Contactless four-terminal MEMS variable capacitor for capacitive adiabatic logic", *Smart Materials and Structures*, 2018.