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TiTe/$Ge_2Sb_2Te_5$ Bi-layer-based Phase-Change Memory Targeting Storage Class Memory

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***Abstract*—In this work, we introduce an innovative Phase-Change Memory (PCM) based on a TiTe and $Ge_2Sb_2Te_5$ (GST) bi-layer stack that presents low resistance variability since the out-of-fabrication in 4 kb array. It allows creating reliably an intermixed system right from the first programming in the active volume of the device. TiTe/GST PCM exhibits higher speed, lower variability of intermediate resistance states and lower drift compared to standard GST. An endurance of more than 10^8 cycles can be achieved and we found a reduced cycle-to-cycle variability even after endurance stress. Such new TiTe/GST stack, based on our results, demonstrates to be a valuable candidate for PCM targeting Storage Class Memory applications.**

I. Introduction

In the last years, the memory hierarchy is facing a big challenge in covering the gap between DRAM and Flash memory. Indeed, DRAM features high speed and endurance, whereas Flash memory is characterized by high density and low cost, but limited speed and endurance [1]. This gap can be filled by a new category of memory called Storage Class Memory (SCM) that would bring non-volatility close to DRAM improving system performances in terms of speed and density and, moreover, reducing the power consumption. Among Non-Volatile Memories (NVM), Phase-Change Memory (PCM) is considered the best candidate for SCM for its high speed, high density and high endurance [2], also after having proved to be a mature NVM entering both standalone [3] and embedded market [4]. PCM working principle is based on a reversible phase transition from a crystalline low resistive phase (SET) to an amorphous high resistive one (RESET). Material engineering in PCM is the key method to improve speed and endurance performances to target SCM requirements. For example, Sb-rich GST has been recognized as a suitable phase-change material for SCM thanks to its ns range programming time [5] and a record endurance of 2×10^{12} [6]. However, these materials require a very good control of the stoichiometry, which otherwise could induce devices variability. Moreover, they present a really steep SET-to-RESET characteristic [5], which prevents the possibility of achieving intermediate states with low variability i.e. multi-level cell (MLC). Another example of phase-change material with reduced compositional and structural variability is the multilayer based on TiTe/Sb_2Te_3 stack that ensures also good speed and cyclability [7], however requiring a huge stability of the multilayer structure that could result difficult along cycling.

For the first time, we introduce a relatively simple PCM structure based on TiTe and $Ge_2Sb_2Te_5$ (GST) bi-layer stack, which ensures low device-to-device variability (D2D) already at the out-of-fabrication thanks to a TiTe layer that features low resistivity and high stability in temperature. An initialization step drives a reliable intermixing of TiTe and GST. We explore the SET speed, the MLC capability, drift in temperature and in time as well as cycle-to-cycle (C2C) variability in 4 kb, making a comparison with standard GST based PCM. Results are supported by Transmission Electron Microscopy (TEM) and Energy-Dispersive X-ray spectroscopy (EDX) analyses. Finally, we analyze the behavior of TiTe/GST devices before and after endurance stress highlighting an extremely low variability of the resistance states even after cycling.

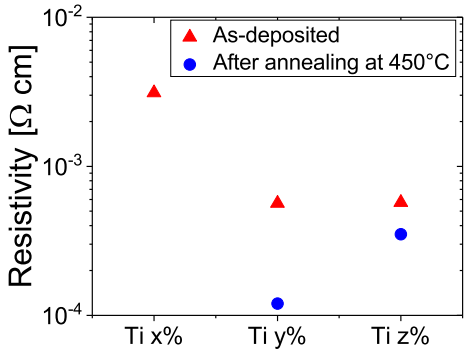


Fig. 1. Resistivity of TiTe samples with three different percentages of Ti (x, y and z with x<y<z) measured at room temperature before and after annealing at 450°C. The resistivity after annealing of the layer with Ti x % is not reported since the layer resulted degraded after the test.

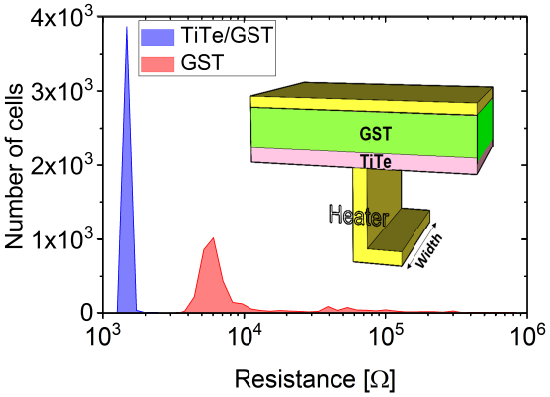


Fig. 2. As-fabricated resistance distributions of TiTe/GST and GST 4 kb arrays. Inset: simplified scheme of the studied "Wall" PCM device based on TiTe/GST bi-layer stack.

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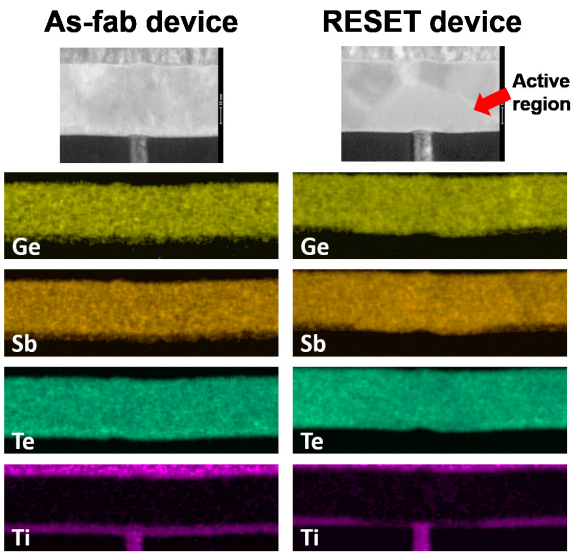


Fig. 3. TEM/EDX analyses performed on as-fabricated TiTe/GST device (left column) and on a device programmed in the RESET state after initialization (right column).

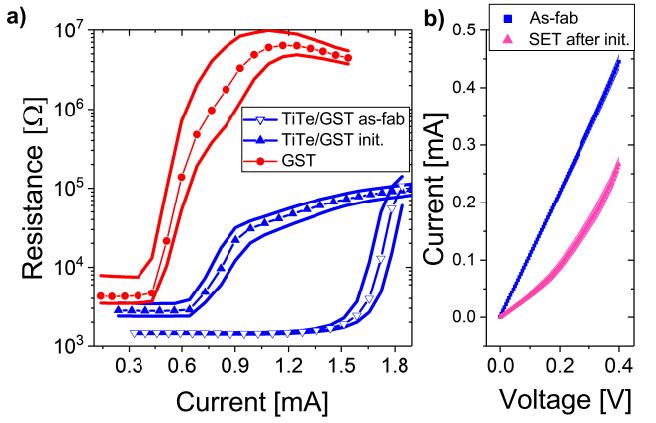


Fig. 4. a) Resistance as a function of current measured in 4 kb array for GST and TiTe/GST devices starting in the SET state. We represent median values and 1σ intervals, and in particular before (as-fab) and after initialization (init.) for TiTe/GST. b) Current-Voltage (I-V) characteristics of five TiTe/GST PCM devices as-fabricated (as-fab) and after initialization in the SET state (SET after-init.).

II. TiTe/GST Bi-Layer Development and Characterization

In order to ensure stability against Back-End-of-Line (BEOL) fabrication process thermal budget, we engineered the thin TiTe layer integrated in our PCM devices. For this purpose, we deposited three TiTe layers with different percentages of Ti ranging from ∼10 at.% to ∼50 at.% (addressed as Ti x, y, z% with x<y<z) and we measured at room temperature the resistivity of TiTe layers before and after annealing at 450°C by four-probe method (**Fig. 1**). The resistivity of TiTe layer decreases as the Ti content increases due to its metallic nature. The layer with Ti z% maintains a resistivity similar to the initial one after being annealed, showing a higher stability compared to the layers with less Ti content. For this reason, we selected Ti_zTe_{100-z} as thin layer to be co-integrated with a GST layer in "Wall" PCM devices, as described in the inset of **Fig. 2** (this PCM will be addressed as TiTe/GST in the following). We performed electrical characterization on 4 kb arrays consisting of PCM devices with a heater width of 100 nm integrated into the BEOL of LETI Memory Advanced Demonstrator (MAD) based on 130 nm CMOS technology.

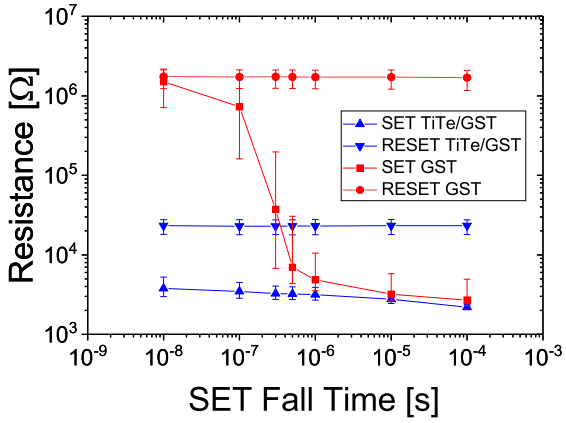


Fig. 5. SET speed test performed on TiTe/GST and GST 4 kb arrays. Data are obtained applying a SET pulse with optimized current, 300 ns width time and incremental fall time on arrays pre-programmed in RESET state before each SET pulse. RESET state resistance is reported as well.

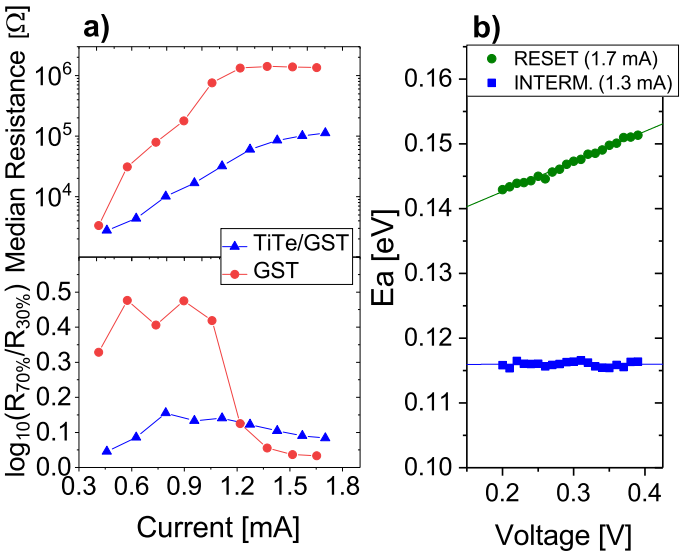


Fig. 6. a) Intermediate states obtained in GST and TiTe/GST applying 300 ns squared pulses with increasing current intensity pre-programming the array in the SET state before each pulse. Median (above) and variability (below) of the resistances in 4 kb arrays are represented. The variability was calculated as the ratio between the 70th and the 30th percentile of the 4 kb resistances. b) Activation energy of the conduction measured from I-V characteristics of TiTe/GST (not reported), for RESET state and an intermediate state, following the model from [8].

A. TiTe/GST Programming Characteristics

Resistance of as-fabricated devices is reported in Fig. 2 showing an extremely low dispersion in TiTe/GST with respect to GST. Such low resistance variability is ensured by the low resistive Ti_zTe_{100-z} layer, which offers a good temperature stability against fabrication process thermal budget. This is confirmed by TEM/EDX analyses of **Fig. 3** illustrating that the TiTe layer remains intact after the fabrication, while in

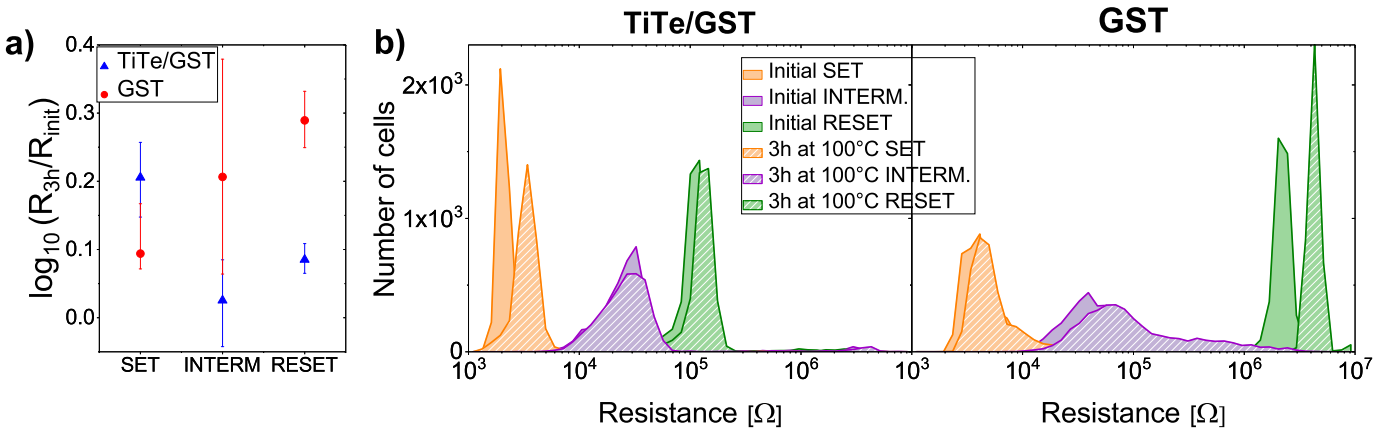


Fig. 7. Data retention evaluated after annealing at 100°C for the SET, intermediate and RESET states in TiTe/GST and GST 4 kb arrays. a) The resistance drift is quantified as the ratio between the resistance measured after a 3 hours annealing and the initial resistance. Median values and variability are represented. b) Resistance distributions of the three states before and after 3 hours annealing at 100°C.

a programmed TiTe/GST the TiTe layer is no longer visible in the active region due to the intermixing of TiTe with GST. The R-I curve in **Fig. 4a** evidences that as-fabricated TiTe/GST devices need an initialization step to give rise to the intermixing of TiTe with GST in the active region. Such initialization effect is also highlighted by current-voltage (I-V) measurements in Fig. 4b: as-fabricated TiTe/GST devices exhibit an ohmic behavior, while after the initialization and the first programming in the SET state, the I-V characteristic changes showing an exponential behavior. Resistance-Current (R-I) curve of TiTe/GST devices after initialization shows an extremely low variability and more gradual SET-to-RESET transition with respect to GST, despite a reduced resistance window. The SET speed is evaluated in (**Fig. 5**) indicating that GST needs pulses longer than 1 µs to obtain a reliable SET state, whereas in TiTe/GST the SET operation is achievable using pulses with a short fall time lower than 10 ns. MLC capability is analyzed in **Fig. 6a**, which reports the resistances obtained applying pulses of increasing intensity in arrays programmed in the SET state before each pulse. GST shows a higher variability, except for the RESET state. On the contrary, a low variability of all the programmed states is confirmed in TiTe/GST. The activation energy of conduction (E_A) of the RESET state and of an intermediate state in TiTe/GST is measured from subthreshold I-V realized at different temperatures (Fig. 6b) according to [8]. In common phase-change materials, such as GST, the amorphous phase shows a trap-limited transport described by Poole-Frenkel mechanism, where E_A decreases with increasing voltage [8]. In the case of TiTe/GST, E_A is not dependent on the voltage for the intermediate state and it increases with voltage for the RESET state. Moreover, TiTe/GST presents a low E_A ($\sim$ 0.1 eV i.e. small energy gap) compared to GST (0.37 eV) [8]. These results evidence a different conduction mechanism in RESET TiTe/GST that appears more close to a metallic behavior, with the presence of defects that generates scattering, increasing E_A value as the electric field increases.

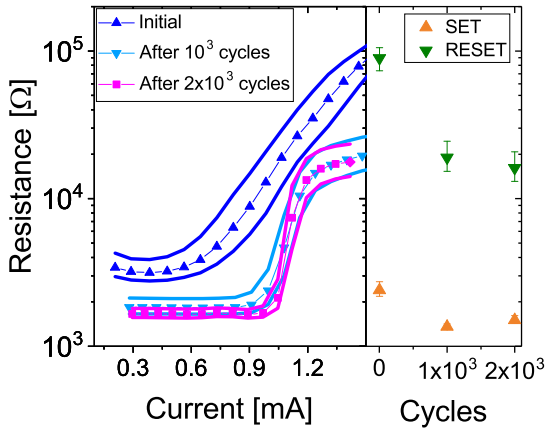


Fig. 8. Left: R-I characteristic at the beginning of the devices life and after endurance for TiTe/GST. Right: 4 kb TiTe/GST SET and RESET resistances evolution along cycles performed with pulses of 10 µs to accelerate and evidence the evolution.

B. Data Retention

Data retention in our PCM devices was investigated comparing the resistance states values before and after an annealing at 100°C for 3 hours. The resistance drift is quantified for each device of the array in **Fig. 7**. SET state drifts more in TiTe/GST than in GST devices, likely due to the presence of defects in the crystalline matrix of the material related to Ti inclusion. GST intermediate state shows a large spread in the behavior of the devices after annealing, that is suppressed in TiTe/GST. The RESET state is also more stable in TiTe/GST with respect to GST. We think that the (almost) metallic behavior of amorphous TiTe/GST observed in previous E_A analyses contributes to the improved stability in this material.

C. Endurance

In order to analyze the behavior of TiTe/GST during cycling, R-I curves and SET and RESET resistances before and after endurance stress are reported in **Fig. 8**. The cycles were executed with long pulses of 10 µs for accelerated aging. After 10^3 cycles, the R-I curve evolves and SET and RESET resistances decrease. Additional 10^3 cycles, applied with the same protocol, highlight that this evolution is not detrimental

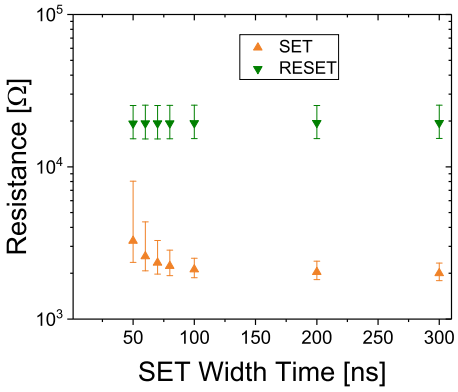


Fig. 9. SET speed test realized in TiTe/GST 4 kb array after endurance test performed in Fig. 8b, using SET pulses with increasing width time and short constant fall time of 10 ns.

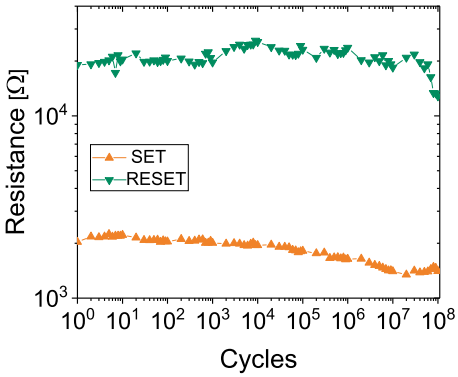


Fig. 10. Endurance evaluated in a TiTe/GST device with optimized SET and RESET pulses (width time = 50 ns, rise/fall time = 10 ns).

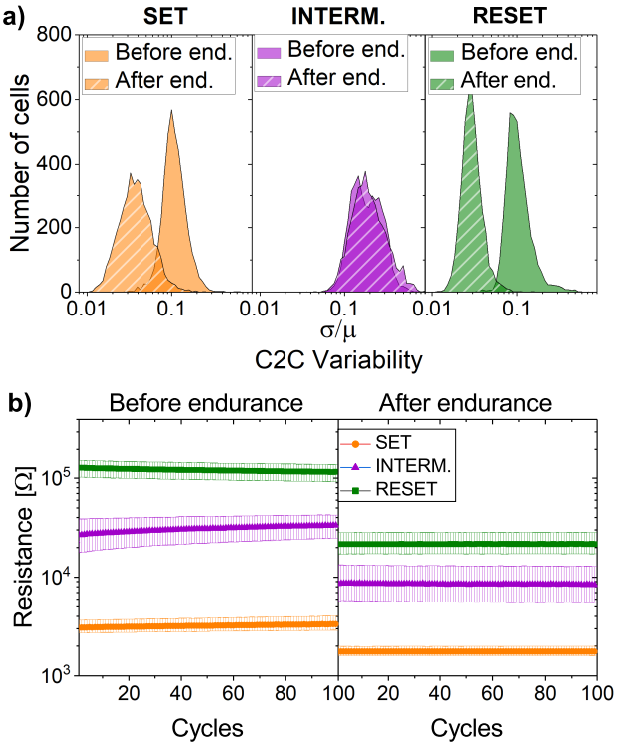


Fig. 11. Variability of SET, RESET and intermediate states evaluated along 100 programming cycles (SET/RESET pulses of 50 ns) in TiTe/GST 4 kb arrays, before and after an endurance test compatible with the one performed in Fig. 8. a) C2C variability distributions: for each device in the array the C2C variability was calculated as the ratio between the standard deviation of the resistance value and its median resistance along 100 cycles. b) D2D variability: median and standard deviation for the 4 kb resistance values along the 100 cycles.

and the devices achieve an extremely stable behavior. Indeed, we realized that the composition achieved in the active region of the PCM features unique stability properties. **Fig. 9** shows the programming SET time kept in tens of ns range and an endurance higher than 10^8 cycles without the use of any smart programming protocol (**Fig. 10**). The devices were still perfectly functional after all the stresses applied. The C2C and D2D variability in TiTe/GST 4 kb arrays along 100 cycles were evaluated for SET, intermediate and RESET state before and after the endurance stress (**Fig. 11**). The three states modify their resistance values after cycling, as shown in Fig. 11b, compatibly with previous results. Nevertheless, the three states are still perfectly achievable and distinguishable and the C2C variability of SET and RESET states is even reduced after cycling (Fig. 11a). Further analyses are ongoing to reveal the nature of this new composition featuring such striking stability and endurance performances.

III. Conclusions

We investigated through electrical characterization an innovative PCM device based on a TiTe/GST bi-layer stack. The TiTe layer was engineered to be stable after the fabrication process, as demonstrated by the low variable resistance distributions of as-fabricated 4 kb devices and by TEM/EDX analyses. The first programming into the high resistive state gives rise to a new alloy made by GST and TiTe, that showed improved performances with respect to GST, such as higher speed and intermediate states featuring lower variability. Endurance up to more 10^8 cycles was demonstrated, nevertheless a modification of R-I characteristic and a reduction of SET and RESET resistances were found after aging. The obtained new alloy revealed striking stability along cycling, showing high SET speed and reduced C2C variability even in MLC mode. This new alloy, obtained from our TiTe/GST investigation, holds great promise for targeting DRAM-like performances for SCM applications.

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