A Mixed Method to Mitigate the TID Effects on 28nm FDSOI Transistors

A. Ureña Acuña, J. M. Armani, M. Slimani, M. Cassé, P. Dollfus, Member, IEEE

***Abstract*—In this work we propose a mixed method to mitigate the effects of Total Ionizing Dose (TID) on 28nm Fully-Depleted Silicon-On-Insulator (FDSOI) MOSFETs exposed to ^{60}Co gamma radiation at two different dose rates. This new thermal-electrical method uses thermal regeneration by applying rapid annealing cycles in addition to threshold voltage modulation inherent in FDSOI technology. Applying this methodology could enhance the transistor reliability during a mission in radiative environments.**

***Index Terms*—FDSOI, Total ionizing dose, annealing, thermal regeneration, electric compensation.**

I. Introduction

Silicon-On-Insulator (SOI) technologies are nowadays considered as an attractive alternative to CMOS-bulk counterpart for applications requiring good performance and low power consumption [1]. Additionally, FDSOI technologies are increasingly used in space applications thanks to their architecture proved to be intrinsically resistant to single event effects (SEE) [2]. However, these technologies have shown a significant sensitivity to TID effects due to radiation-induced charge trapping in the buried oxide (BOX) [3].

Many works have studied radiation sensitivity of FDSOI technologies [4]–[6]. In ref [5], the authors showed that, in some cases, FDSOI transistors can withstand very high dose levels depending on their BOX thickness and channel length. However, in the worst case, the degradation of their electrical characteristics can be quite large. Therefore, appropriate margins should be applied in the circuit design to have electronic systems still able to operate after receiving high TID levels.

Hardening strategies to mitigate TID induced-effects in FDSOI devices have been explored in some recent works. It includes, hardening by design using 3D FDSOI transistor structure [7], body-tieing [4], [8], and substrate biasing [9]. In [9], Gaillardin et al have proposed to calibrate back-bias to cancel threshold voltage shifts induced by TID in NMOS and PMOS Ultra Thin SOI (UTSOI) transistors. However, back-bias technique allows only the compensation of threshold voltage shifts. TID-induced degradation of the subthreshold slope is not recovered, which can affect the switching speed of the device and impact the operating frequency of integrated circuits. On the other hand, thermal annealing has demonstrated its efficiency in the recovery of the electrical characteristics of irradiated devices [5]. However, the high temperature used can accelerate the ageing degradation of the circuit and reduce its lifetime. In this work we propose a mixed thermal/electrical hardening strategy combining thermal annealing and back-bias mitigation techniques. The aim of this method is to reduce the annealing temperature used to regenerate the device in order to have less impact on its reliability. For that purpose, we take advantage of the front and back gate coupling effect, inherent in FDSOI technology, that allows to compensate the threshold voltage shift by applying a back-gate voltage.

This paper is organized as follows. In Section 2, we explain thermal annealing and back-bias technique for TID effects mitigation. Section 3 presents experimental gamma radiation details. In Section 4, we discuss experimental results and we propose a new mitigation strategy. Section 5 discusses the eventuality of dose-rate effects in the irradiated devices. In section 6, the possible impact of the proposed methodology on the reliability of the device is analyzed. Finally, concluding remarks are drawn in Section 7.

II. Mitigation methods

A. Thermal annealing approach

Thermal annealing consists in applying high temperature to irradiated devices in order to accelerate radiation-induced charge detrapping process, which results in a quick regeneration of the electrical characteristics of the device. This may also occur at room temperature, but following a slow process that can take many years [10]. Physically, charge detrapping in oxides is a thermally activated process that can be modeled by a first order kinetics with a probability of trap emission given by [11]:

$$\sigma = Ae^{\frac{-E_a}{kT}} \tag{1}$$

where A is the frequency factor (s^{-1}), E_a is the activation energy (eV), k is the Boltzmann constant and T is the absolute temperature (K). So, to reach a specific activation energy, the annealing time and temperature must be chosen following the time-temperature equivalence described in [10]. Hence, we can predict the annealing time for a specific activation energy. Previous works have shown that for high TID levels, an annealing temperature around 300 °C should be applied to achieve a correct regeneration [5]. As shown in [12] the application of rapid thermal annealing cycles at high temperatures can recover rapidly the TID effects, however, such a high temperature can cause accelerated aging degradation and

Manuscript received April 12, 2020.

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results in reliability issues of electronic devices and its lifespan is severely impacted.

B. Back-gate bias

An interesting feature of FDSOI devices is the coupling between the front and back transistors allowing threshold voltage control and resulting in multiple advantages over bulk ones such as higher operation frequency and lower power consumption. Back-bias approach for TID mitigation consists in applying a voltage to the back-gate (substrate) in order to compensate TID-induced threshold voltage shifts on NMOS and PMOS transistors [9], [13]. In a FDSOI transistor, the variation of the front threshold voltage ΔV_{tf} can be expressed as function of a variation of the back-gate biasing ΔV_{bg} as [13]:

$$\Delta V_{tf} = n\Delta V_{bg} \quad ; \quad n = \frac{C_{Si}C_{BOX}}{C_{OX}(C_{Si}+C_{BOX})}, \qquad (2)$$

with C_{Si} the silicon layer capacitance, C_{OX} the front gate oxide capacitance and C_{BOX} the buried oxide capacitance. The value of n coefficient, also called "body factor" is around 85 mV/V for a pristine device [14]. For this study we have used two types of FDSOI transistors [15]: low threshold voltage (LVT) and regular threshold voltage (RVT) transistors, depicted in Figure 1. RVT transistors are built on a standard well while LVT ones are built on a flip well. As shown in Figure 1, applying reverse body biasing (RBB: negative body bias voltage) shifts the threshold voltage in the positive direction while forward body biasing (FBB: positive body bias voltage) induces a shift in the negative direction.

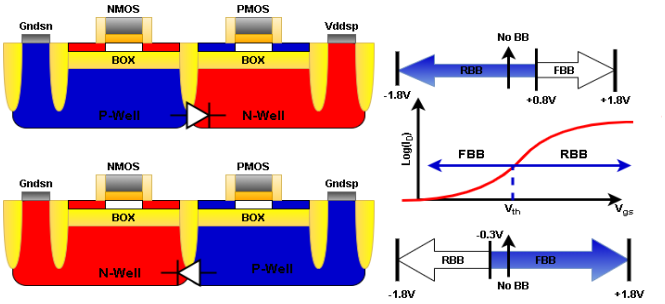

Figure 1. Cross-sectional view of FDSOI RVT/LVT transistors and illustration of back-bias effect on the threshold voltage.

Under radiation environment, RVT transistors allow a better compensation of TID-induced threshold voltage shift than LVT ones due to the possibility to apply a large RBB. In [9], the authors showed that a significant back-bias voltage should be applied in order to counterbalance 1 kGy (100 krad) irradiation induced-effects on PMOS and NMOS UTSOI transistors. For high dose levels above 10 Mrad, such technique is no longer sufficient to recover TID-induced threshold voltage shifts due to the body bias voltage limit of the technology.

III. Experimental Details

The tested devices are transistors processed by STMicroelectronics with short-narrow and wide-long dimensions and different substrates (LVT and RVT). The characteristics of the transistors are summarized in Table I. Two wafers with 12 transistors (6 NMOS and 6 PMOS) on each were irradiated with a ^{60}Co γ-ray source at ArcNucleART facility in Grenoble, France. The two wafers, Wafer 1 (W1) and Wafer 2 (W2), were irradiated during 88 hours at dose rates of 1.3 kGy/h (36.1 rad/s) and 115 Gy/h (3.2 rad/s), respectively. These two different values were chosen in order to observe the influence of the dose rate on the devices. The total dose was deposited in several steps to reach 115 kGy (11.5 Mrad) on W1 and 10.12 kGy (1.012 Mrad) on W2. The irradiated transistors have a thin BOX thickness T_{BOX} = 25 nm and a gate oxide thickness T_{OX} = 1.8 nm (GO1). Only 2 transistors for each wafer have a gate oxide thickness of 2.8 nm (GO2). All devices have been irradiated unbiased because the samples were designed for probe testing only and not intended to be packaged. In [9], [16] authors show that the influence of an electric field during irradiation further degrades the electrical characteristics of the device. However, this should not call into question our work aiming to establish a new hardening strategy. To observe the degradation of the electrical characteristics of the FDSOI devices, I-V and C-V measurements were performed before experiment and immediately after each irradiation step. V_{bg} was applied during the electrical characterization according to the limits established by the manufacturer for both the LVT and RVT transistors, in order to observe the effect of the inter-substrate junctions and the compensating capacity of V_{bg}.

Table I
Characteristics of tested MOSFETs on both wafers.

Type	Transistors	W	L
LVT	NMOS1	*Wide*	*Long*
	NMOS2	*Narrow*	*Short*
	NMOS3 (GO2)	*Wide*	*Long*
	PMOS1	*Wide*	*Long*
	PMOS2	*Narrow*	*Short*
	PMOS3(GO2)	*Wide*	*Long*
RVT	NMOS4	*Wide*	*Long*
	NMOS5	*Narrow*	*Short*
	NMOS6	*Narrow*	*Short*
	PMOS4	*Wide*	*Long*
	PMOS5	*Narrow*	*Short*
	PMOS6	*Narrow*	*Short*

The annealing process has been applied after the irradiation was completed. Four isochronal thermal annealing cycles were applied to all devices with temperatures of T_1 = 150 °C, T_2 = 175 °C, T_3= 200 °C and T_4 = 250 °C with a duration Δt of 18 minutes. I-V measurements were made immediately after each cycle at room temperature to observe the progressive regeneration of the electrical characteristics of the irradiated devices as shown in Figure 2.

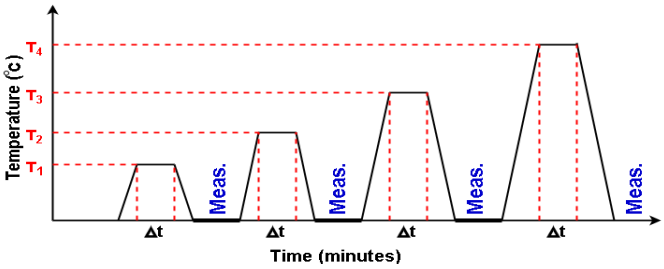

Figure 2. Isochronal annealing applied to FDSOI transistors

IV. Results and Discussion

To analyze the effects of TID on the irradiated FD-SOI transistors and verify the effectiveness of the proposed methodology, we have extracted some key parameters using the methods described in [17], [18]. The main parameters extracted were: the threshold voltage (V_{th}), the subthreshold slope (SS), the density of charges trapped in the oxides (N_{ot}) and the density of charges trapped at Si/SiO_2 interface (D_{it}).

In Figure 3, continuous and dashed curves show I_d versus V_{gs} before irradiation and after 115 kGy of total dose respectively. The results showed here are those of NMOS1 transistor but all other irradiated devices present the same dynamics. The maximum observed shift of the threshold voltage is 192 mV corresponding to NMOS3 due to its thicker gate oxide (GO2). The mean threshold voltage shift is about 150 mV on GO1 transistors while the subthreshold slope degradation is around 25% on average. In the next sub-sections, thermal annealing and back-bias mitigation techniques were applied to the irradiated devices in order to analyze their efficiency and their limits. Then, the proposed thermal/electrical strategy is explained.

A. Thermal Regeneration

As shown in Figure 3, applying thermal annealing progressively cures TID effects. Figure 5 shows the evolution of oxide trapped charges N_{ot} and Figure 6 the $Si - SiO_2$ interface trapped charges density of NMOS LVT/RVT devices on Wafer 1 during the experiment. NMOS1 and NMOS4 have exactly the same dimensions and different substrate as well as NMOS2 and NMOS5 (see Table I). As expected, the applied temperature progressively detraps the charges in the gate oxide, which explains the recovery of the threshold voltage. For NMOS2 and NMOS5 devices, we notice a saturation of charges from 21.4 kGy, which explains why the threshold voltage does no longer shift with the accumulated dose. This saturation can be explained by the small dimensions of the gate oxide (short/narrow). The remaining threshold voltage and subthreshold slope degradation after annealing at 250 °C is on average about $\Delta V_{th} = 22$ mV and $\Delta SS = 4.5\%$, respectively. To get a total recovery of the device characteristics, we can consider increasing the temperature or the time of the annealing process. However, on one hand the exposure of electronic devices to higher temperature can cause accelerated ageing degradation and reliability issues. On the other hand, increasing the annealing time would make the system unavailable for longer time.

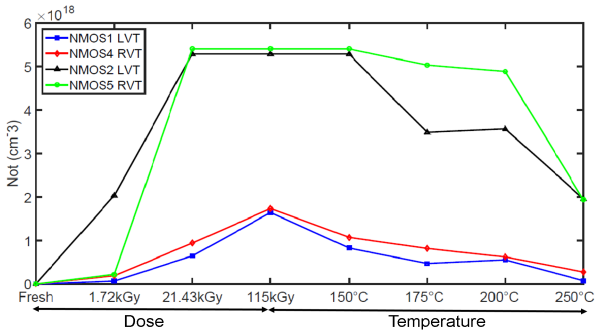

Figure 5. Time evolution of the oxide-trapped charges on devices of Wafer 1 over the irradiation and annealing steps.

Similarly, in the case of W2, irradiated at a lower dose-rate, a maximum $\Delta V_{th} = 194$ mV was observed for NMOS3 due to its thicker gate oxide. The same dynamics of V_{th} recovery as for W1 was observed for all tested transistors. For GO1 devices, the average degradation observed is around $\Delta V_{th} = 110$ mV and $\Delta SS = 12\%$.

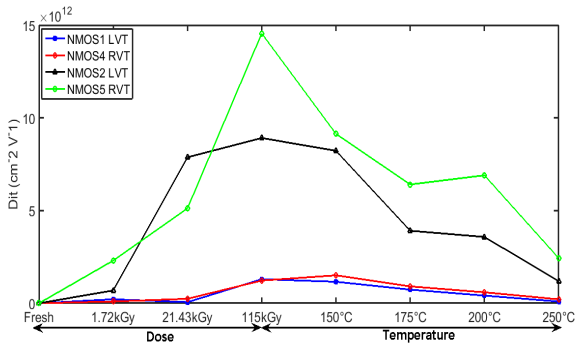

Figure 6. Time evolution of the interfaces trapped charges on devices of Wafer 1 over the irradiation and annealing steps.

As described in the state of the art, the interface trapped charges degrade the subthreshold slope producing a slower response of MOSFET devices. As shown in [19] the interface trapped charges at $Si - SiO_2$ (D_{itf}) and the interface trapped charges at $Si - BOX$ (D_{itb}) have a direct impact on the body factor **n** defined previously. The charges created in the oxide move slowly occupying both interfaces. In this case, a thermal annealing cycle becomes necessary to detrap these charges and thus recover the degraded slope. Figure 6 shows the evolution of the density of charges trapped at both interfaces during irradiation and after each annealing cycle. Short channel devices show a more rapid increase in their interface trapped charges density than long channel ones. This occurs because the charges populate the interface in a faster way due to the reduced volume of the oxides. The direct consequence is a more severe degradation of the subthreshold slope.

B. Back-gate voltage Compensation

Figure 4 shows results of applying multiple values of back-gate voltage. We notice that the back-bias technique allows the compensation of the threshold voltage shift induced by radiation, but due to the high levels of TID applied to Wafer 1, the V_{bg} is not sufficient to fully compensate for the degraded

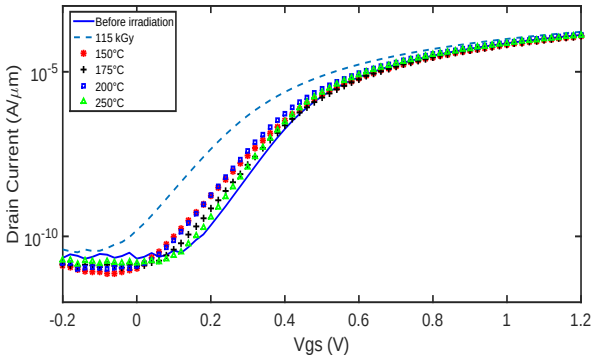

Figure 3. Isochronal annealing applied to NMOS1 on Wafer 1.

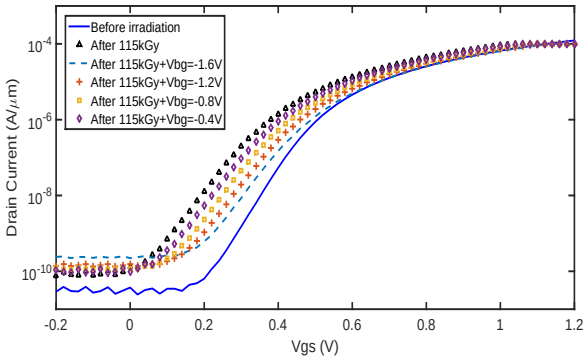

Figure 4. Back-gate bias applied to NMOS4 on Wafer 1.

electrical characteristics of the transistors. For Wafer 2, we were able to totally cancel the TID induced threshold voltage degradation by applying a V_{bg} of -1.6 V to most transistors. However, as expected, back-bias technique does not recover the degradation of the subthreshold slope.

C. Mixed Thermal/Electrical Method

As previously shown, the back-bias technique allows to counterbalance TID-induced threshold voltage shift but does not repair the subthreshold slope degradation. On the other hand, annealing technique has the disadvantage of using elevated temperature to recover both transistor characteristics. In this work, we propose a combined thermal/electrical method that takes advantage of both mitigation techniques: back-bias to limit the heating temperature and annealing to recover subthreshold slope. Figure 7 shows the I_d versus V_{gs} characteristics of NMOS4 transistor before irradiation and after applying annealing with different back-bias voltages.

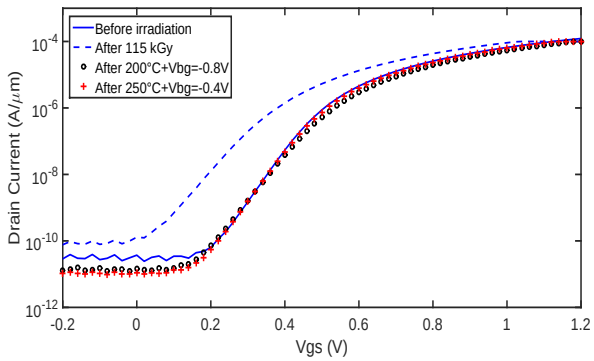

Figure 7. Thermal/Electrical method applied to NMOS4.

As shown in Figure 4, with a V_{bg} = -0.4 V, the remaining uncompensated threshold voltage shift is about 110 mV. Applying annealing approach at 250 °C with a V_{bg} of -0.4 V results in a total recovery of the threshold voltage degradation and only ΔSS of 4% is still observed. In order to keep a relatively reduced annealing temperature ($T \leq 200$ °C), the RBB voltage should be decreased from -0.4 V to -0.8 V allowing the recovery-compensation of the total threshold voltage shift. In this case, the remaining subthreshold slope shift is about 10%. Clearly, a trade-off between the annealing temperature and the subthreshold slope recovery has to be considered. The subthreshold slope degradation may impact the operating frequency and this could not always be tolerated by the system. In this case, the annealing temperature/time should be increased. As an example, we fixed acceptable degradation limits for tested devices to $\Delta V_{th} \leq 5$ mV and $\Delta SS \leq 10\%$ and we searched the optimum couple (T, V_{bg}) that mitigates the effects of TID on FDSOI-RVT transistors with the lowest possible temperature.

We notice that for almost all transistors, we can reach the required mitigation level using an annealing temperature of 200 °C. However, PMOS transistors with narrow/short gate dimensions require a higher temperature of 250 °C as can be seen in Figure 8. This can be explained by the saturation of oxide trapped charges as shown in Figure 5. To ensure a good mitigation, such transistors should be avoided in the circuit design.

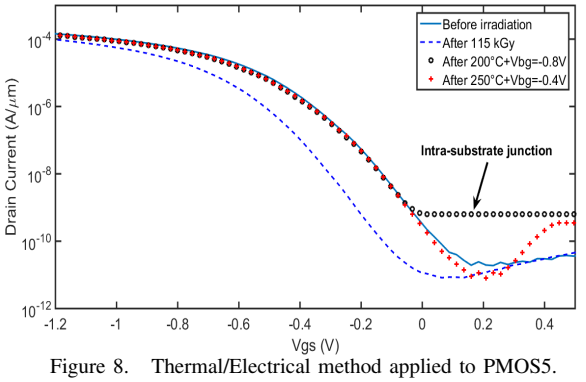

Figure 8. Thermal/Electrical method applied to PMOS5.

D. Irradiated transistors on Wafer 2

As mentioned, W2 was irradiated at 115 Gy/h up to a TID of 10.12 kGy. This dose is similar to those found during a long-term space mission. The irradiated devices showed the same electrical degradations than those of W1. Being irradiated at a much lower TID level than W1, FDSOI devices of W2 have less threshold voltage shift. As was also observed in W1, the PMOS transistors showed a higher ΔV_{th} than the NMOS transistors with a maximum value of 230 mV and 194 mV respectively. At this dose level, the ΔV_{th} of NMOS

transistors can be compensated by only applying the electrical compensation as shown in figure 9. We noticed in these devices that the subthreshold slope was not severely impacted by the TID. The maximum ΔSS in the irradiated devices was 8%. This phenomenon can be explained by the predominance of trapped charges in the volume of oxides created at a low dose rate. After being trapped, these charges will slowly begin to move towards the interfaces. On the other hand, the charges created by a higher dose rate will have a tendency to occupy both interfaces more quickly, severely degrading the slope as can be observed in the W1 devices.

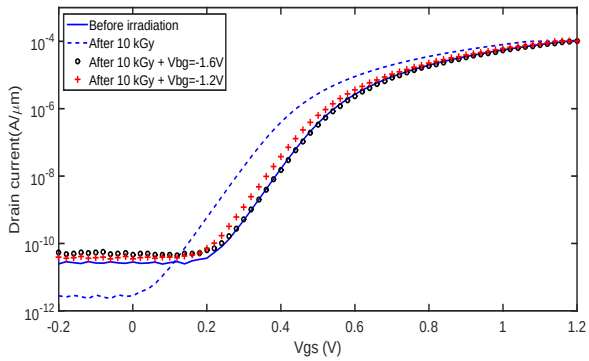

Figure 9. Thermal/Electrical method applied to NMOS4 Wafer 2.

Table II summarizes the obtained results for RVT tested transistors, where ΔV_{thr} and ΔSS_r are the remaining parts of degradation after applying thermal/electrical mitigation on both wafers.

Table II
(T-V_{bg}) OPTIMUM COUPLE TO MITIGATE TID EFFECTS.

Transistors	T (°C)	V_{bg} (V)	$\Delta V_{thr}(mV)$	ΔSS_r (%)
NMOS4 W1	200	−0.8	0.6	9.8
NMOS5 W1	200	−0.8	0.8	8.9
PMOS4 W1	200	−0.8	4.9	4.8
PMOS5 W1	250	−0.8	2.3	7.6
NMOS4 W2	25	−1.6	0.3	4.2
NMOS5 W2	25	−1.6	1.6	7.7
PMOS4 W2	175	−0.4	3.5	8.1
PMOS5 W2	200	−0.4	1.3	8

E. Strategy proposed for TID mitigation

Based on the previous results, we propose a new strategy to mitigate the effects of the ionizing dose in FDSOI circuits. This strategy includes first a pre-characterization of the degradation induced by the TID on elementary FDSOI transistors with different dimensions. Then, during the mission a back-gate voltage, proportional to the degradation of the irradiated device, is applied in order to compensate the threshold voltage shift. In a complex integrated circuit, there are many transistors with different geometries that could have dissimilar TID responses, as we noticed during our experiments. Consequently, a single V_{bg} value could not be enough to fully compensate the transistors all at once. To solve this problem, a series of V_{bg} generators could be implemented by grouping the transistors with similar characteristics for applying the compensation method. The annealing process is started only when the compensation by the electrical technique is no longer efficient to cancel the TID-induced degradation during a short period of time. Once the thermal annealing cycle has finished, the compensation method is activated again, calculating and compensating the residual ΔV_{th}.

V. DOSE-RATE EFFECTS

In order to analyze the dose-rate response of devices on both wafers, a common irradiation step was set at 2 kGy. The charges trapped in the volume of the oxides of MOSFETs transistors can present different time constants and distributions during their transport to the $Si - SiO_2$ interface when irradiated at different dose-rates [20]. As a consequence, the magnitude of the electrical degradations can vary significantly. We noticed that devices irradiated at a dose rate of 115 Gy/h showed a higher V_{th} degradation than those irradiated at 1.3 kGy/h for a TID of 2 kGy. Figure 10 shows a NMOS with long channel that underwent a large degradation with ΔV_{thW1}=-5.7 mV and ΔV_{thW2}= -49 mV.

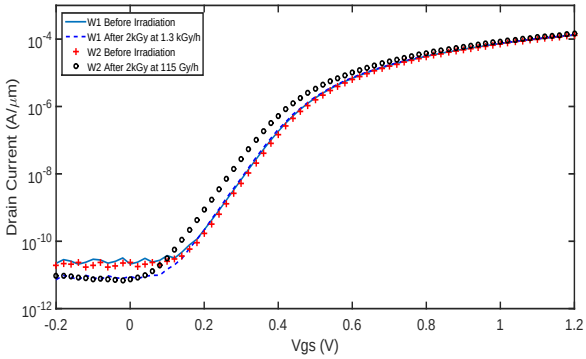

Figure 10. NMOS1 after 2 kGy, irradiated with two different dose rates

Figure 11 shows the dose rate effect on a short channel NMOS device. An initial variation in threshold voltage between both devices was observed purely due to the manufacturing process. On the other hand and as previously demonstrated, the irradiated device of W2 showed a greater degradation of threshold voltage with a ΔV_{thW1}=-25 mV and ΔV_{thW2}= -40 mV.

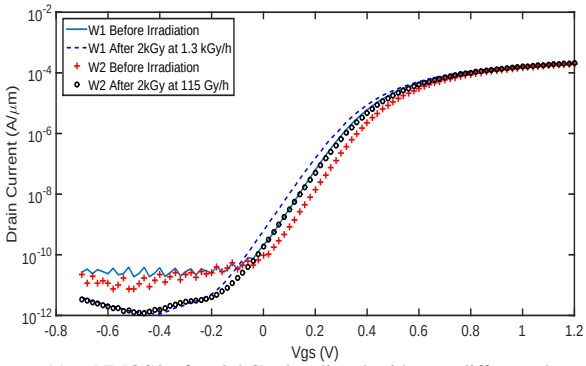

Figure 11. NMOS2 after 2 kGy, irradiated with two different dose rates

VI. RELIABILITY

As described in section 2, a thermal annealing can promote the detrapping of the radiation induced charges in the oxides. The higher the temperature, the greater the recovery of electrical characteristics. However, a high temperature can exacerbate phenomena such as negative bias temperature instability

(NBTI) and electromigration [21] which induce a significant degradation and ageing of the device. Other mechanical effects linked to the thermal expansion of the materials are potential issues when applying numerous thermal cycles at high temperature [22]. Therefore, prioritizing electrical compensation reduces the impact of thermal annealing cycles, safeguarding the reliability of the irradiated device. In contrast, the applied V_{bg} must not exceed the limits established by the manufacturer. The immediate effect would be the conduction of the intra-substrate junctions present in CMOS-FDSOI devices, which will result in a high increase of the power consumption in off-state. This effect can be observed in Figure 8, where the pair (200 °C, -0.8 V) shows the conduction of the intra-substrate junction. Knowing all these factors, we propose to apply a regeneration-compensation or thermal/electrical method in order to reduce the annealing temperature prioritizing the inherent coupling effect proper to the FDSOI technology. This mixed method reduces the negative impact on the device reliability due to the TID and the high temperature.

VII. Conclusions

In this work a new mixed thermal/electrical hardening method using the regeneration-compensation principle has been proposed in order to mitigate the TID effects on FDSOI devices. It is well known that the effects of TID on NMOS and PMOS are different. The V_{th} degradation is less important in NMOS devices due to self-compensating effects such as the rebound effect [20]. These effects were observed during irradiation where PMOS devices showed much more severe V_{th} degradations than NMOS. This is a factor to take into account in the hardening methodology proposed in this article because the pair (T, V_{bg}) will be different in NMOS and PMOS devices for high TID levels. The use of this method is promising for nuclear applications where high TID levels are expected. The TID-induced threshold voltage shift can be compensated using back-bias while annealing can recover both threshold voltage and subthreshold slope degradation. The main advantage of the proposed method is to reduce the impact of the annealing temperature affecting the reliability of the circuit. When implemented in an ASIC, this method requires an extra monitoring block able to automatically apply a back-gate voltage and a controlled heating. Additionally, we used two dose rates during the experiment in order to study the effects of the dose rate. It was found that V_{th} degraded more severely at 115 Gy/h than at 1.3 kGy/h, thus showing the time domain effect of irradiation. Future work will involve the evaluation of this methodology with devices biased in different modes.

Acknowledgments

The authors would like to thank T. Sassolas, P. Vincent, M. Cassé, F. Gaillard, S. Martinie, C. Arnaud, R. Mourot and A. Evans of CEA for the technical support provided during measurements, parameter extraction and thermal annealing of the devices. Special thanks also go to L. Cortella from ArcNucleART for the support provided during the irradiation procedure and R. Gaillard for the contributions on this article.

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