Evaluation of total ionizing dose effects on commercial FRAMs

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***Abstract*—This work evaluates the sensitivity of two commercial ferroelectric random access memories to total ionizing dose. Functional failure analysis and current measurements have been performed as a function of total ionizing dose. Results of testing under Co-60 gamma radiation show a huge difference of radiation hardness levels between FRAM references and give an idea of the most sensitive part causing failure on each memory chip. Annealing responses at room temperature have been reported.**

***Index Terms*—Sub-threshold logic; Near-threshold operation; Variability; Modeling**

I. Introduction

Ferroelectric Random Access Memories (FRAMs) are one of the non-volatile memory technology featuring short write access time, low power consumption and high read/write endurance [1] [2]. Moreover, they are nowadays identified as an attractive candidate for space and civilian nuclear applications thanks to their ferroelectric materials shown to be highly tolerant to ionizing radiation [3]. Although ferroelectric materials are proved to be very resistant to Total Ionizing Dose (TID) and able to support up to 10 Mrad(Si), FRAM devices have shown a much lower tolerance to TID due mainly to the sensitivity of the peripheral control circuitry [4]. To allow a better understanding of TID effects on different function blocks of the memory chip, studies performed so far develop generally their own FRAM prototypes to have the complete knowledge of the architecture and CMOS process technology [4]–[6]. Some works have investigated the degradation induced by TID on FRAM Commercial Off The Shelf (COTS) [7]–[10]. Knowing that some COTS references have a high radiation hardness level could be of great interest to radiation effects community.

In this work, we present TID experimental results of two references of commercial FRAM devices from two different manufacturers. We report different damage effects on each memory and we determine the most sensitive part (peripheral circuitry or memory cell) responsible of the failure. The annealing response of FRAM devices at room temperature is also analyzed.

II. Ferroelectric RAM technology

FRAM uses a ferroelectric thin film that keeps a remanent polarization after the application of an external electric field. Changing the direction of the electric field inverts the polarization of the ferroelectric material and hence the stored logic state. As a matter of fact, the binary information depends on the charge density of the remanent polarization stored in the equivalent capacitor of the ferroelectric material. FRAMs are built using either 2T/2C or 1T/1C bit cell structures shown in Fig. 1 (a) and (b), respectively. To write a logic value '1' or '0' to a cell, a +Vcc or -Vcc voltage is applied to both electrodes of the ferroelectric capacitor. In read operation, the bit line (BL) is precharged to 0 V,

the word line (WL) is selected and Vcc voltage is applied to the plate line (PL). If the stored bit is '0', the polarization is not reversed but BL is charged up by ΔV_L which is further reduced to 0 V by the sense amplifier connected to the BL. In the case where the cell holds a logic value '1', polarization is reversed causing BL to charge up by ΔV_H which is raised to Vcc by the sense amplifier. Note that after reading a logic value '1', a rewriting operation is performed to restore the data as the reversal of polarity destroys the initial value and creates a '0' data state.

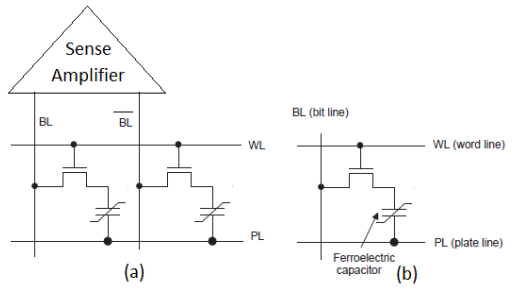

Fig. 1: Structure of 2T/2C (a) and 1T/1C (b) cells.

III. Experimental Setting

Two commercial FRAM chips from two different manufacturers were irradiated with a Co-60 γ ray source. Table I summarizes the main characteristics of Devices Under Test (DUTs). The ferroelectric materials of the two tested devices is lead Zirconate-titanate (PZT). Based on [11], we deduce that Fujitsu FRAM is built using 1T/1C structure, while the architecture of the Cypress semiconductor FRAM is probably 2T/2C.

The irradiation was performed with the SynergyHealth facility in Marseille [12]. The dose rate was fixed to 3.5 rad/s. Radiation dosimetry was performed using Harwell Red 4034 dosimeters placed on the test board. These dosimeters are made from radiation-sensitive poly-methylmethacrylate (PMMA) which darken when irradiated. Before irradiation, the DUTs were initialized with the following test pattern (0xAA, 0x55, 0x00, 0xFF, 0xCC, 0xFF, 0x33, 0x66, 0x99) written at consecutive addresses. During the test, half of the memory cells were kept in read only mode to verify retention problems whereas the other half were exercised with read/write cycles for each measurement. Let *ErBit-RD* be the bit error rate associated to the read only part. For the read/write mode, the test methodology is as follows :

a- Read and verify the data, let *ErBit-WR/RD* be the bit error rate associated
b- Refresh by writing initial test pattern
c- Read and verify the data, let *ErBit-reffresh* be the bit error rate associated
d- Write the complement of read data
e- Read and verify the data, let *ErBit-complement* be the bit error rate associated
f- Write initial test pattern
g- Repeat **a** to **f** for each radiation step

A software was developed to write, read and verify the data in the memories via the Serial Peripheral Interface (SPI) bus. The SPI frequency was fixed to 1 MHz for all DUTs. Standby and operating read currents were periodically measured as a function of total ionizing dose. Note that functional control and current measurements were carried out during irradiation of the DUTs.

IV. Test results and discussion

Total ionizing dose testing has shown very different results between FRAM references. Fig. 2 and Fig. 3 show the percentage of bit errors in the memory chips as a function of the deposited dose for FRAM-1 and FRAM-2, respectively. The reference FRAM-1 has maintained the complete functionality up to 200 krad, while radiation hardness level of FRAM-2 is 17 krad. This huge difference can be explained either by the use of different CMOS technology process for the implementation of the peripheral CMOS circuitries (sense amplifier, decoders...) and the nMOS transistors of the memory cell [13] or by the use of different bit cells architectures (1T/1C vs 2T/2C) .

All read data were stucked at zero at 300 krad for FRAM-1 and at 20 krad for FRAM-2. As half of the theoretical test pattern bits are at logic value '0' and the other half at logic value '1', the bit errors (*ErBit-RD*, *ErBit-WR/RD* and *ErBit-reffresh*) have a maximum value of 50%. However, trying to write the complement of read data reveals the stuck-at faults problem. Actually, the bit errors in the read only part of the memory expose retention problem

TABLE I: Characteristics of DUTs.

	Capacity (kB)	F_{Max} (MHz)	Technology Node (nm)	Part Number	Manufacturer
FRAM-1	512	40	130	CY15B104Q semiconductor	Cypress
FRAM-2	512	108	180	MB85RQ4MLPF	Fujitsu

while the bit errors in the write/read part can be due to either stuck-at problem where we can not change the value of bits or also retention problem being accelerated by the total ionizing dose effects.

The results of FRAM-2 show a sudden functional failure where all read data are stucked-at zero. This failure is most probably due to a problem at the peripheral CMOS circuitries shared by all memory bit cells, such as control or I/O circuitries.

On the other hand, FRAM-1 shows an increase on the number of erroneous bits as the deposited dose increases. This can be assigned either to a damage on the peripheral circuitries including row decoder, column decoder, sense amplifier or plate line selectors, where clusters of bit errors are expected, or to a failure problem at the memory cell. Actually, memory cell degradation can be ascribed to one of the following problems :

- Fatigue-like or/and imprint-like phenomena affecting the remanent polarization (PR+, PR-) of the ferroelectric capacitor under irradiations. The fatigue-like phenomenon induces a decrease in the hysteresis loop width due to the charge trapping in the ferroelectric volume while the imprint-like phenomenon results in a shift in the hysteresis loop from the right to the left or from the left to the right depending on the pre-poled state of the capacitor, as shown in Fig. 4 [14]. These shifts influence the charge density of the remanent polarization becoming very close and can not be distinguished any more.
- Radiation-induced damage on the NMOS pass transistor which results in the increase of leakage current flowing from the bit line to the plate line, even if the memory cell is not selected. First, this may induce a voltage drop on the ferroelectric capacitor affecting the original polarization state. And second, when the NMOS transistor is open, the output voltage at the bit line may decrease drastically resulting in stuck at '0' error.

The data collected from the test of FRAM-1 show that erroneous bits belong to different words, which dismiss an address error problem. Moreover, the first observed errors for FRAM-1 appear when trying to write the complement of read data, namely we had failed to change the value of some bits initially

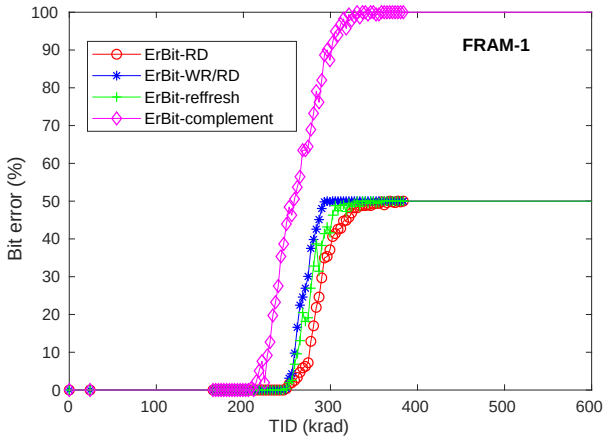

Fig. 2: Bit error versus deposited dose for FRAM-1.

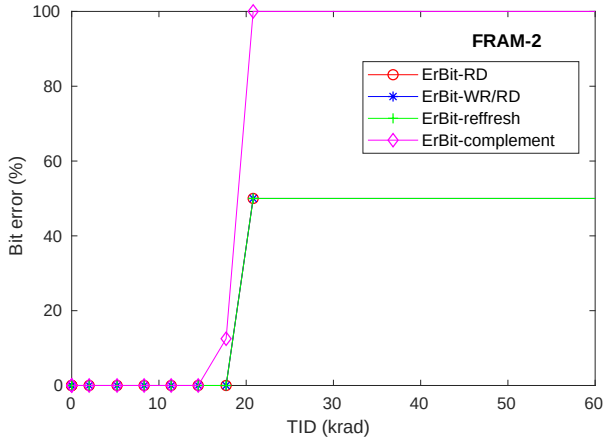

Fig. 3: Bit error versus deposited dose for FRAM-2.

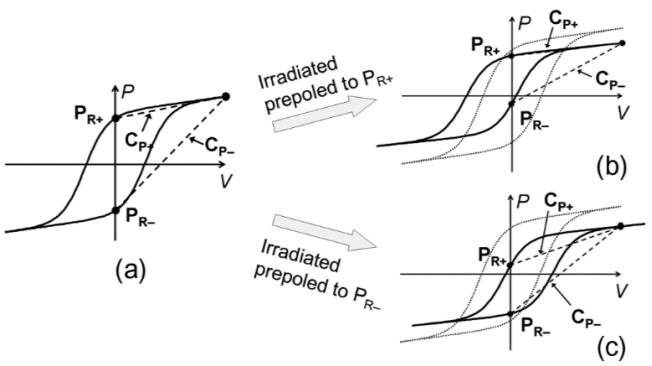

Fig. 4: Radiation effects on the hysteresis loop (a) fresh ferroelectric hysteresis loop (b) shift to the left of the hysteresis loop after irradiation of a capacitor pre-poled to PR+ (solid = irradiated , dotted = fresh) (c) shift to the right of the hysteresis loop after irradiation of a capacitor pre-poled to PR- (solid = irradiated, dotted= fresh).

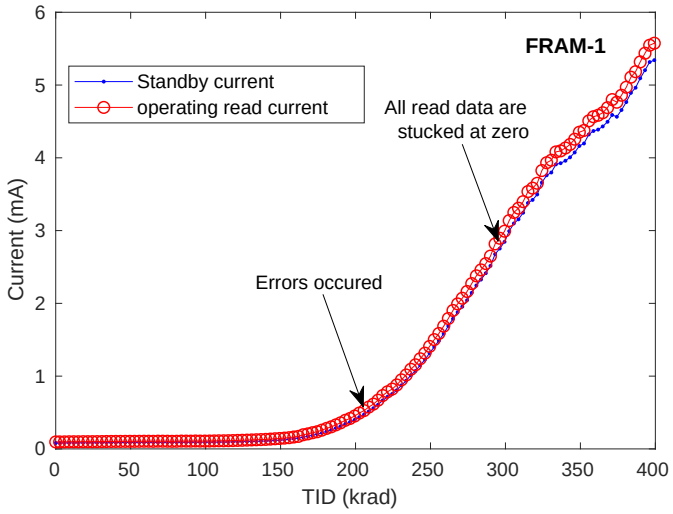

Fig. 5: TID effects on dynamic and standby currents of FRAM-1.

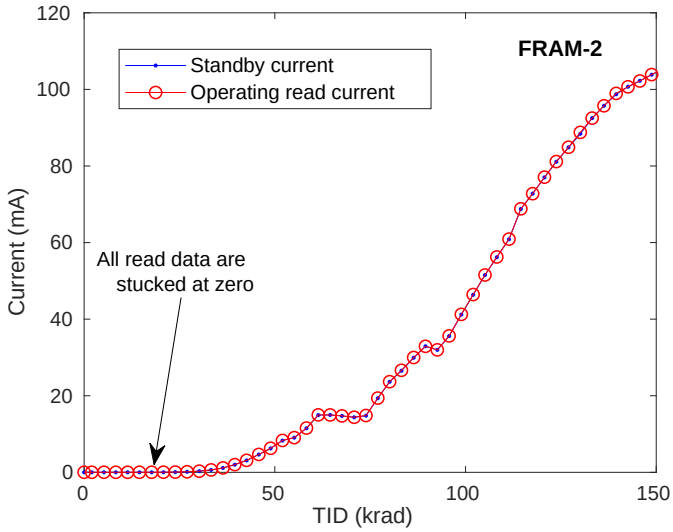

Fig. 6: TID effects on dynamic and standby currents of FRAM-2.

programmed at the logic value '0' to the logic value '1'. This suggests first a correlation between the initial programmed value and the stuck-at error and second that bits initially programmed at the logic value '0' are more sensitive to ionizing radiation. This behavior can be explained by the photo induced fatigue-like of the ferroelectric material which reduces the hysteresis loop of ferroelectric capacitor, as explained previously. However, we do not exclude the scenario of a reading problem due to the leakage current increase in the NMOS pass transistor, as current measurements show that the increase of leakage current is followed by the presence of bit errors.

Note that almost the same results of FRAM-1 were observed in [5], where the tested device was a 1MB parallel FRAM fabricated with a 130 nm CMOS process. This device, as ours, was operational up to 200 krad and all read data were stuck at zero at $\sim$300 krad. However, the standby current of FRAM-1 was 6 times smaller, which can be explained by the use of lower dose rate in our case.

Fig. 5 and Fig. 6 show TID effects on dynamic and standby currents of the studied FRAMs. Before irradiation, FRAM-2 has the lowest standby current in the order of 70 μA. This current had rapidly increased with the deposited dose. When it reached 16 times its initial value ($\approx$1 mA), the corresponding memory failed to read data. Like FRAM-2, the supply current of FRAM-1 had steadily increased but with much smaller increments. Errors started to occur when the current reached 1.3 mA and the data bits were all stucked-at 0 at a supply current of 4.5 mA. For both FRAM-1 and FRAM-2, the operating read current follows the trend of standby current which is explained by the fact that TID increases mainly leakage currents.

Annealing tests were performed at room temperature. The results show no significant annealing effect on FRAM-2. Although its leakage current

has drastically decreased (68 mA after 3 days of annealing and 5 mA after 1 month of annealing versus 100 mA at the end of irradiation), all read data bits were still stucked-at zero. On the other hand, FRAM-1 has undergo a gradual annealing where its leakage current has regained a small value (1 mA after 3 days of annealing and 0.33 mA after 1 month of annealing) and all data bits were correctly written/read just after 3 days of annealing.

V. Conclusion

We investigate TID effects on FRAM COTS under Co-60 γ radiation. Functional failure and current measurements have been carried out constantly during irradiation. The analysis of the failure rate as a function of the deposited dose has allowed to know the most sensitive part of the memory chip (peripheral circuitry or memory cell). The results of the studied memories were very different due certainly to different architecture and different CMOS technology. Experimental results have shown a good hardness radiation level of one of the studied references that maintained a complete functionality up to 200 krad. The annealing tests at room temperature have shown a complete recovery of this reference just after 3 days.

Acknowledgments.

The authors would like to thank ERMES company for the financial support given to this work.

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