Recent advances in GaN power devices development at CEA-LETI

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Recent Advances in GaN Power Devices Development at CEA-LETI

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***Abstract*— In this paper we present recent results obtained on GaN Power devices at CEA-LETI. In a first part, we will discuss the benefits of AlGaN/GaN MOS channel High Electron Mobility Transistors (MOSc HEMTs) with fully recessed gate architecture on 200mm Si substrates with respect to their pGaN HEMT counterparts for 650V applications, especially in terms of On-state resistance Ron, gate leakage and temperature dependency. In the second part, we will discuss the gain expected from vertical device architectures on GaN.**

I. Introduction

GaN-on-Si High Electron Mobility Transistors (HEMTs) are considered as one of the major solutions to address medium power applications in the 650V range [1]. Among the different device architectures that benefit from the high conduction properties of the two-dimensional electron gas (2DEG), induced by the presence of the AlGaN/GaN heterojunction, those with **normally-off behaviors** are desired to simplify device driver design [1]. Two main device architectures enabling normally-off behavior are of major interest today: **pGaN-gate** technology and **insulated-gate** technology [1]. Despite its manufacturing maturity and market availability [2], pGaN-gate transistors are still suffering from a limited gate endurance to overvoltage. Indeed, during commutation in standard power converter topologies, circuit instabilities lead to gate voltage overshoot phenomena compromising normal transistor functionality. In addition, other needs concerning power devices are related to addressing higher blocking voltages (BV), typically 1200V or above. A **vertical structure** is an efficient way to increase the breakdown voltage and allows higher current density with respect to a lateral architecture. Due to the difficulty of controlling the high electric field located near the surface, lateral devices typically take up an order of magnitude more surface area than their vertical counterparts [3].

II. 650V MOS-channel HEMT devices

A. Technology and device fabrication

In **Fig. 1** we show a schematic of the MOS-channel HEMT device structure [4]. The GaN stack is grown by metalorganic chemical vapor deposition (MOCVD) on 200 mm Si wafers: The reference epitaxial stack includes a transition layer followed by a thick C doped GaN (GaN:C > 1µm). An unintentionally doped GaN layer (GaN:UID), followed by the AlGaN barrier, is grown to form the channel : a 2DEG is formed at the AlGaN/GaN interface.

The insulated MIS-gate stack is fabricated via full etching of the AlGaN barrier, followed by Atomic Layer Deposition (ALD) of an Al_2O_3 oxide, gate-metal deposition and patterning. Field plate architectures are also embedded to smooth the electrical field between gate and drain in the blocking regime. Finally, source and drain ohmic contacts are formed using a Ti/Al stack followed by annealing.

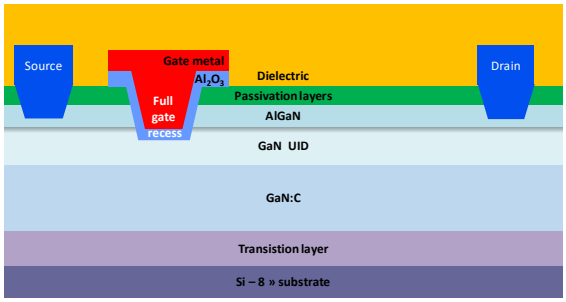

Fig. 1 Schematic cross-section of the CEA-LETI GaN-on-Si fully recessed-gate MOS-channel HEMT architecture for 650V applications.

B. MOS-channel HEMT device results

Fig. 2 shows an example of $I_D(V_G)$ characteristics at room temperature with excellent performance: V_{th}=+1V, SS=88mV/dec. These curves illustrate the intrinsic gain of this architecture with respect to pGaN gate: gate current is very low (I_D/I_G >8 decades in **Fig. 1**, versus ~3 decades for pGaN [5]). The extracted low field mobility µ = 225 cm²/V/s outperforms most published MOS channel HEMT results (see review [1]). Note that MOSc HEMT technology is capable of supporting high Vg, such as 20V (not shown here), which outperforms pGaN. **Fig. 3** illustrates the linear Ron as a function of gate length L_G and gate-to-drain distance L_{GD} from 25°C to 150°C. The 2DEG resistance is the main contributor to the total Ron, and shows the largest temperature dependency. **Fig. 4** shows the ratio of Ron variation with temperature Ron(T)/Ron(25°C) for two L_{GD} values and a comparison with pGaN data from [5].

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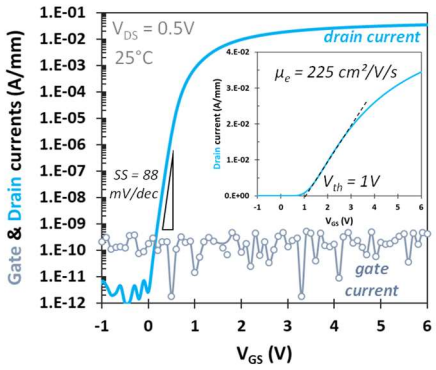


Fig. 2 Measured drain current and gate leakage (I_D, I_G) as function of gate voltage V_{GS}, in log scale (Inset: linear scale for I_D) – $L_{g,eff}$=0.29µm.

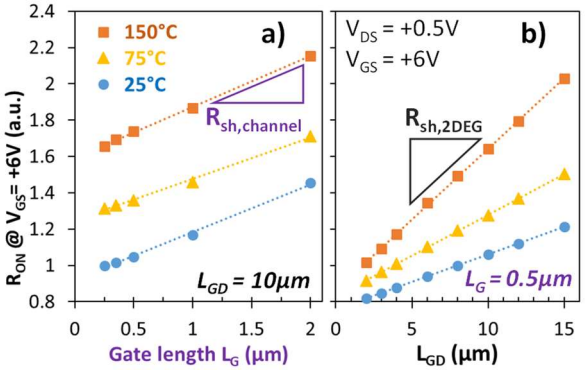


Fig. 3 Impact of L_G and L_{GD} on the on-state resistance Ron at different temperatures.

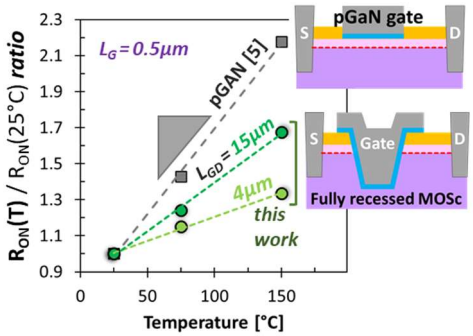


Fig. 4 Ron ratio (increase) with temperature.

III. VERTICAL GAN DEVICES DEVELOPMENT

Vertical GaN devices in principle allow the Ron.A/BV (Ron.A: specific resistance in mOhm.cm²) factor of merit to be reduced with respect to lateral devices. Until now, the best results according to this metric have been obtained using native GaN substrates [6]. One key point is understanding the root cause of device off-state leakage. Experimental leakage current measured on vertical GaN-on-Si Schottky diodes (**Fig. 5**) have been compared to TCAD simulations (**Fig. 6**). The current is explained by a combination of several physical mechanisms with Poole-Frenkel emission being dominant at high temperature and high voltages. A possible origin for the discrepancy with TCAD at lower temperatures could be defects either due to etching of GaN and/or related to the fluorine implant [7].

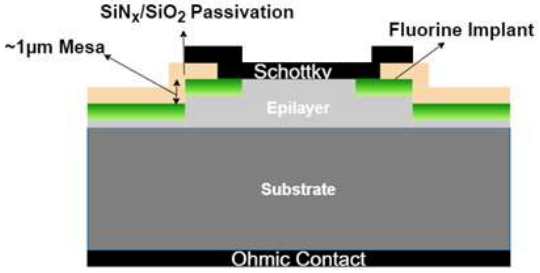
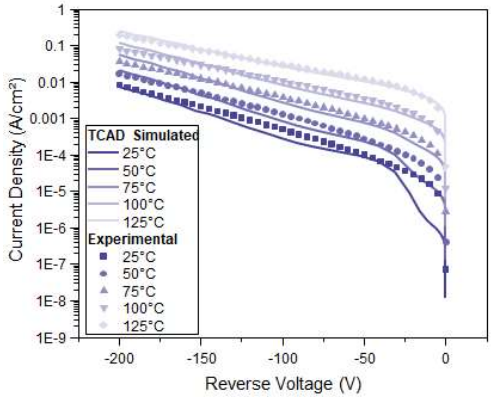


Fig. 5 Device cross-section with 5µm GaN epitaxy layer grown on 2-inch substrate (Schottky contact is Pt capped with Au) [7]

Model	Width/ Region	Trap Energy (eV)	Type	Concentration
Trap Assisted Tunneling	10 nm	Ec – 0.25	Donor	1.0E15cm^{-3}
Poole Frenkel Emission	GaN	Ec – 0.9	Donor	1.0E15cm^{-3}



$$J_{Total,Leakage} = J_T + J_{BL} + J_{TAT} + J_{PF}$$

(J_T = Thermionic, J_{BL} = Schotky Barrier Lowering, J_{TAT} = Trap assisted tunnelling, J_{PF} = Poole Frenkel)

Fig. 6 : (top) Traps characteristics; (bottom) Experimental (dots) and simulated (lines) currents for vertical GaN-on-GaN Schottky diode. [7]

IV. CONCLUSION

Fully recessed insulated-gate normally-off GaN MOS-channel HEMTs have been successfully fabricated on 200mm Si-wafers with a fully CMOS compatible Au-free process for 650V applications. Typical devices show strongly reduced gate current and a lower temperature coefficient of Ron with respect to pGaN. For the future higher voltage applications, strong Ron/BV gain is expected from vertical GaN devices with the requirement of a good control of conducting defects in order to limit reverse leakage.

REFERENCES

[1] F.Roccaforte *et al.*, "An Overview of Normally-Off GaN-Based High Electron Mobility Transistors", *Materials* **2019**, *12*, 1599; doi: 10.3390/ma12101599
[2] https://www.infineon.com/cms/en/product/power/wide-band-gap-semiconductors- sic-gan/gallium-nitride-gan/
[3] R. Gaska et al, 2013, IEEE Energytech
[4] A. G. Viey et al., "Investigation of nBTI degradation on GaN-on-Si E-mode MOSc-HEMT," IEDM 2019
[5] IGT60R070D1 data sheet: 600V CoolGaN™ enhancement-mode Power Transistor, 2020-05-29.
[6] H. Fu et al., IEEE TED, Vol. 68, No. 7, July 2021
[7] V. Maurya et al., IMAPS, Tours, November 2021