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### ► To cite this version:

Victor Hui, Agathe André, Alexandre Arnoult, P Besson, Christophe Dubarry, et al.. Transfer of AlGaAs/GaAs crystalline Bragg mirror from a GaAs substrate to a fused silica substrate by direct bonding. SPIE Photonics Europe, Apr 2022, Strasbourg, France. cea-03735678

**HAL Id: cea-03735678**

**<https://cea.hal.science/cea-03735678>**

Submitted on 5 Aug 2022

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# Transfer of AlGaAs/GaAs crystalline Bragg mirror from a GaAs substrate to a fused silica substrate by direct bonding

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## ABSTRACT

Direct bonding has been a major key technology in many fields nowadays. From microelectronic to optoelectronic technologies, it became a technique used for mass production technology in many different applications. Direct bonding of silicon or silicon dioxide is now a well known process. In this article, we explore this technology through the transfer of III-V *AlGaAs/GaAs* crystalline multilayer from its native *GaAs* substrate upon a fused silica substrate (*SiO<sub>2</sub>*). The goal of this work is to explore the conception of crystalline Bragg mirrors with low mechanical loss and high optical quality for precision measurement applications.

We present the main results obtained for each step of the transfer process. Various experiment such as AFM characterization have been performed on the wafers to probe surface quality. Chemical wet etching with different experimental conditions have been tested to remove the *GaAs* substrate. We discuss the main challenges of the process, especially the bonding of two rather different materials from the thermo-mechanic point of view. Focus is also made on the chemistry used in the wet etching part to have a selective etching between *GaAs* and *AlGaAs*.

**Keywords:** III-V, Direct Bonding, Surface pretreatment, Selective wet etching, Native oxide, AFM

## 1. INTRODUCTION

Today's most developed technologies used to study space-time metrology such as optical atomic clocks or interferometric gravitational wave detectors are encountering the boundaries set by thermally induced process. Indeed, such instruments are based on optical interferometry involving highly reflective mirrors that are affected by thermally driven fluctuations. It results in phase shift of the laser beam and thus thermal noise.<sup>1</sup> Minimizing this effect is crucial to enhance the sensitivity of these optical instruments.

The main impediment to overcome in order to achieve enhanced performance is the Brownian noise driven by the Brownian motion of the cavity's multilayer coating.<sup>2,3</sup> The fluctuation-dissipation theorem asserts that the position of any mechanical system, affected by an energy dissipation process is subject to a fluctuation directly related to its thermodynamic temperature. Applying that theorem to the Brownian process leads to the fact that this motion directly depends on intrinsic characteristics of the coating's materials such as mechanical damping.

Until now the best performances for accurate phase changes of a probe laser beam are achieved by highly reflective coatings on transparent substrates. Materials used involves *SiO<sub>2</sub>/Ta<sub>2</sub>O<sub>5</sub>* multilayers deposited by ion beam sputtering (IBS) on *SiO<sub>2</sub>* substrate. With latest improvement of optical cavity sensitivities, coatings made of these materials presents mechanical damping that results in largely limiting thermal noise level. In order to lower the thermal noise barrier, focus has been made on other types of materials used for the conception of such multilayer coatings.

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Exploring monocrystalline *AlGaAs* heterostructures happens to be a very interesting option, for this material has both excellent optical properties and very low mechanical damping, thus low thermal noise level.<sup>4,5</sup> It should be noted that high quality optical coatings with low thermal noise are interesting also for other applications (optical clocks,<sup>6</sup> opto-mechanical experiments,<sup>7</sup> VCSELs conception<sup>8</sup> among others). The industry is looking into this type of coatings also for applications in gyrolasers (These devices are used routinely in navigation. They are made with thin layers immersed in a laser plasma that tends to degrade the layers. Crystalline materials have a better resistance to such plasmas).

We present in this context the experimental process developed to realize a Bragg mirror using such crystalline materials. The goal is to transfer epitaxial grown quarterwave layers made of *AlGaAs* and *GaAs* materials from their growth substrate to a fused silica substrate, making an optimized Bragg mirror. The process encounter many challenges on the key technologies involved, mostly because the materials that are used have quite different properties on the mechanical and thermal field.

In the following of the article, we will describe the experimental process that was implemented in section 2. In section 3 we presents the results of AFM characterizations that were performed on the wafers. The results and optical characterization of the transfer are presented in section 4. Finally we discuss prospects for future work in section 5.

## 2. EXPERIMENTAL PROCEDURE

Two types of wafers are used in this study : 580 nm thick *AlGaAs/GaAs* epitaxial layers grown by MBE (molecular beam epitaxy) on 650  $\mu\text{m}$  thick GaAs substrates and 530  $\mu\text{m}$  amorphous *SiO<sub>2</sub>* bulk substrates. The preliminary tests and surface characterizations to validate the process were done on *GaAs* bulk and *SiO<sub>2</sub>* bulk substrates. The epitaxial stack that compose the multilayer is made of one thick 270 nm *GaAs* top layer, 35 pairs of *AlGaAs/GaAs* quarter-wave layers and one 270 nm *AlGaAs* sacrificial layer.

The figure 1 shows the main steps of the fabrication process.

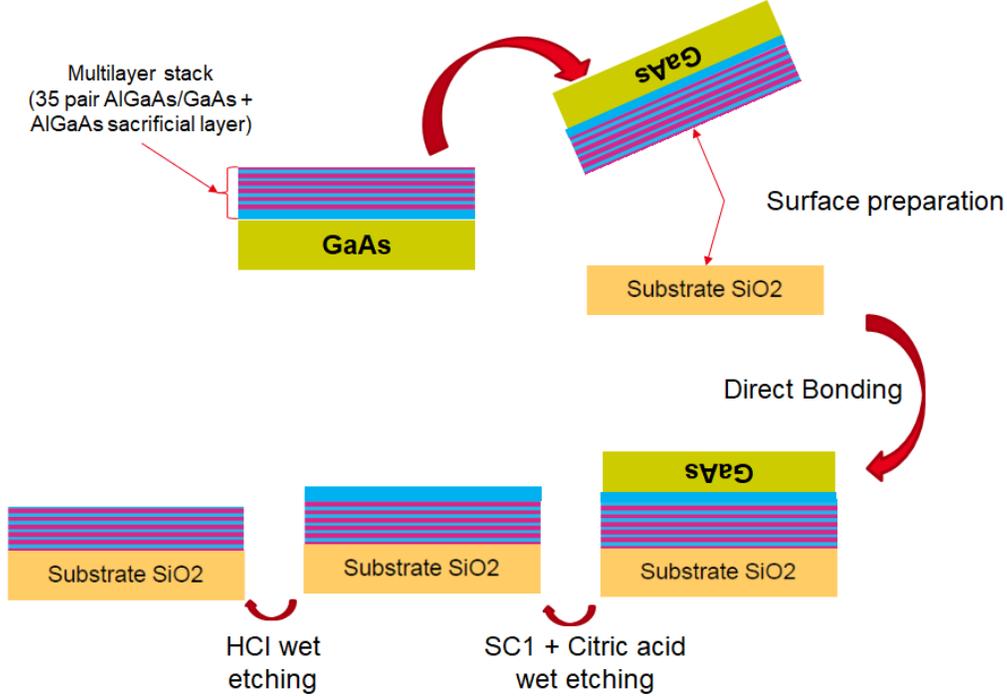


Figure 1. Transfer process of  $AlGaAs/GaAs$  multilayer: 1) Surface preparation with  $NH_4OH$  wet cleaning treatment followed by PECVD deposition of  $SiO_2$ . 2) Surface polishing before room temperature direct bonding. 3) Room temperature wet etching with SC1 ( $NH_4OH/H_2O_2/DIWater$ ) to remove the majority of  $GaAs$  substrate (50  $\mu m$  thick  $GaAs$  bulk left) and Citric Acid/ $H_2O_2$  to remove the  $GaAs$  left selectively regarding  $AlGaAs$  sacrificial layer. 4) Final  $HCl$  wet etching to remove selectively  $AlGaAs$  sacrificial layer and claim transferred multilayer on  $SiO_2$  substrate

First step is wet cleaning on the multilayer surface which was performed using  $NH_4OH$  solution.

Immediately after that step, wafers are carried into a PECVD equipment. Then samples were treated with 500 nm  $SiO_2$  PECVD deposit without air exposure.

The impact surface polishing on  $GaAs$  surfaces are studied using surface analyses such as atomic force microscopy (AFM) in section 3.

Once the oxide deposit is done on the multilayers, wafers are annealed during 2 hours at  $450^\circ C$  to reinforce the bonds at the interface between the  $GaAs$  surface and the 500 nm layer of  $SiO_2$ .

To be able to bond, the wafer surfaces need to show low roughness. AFM measurements showed that bulk  $SiO_2$  wafers and the  $SiO_2$  deposit have high values of roughness and need to be corrected to be able to perform direct bonding (see section 3). To correct roughness on the surfaces, the wafers went through a chemico-mechanical polishing (CMP). The polishing removed a 300 nm thick layer off bulk  $SiO_2$  wafers and 200 nm thick layer of the  $SiO_2$  deposit on the  $AlGaAs/GaAs$  multilayer.

Direct bonding is then performed simply by pressing the wafers together. Studies of standard bonds between silicon wafers<sup>9</sup> have shown that the origin of these spontaneous bonds comes from Van der Waals forces and forces associated with hydrogen bonds as well as capillary bridges for bonds that involve hydrophilic surfaces.<sup>10</sup>

After direct bonding, bonded wafers usually undergo an annealing treatment to strengthen the interface bonds. The first validation tests showed that due to the difference of thermal coefficient of thermal expansion (CTE) between  $GaAs$  and  $SiO_2$ , the wafers break after low temperature annealing ( $100^\circ C$ ).<sup>11</sup> Indeed,  $GaAs$  CTE value is  $CTE_{GaAs} = 6.10^{-6} K^{-1}$  whereas  $SiO_2$  has a CTE of  $CTE_{SiO_2} = 5.10^{-7} K^{-1}$ . It means that the CTE difference is of one decade between the two materials. So  $GaAs$  wafers will expand 10 times more than

$SiO_2$  wafers under annealing, leading to mechanical stress at the bonding interface. As a consequence, there are no post-bonding annealing.

The final step is the removal of the GaAs substrate through chemical wet etching. This step was done with three different solutions : First one is SC1 (Standard Cleaning 1), which is  $NH_4OH/H_2O_2/DIwater$  in 1/2/8 proportions. This solution is meant to etch *GaAs* with a relatively quick etch rate (1.6 $\mu$ m/min). Unfortunately, tests showed<sup>11</sup> that this solution is not selective between *GaAs* and the *AlGaAs* sacrificial layer that protects the crystalline multilayer. A second solution is then used, Citric acid/ $H_2O_2$  which is selective between *GaAs* etching and *AlGaAs* etching and thus etches *GaAs* without consuming the *AlGaAs* stop layer. Finally, to remove the sacrificial layer, *HCl* solution diluted at 10% is used to etch *AlGaAs* and stop on the first *GaAs* layer of the multilayer.

### 3. SURFACE CHARACTERIZATIONS

#### 3.1 Impact of chemico-mechanical polishing on *GaAs* and $SiO_2$ surfaces

In order to be suitable to direct bonding, wafers must have low roughness surface. Indeed, since Van der Waals bonds have a very limited range, the bonding surfaces must be separated by a few nanometers. This is only possible if the surfaces are very smooth. This means that the roughness must be less than 0.55 nm RMS to have spontaneous bonding in the case of hydrophilic bonding.<sup>12</sup> To make sure of this, surface flatness need to be characterized.

The surface of *GaAs* and  $SiO_2$  substrates were characterized with the AFM technique. For each measurement, a 10  $\mu$ m x 10  $\mu$ m wide area was probed. RMS roughness and Peak-to-Valley (PV) values of the probed area were obtained . Three areas were explored: in the center of the wafer, at mid-radius and at the edge of the wafer. The results are given in the table of figure 2:

		Reference	After $SiO_2$ PECVD	After CMP
Center	RMS, nm	0.21	0.52	0,21
Mid-radius	RMS, nm	0.24	0.60	0,21
Edge	RMS, nm	0.22	0.58	0,19

Figure 2. AFM measures for *GaAs* reference wafer at the center, mid-radius and edge

Whereas the reference *GaAs* substrates are good to be bonded, it is clearly observed that the roughness after PECVD deposition is much higher than that of the *GaAs* raw substrates. In order to correct that roughness to meet the requirements of direct bonding, it is necessary to perform CMP polishing of the *GaAs* wafers after deposition. One can observe that the RMS roughness values are good for direct bonding.

AFM measurements were also carried on bulk  $SiO_2$  substates. Results are shown in the figure 3.

		Reference	After CMP
Center	RMS, nm	0.88	0.26
Mid-radius	RMS, nm	0.85	0.26
Edge	RMS, nm	0.67	0.28

Figure 3. Comparison of AFM measurements on  $SiO_2$  substrate before and after CMP

Roughness values for reference silica are found to be too high (around 0.8  $\mu$ m RMS) for direct bonding. It can be seen that roughness after CMP is much lower and becomes compatible with the requirements of direct bonding.

These characterizations validate the need of polishing to smooth the surface of the wafers before direct bonding.

## 4. FINAL RESULTS OF THE TRANSFER

### 4.1 Transfer of a doublet

After being validated with bulk *GaAs* and *SiO<sub>2</sub>*, the process was executed first on a simple version of the multi-layer, with a 270 nm *GaAs* layer, only one pair of *AlGaAs*/*GaAs* quarter-wave layers and the 270 nm *AlGaAs* sacrificial layer. This sample is called a "doublet", for there is only one doublet of *AlGaAs*/*GaAs* crystalline layer. After the wet etching of *GaAs* substrate and *AlGaAs* sacrificial layer, ellipsometry characterization was done on the transferred doublet to measure the thickness of each layer composing the stack. Ellipsometry measurements were performed after the citric acid etching to stop on the *AlGaAs* sacrificial layer. The measurements were done on an equipment called Woollam M2000-DI, VASE (Variable Angle Ellipsometry Spectroscopy) whose spectral range is [190-1700 nm]. The results are given in figure 4:

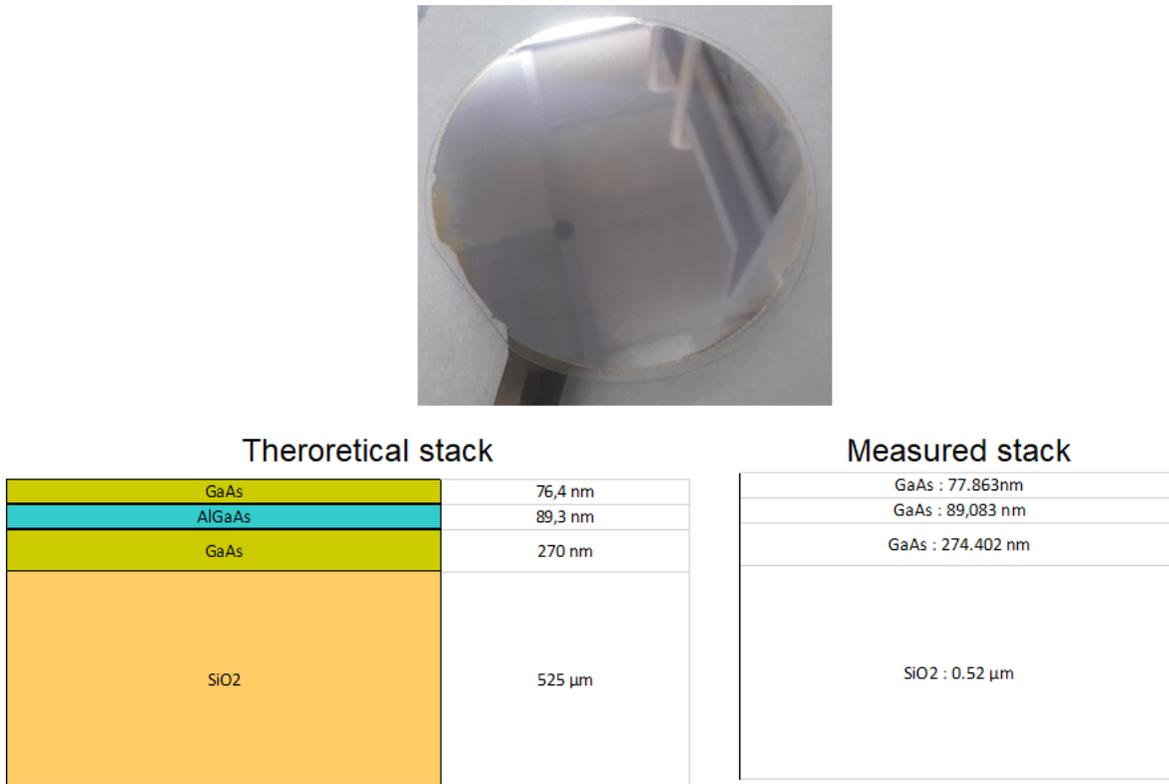


Figure 4. Comparison of stack layers thicknesses after wet etching. The left table gives theoretical thicknesses expected after MBE epitaxial growth. The right table gives the measured thicknesses using ellipsometry

The thickness of the transferred doublet's first *GaAs* layer is very close to the expected thickness. This means that the final etching with *HCl* solution was perfectly selective, etching the *AlGaAs* sacrificial layer without etching the *GaAs* layer.

It is important to note that there are several approximations made on the measurements :

- The optical constants of the materials are calculated theoretically using the electromagnetic formalism. Thus it can impact the relative error on the target thicknesses.

The transfer has been successfully performed on the silica substrate. This validates the transfer process of the doublet from its native *GaAs* substrate to the amorphous silica substrate.

## 4.2 Optical characterizations

Defects detection and optical diffusion measurements were performed on the transferred doublet. The defects detection is done with a interferometric microscope working at  $\lambda = 550 \text{ nm}$  called Micromap550. The diffusion measures are done with a photo-detector that captures the BRDF of the beam which is reflected by the wafer coming from a 1064 nm laser. Figure 5 gives the defects map of the doublet.

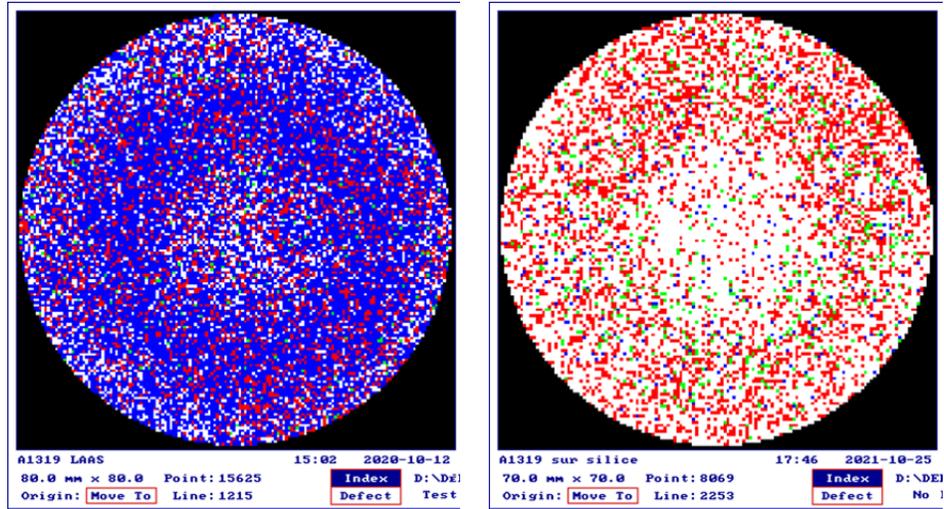


Figure 5. Defect detection on the doublet. Left side gives the defect map of the wafer before transfer (Epitaxial stack on *GaAs* substrate) and right side gives the defect map of the wafer after transfer (Epitaxial stack on *SiO<sub>2</sub>* substrate)

The total number of defects are given by the two numbers (points and line) at the bottom of the figures.

Before the transfer of the doublet, there are 15625 small defects and 1215 large defects, giving a total of 16840 defects. Considering the total size of the scanned are (80 mm diameter), the density of defect is 3,4 defects/mm<sup>2</sup>. After the transfer, there are 8069 small defects and 2799 large defects, giving a total of 10838 defects and a defect density of 2,2 defects/mm<sup>2</sup>. Thus, there are much less defects on the other side of the doublet after the transfer which is rather encouraging because it implies better optical performances in particular at the level of the diffusion.

The diffusion level of the transferred doublet is given by figure 6:

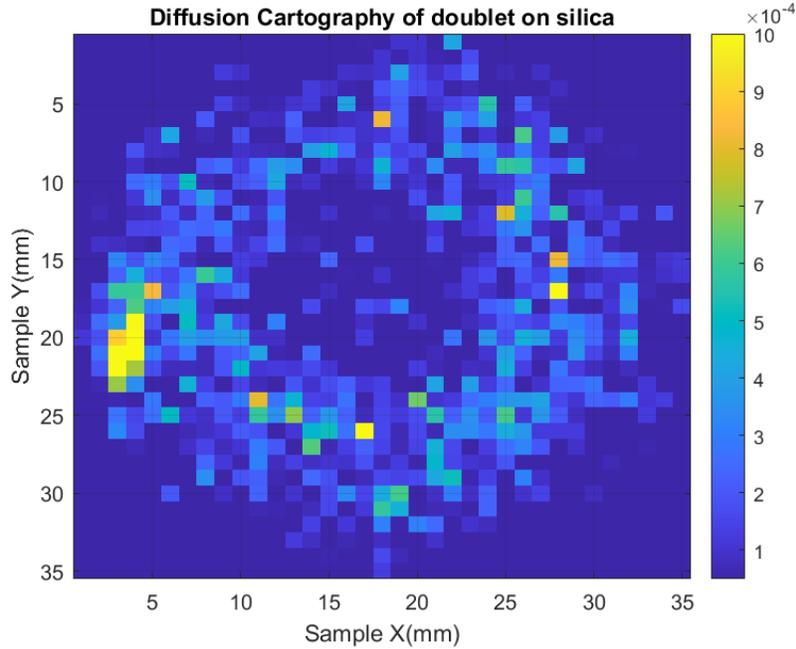


Figure 6. Diffusion map of the transferred doublet

The average diffusion level is 80 ppm. Depending on the application, it may match the specification requirements. For gravitational wave detectors, the mirrors must have very low diffusion levels ( $<10$  ppm) so there are still progress to be made for this application. The pre-transfer measurement was not performed because *GaAs* is partially transparent at the Micromap wavelength (550nm). One would have seen the scattering from the back side of the substrate superimposed on the scattering from the front side, which distorts the measurement. Diffusivity can have several origins: it can be due to defects that appear during the epitaxy because of the crystalline dislocations that multiply at each deposited layer. The diffusion seems less important at the center of the doublet with a corona of points with higher diffusion level than at the center.

This result may come from the temperature difference during the epitaxial growth between the center and the edge of the plate which can cause a concentration of defects in the center of the deposited layers.

### 4.3 Transfer of a multilayer

Eventually, the process was applied to the AlGaAs/GaAs multilayer to transfer the whole epitaxial stack on the  $SiO_2$  substrate. The complete detailed process can be found in Hui's thesis.<sup>11</sup> Results are given by figure 7:

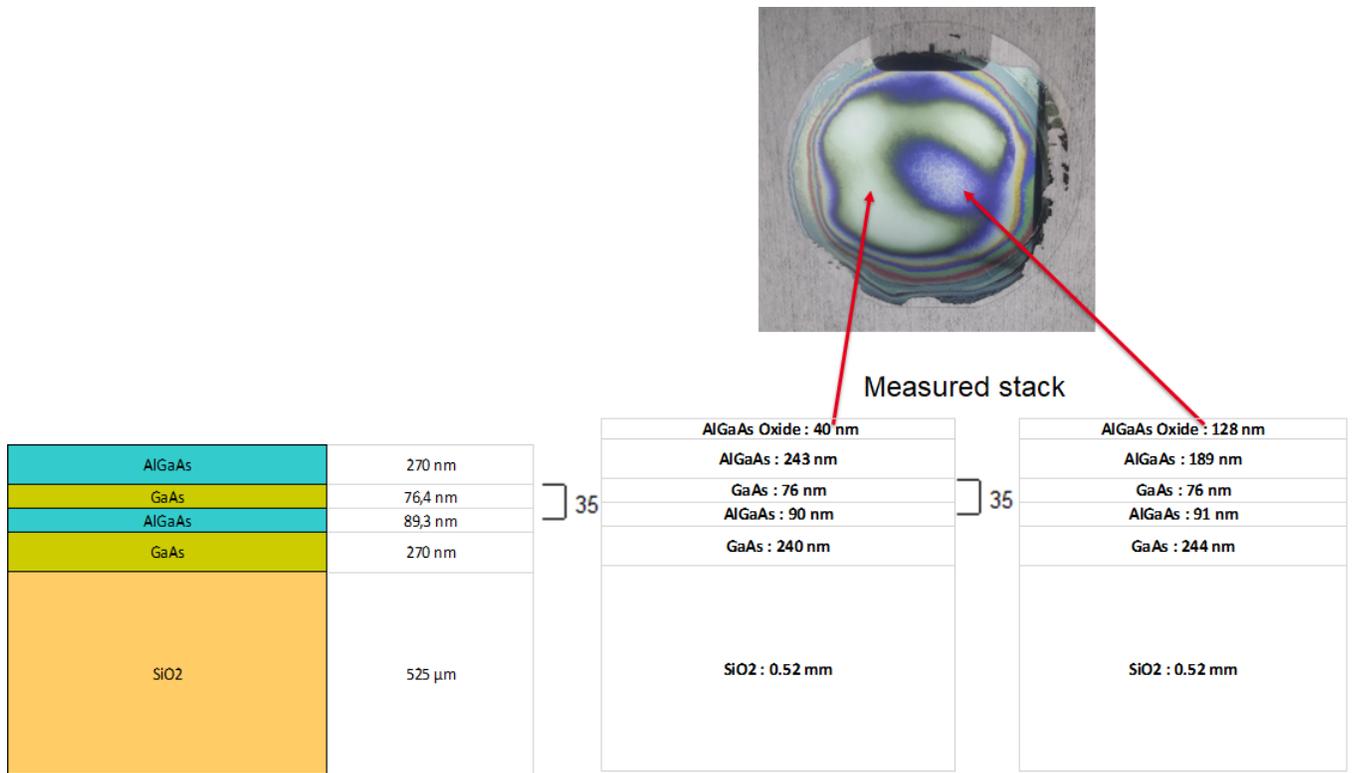


Figure 7. Thickness measurements by ellipsometry of the transferred multilayer stack after citric acid etching. The left table gives the stack's theoretical thicknesses. The table at the center gives the measured thicknesses of the etched wafer in the green zone on the photography. The right table gives the measured thicknesses of the etched wafer in the blue zone on the photography

The photography shows the aspect of the multilayer transferred on the  $SiO_2$  wafer. The different layers of the stack can be seen on the edges of the wafer. It results from the etching step that uncovered the edges of the wafer. Indeed, wet etching process is not completely homogeneous and lateral chemical etching is faster than transverse chemical etching. So edges are etched more deeply than the center of the wafer. Another observation that can be made is the two colors at the center of the wafer. It appears that the *AlGaAs* stop layer was etched deeper in the blue zone than in the green zone, which is confirmed by the measurements. In the blue zone, an 243 nm thick *AlGaAs* stop layer remains whereas in the blue zone, the stop layer's measured thickness is 189 nm. That comes from the in-homogeneous etching of the wafer. However, one can notice that *AlGaAs* are not entirely consumed and that etching with citric acid solution remains selective.

After the last wet etching step using *HCl* solution, the final result of the transfer is given by figure 8:

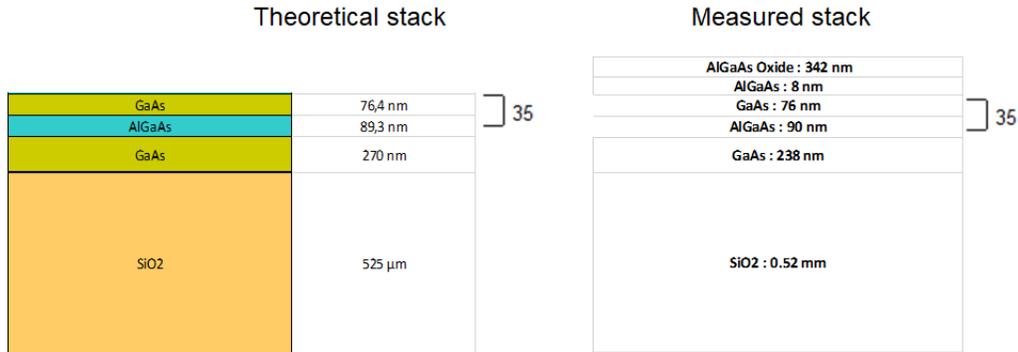
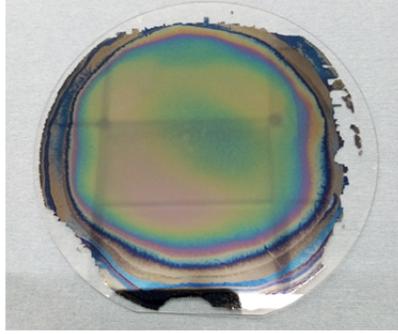


Figure 8. Thickness measurements by ellipsometry of the transferred multilayer stack after final *HCl* etching. The left table gives the stack's theoretical thicknesses. The right table gives the the stack's measured thicknesses

In the end, one can observe that there are still a 342 nm layer of oxidized *AlGaAs* left and a thin 7.7 nm of *AlGaAs* sacrificial layer. These layers can be removed with a second round of *HCl* wet etching to stop on the transferred multilayer.

Since the multilayer has a significant number of layers, ellipsometry can only be an indication and cannot be very precise. One can observe that the oxide layer is very thick. There is no certainty that this layer is an *AlGaAs* oxide. Is is the closest that it can be from an optical point of view. There is a need to confirm this layer composition with other analyses.

## 5. SUMMARY AND FUTURE OUTLOOKS

We have developed, conducted and validated each step of a process flow for the transfer of a crystalline multilayer stack from its native *GaAs* substrate to a *SiO2* substrate giving a Bragg reflector opening the path towards the conception of highly reflective mirrors with both excellent optical performances and low mechanical losses. Surface quality of the wafers was investigated with AFM analyses, exploiting different requirements on the surface quality of the wafers, on the native oxide treatment, on the surface roughness, and the thermo-mechanical differences of the *GaAs* and *SiO2* materials involved. Numerous tests have been conducted to find the right experimental conditions to implement on wafer cleaning, PECVD deposition, direct bonding and *GaAs* substrate removal. In the end we were able to transfer successfully a first sample containing two *GaAs/AlGaAs* thin films on *SiO2* substrate. The characterizations showed better optical performances after the transfer which is encouraging for the future.

One of the main difficulties is the wet etching of the entire 650 μm thick *GaAs* substrate. This implies a very long engraving time which involves several risks:

- lateral infiltration of the chemistry at the bonding interface which degrades the multilayer
- An accentuation of the etching inhomogeneity which leads the chemical solution to consume the wafers edges more quickly than the center.

In order to obtain better results on the transfer of multilayers, several solutions can be considered: First of all, the bonding interface must be strengthened. We cannot perform consolidation annealing after direct bonding of the multilayers to the silica, because of the differences in the thermal expansion coefficient which leads to significant stresses when the temperature rises. At 100°C, the wafers break because the expansion of silica is less important than that of *GaAs*. A first solution is to test if the wafers can be annealed at low temperature, that is, lower than 100°C. Such experiment were conducted to anneal the wafers up to 90°C. It seems that the annealing kinetics is also at stake here. Indeed depending on the temperature rising and falling speed, wafers could have more or less strain at the bonding interface.

Then, to reinforce direct bonding, one can also act on the bonds formed between the adhering surfaces. One solution for this is to perform direct bonding using plasma treatment. A plasma can promote formation of silanol groups ( $Si - OH$ ) on the  $SiO_2$  wafers surfaces. Such a treatment will allow a direct bonding whose bonding energy is much higher than for a simple direct bonding.<sup>13</sup> Another area for improvement concerns chemical etching. We have seen that the chemistry used to etch the last micrometers of *GaAs* (Citric acid/ $H_2O_2$ ) was not sufficiently selective between the *GaAs* substrate and the *AlGaAs* layer covering the multilayer. Since the etching had to last long enough to remove the entire *GaAs* substrate, it eventually affected the *AlGaAs* layer. On the other hand, since edges etching is faster than center etching, the edges of the wafers were being damaged.

We then have two options:

If the grinding track after annealing enhanced bonding works, then we could remove up to 50µm of *GaAs* thickness. We would then be back to the situation with the doublet and we could remove the remaining substrate with the citric acid solution without any problem.

If one were to try to etch the whole substrate, one solution would be to change the sacrificial layer. An InGaP layer seems much more efficient in terms of selectivity of etching chemistry.<sup>14–16</sup> Such a layer could hold the chemical solution long enough for the whole substrate to be etched. One would not have to worry about the problems posed by the etching of the edges, because even if the edges are uncovered faster than the center, the fact of having a layer of *InGaP* which resists to the chemistry protects the multilayer from etching.

## ACKNOWLEDGMENTS

The authors thank T. Philippe, T. Berthet, L. Gabette, R. Souil, C. Lecouvey, J. Dechamp, E. Nolot, D. Despois, C. Di Nardo, and P. Renaud for all the technical assistance and discussions along the work. Special thanks to I. Sagnes for technical discussions on wet etching chemicals. Deep thanks are also adressed to LAAS \* for the MBE crystalline growth of the multilayers and LMA† for optical characterizations.

Work at LAPP is supported by Centre National de la Recherche Scientifique (CNRS). Experimental work were conducted at CEA-leti‡.

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