Key low temperature processes for a silicon-based 3D sequential integration

Xavier Garros, Perrine Batude, Claire Fenouillet-Beranger, Laurent Brunet, Camila Calvacante, Tadeu Mota Frutuoso, Remy Gassilloud, Mickael Ribotta, Laurent Brevard, Valerie Lapras, et al.

Key low temperature processes for a silicon-based 3D sequential integration

X. Garros, P. Batude, C. Fenouillet-Beranger, L. Brunet, C. Cavalcante*, T. Mota Frutuoso, R. Gassilloud, M. Ribotta, L. Brevard, V. Lapras, F. Andrieu, F. Gaillard

CEA, Leti, Minatec Campus, & Grenoble Alpes University

**Now with IMEC*

Outline

- Introduction to 3D sequential integration
- Max thermal budget for the Top Tier
- Key process steps for a low temperature high performance 3DSi CMOS integration
  - Gate oxide
  - Junction engineering
  - Other processes required for RF applications
- Conclusion

Outline

- Introduction to 3D sequential integration
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- Key process steps for a low temperature high performance 3DSi CMOS integration
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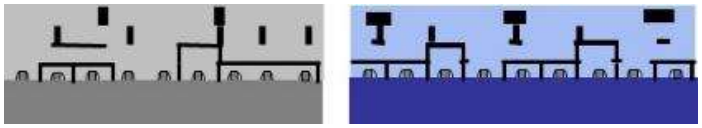
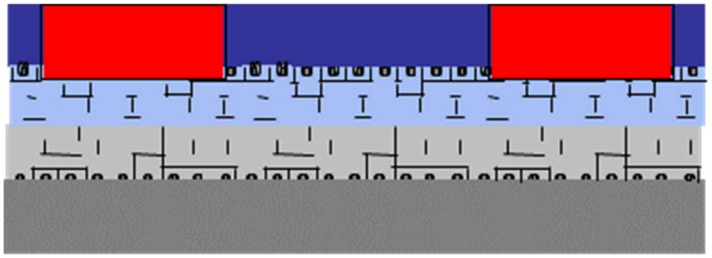
3D parallel integration ≠ 3D sequential integration

Parallel integration (e.g: TSV, Hybrid bonding, Cu pillar, etc..)

1/ Wafers processed separately (in parallel)



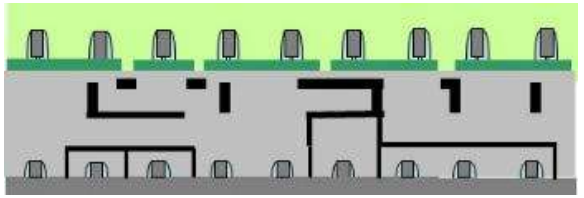
2/ Stacking and contacting



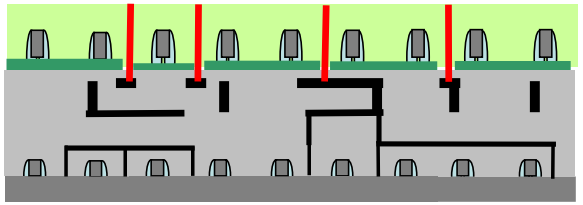
Sequential integration

1/ Bottom Layer process

2/ Top layer process



3/ 3D contact formation

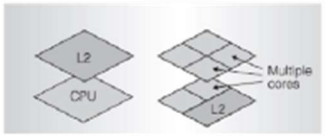
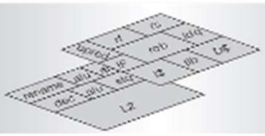
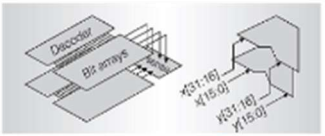
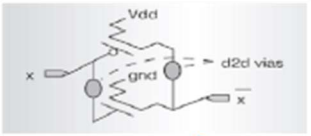


Parallel integration: stacked MOSFETs processed separately
Sequential integration: stacked MOSFETs processed sequentially

3D contact pitch and design granularities

Global Interconnect: 3D parallel

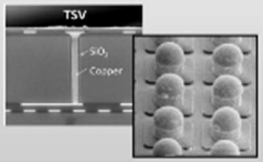
Local Interconnect: 3D sequential

1-Entire core	2-Logic bloc	3-Logic gates	4-Transistors
			
2.5 x10^3 3D plugs / mm^2	100 x10^3 3D plugs / mm^2	5 x10^6 3D plugs / mm^2	100 x10^6 3D plugs / mm^2

Granularity scale

TSV & Cu-Pillar > 10 µm

TSV + Cu-pillar



Ø	10 µm
pitch	20 µm

HD TSV + Direct bonding

Ø	1.7 µm
pitch	3.4 µm

3D Monolithic: 28nm FDSOI CoolCube™ [

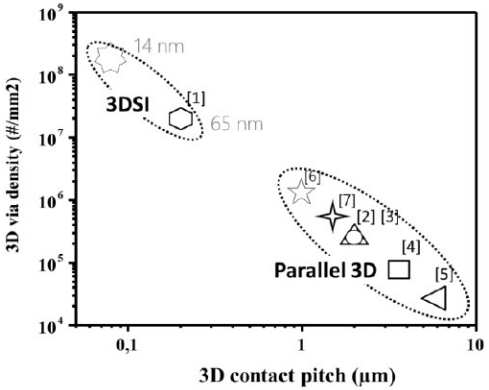
3D monolithic integration

- Very thin active and inter-die layers
- Intermediate BEOL

Ø	0.05 µm
pitch	0.11 µm

MIV=3D-contact
(Monolithic Inter-tier Via)

High 3D contact density:
2x10^7 via/mm^2 demonstrated[1]



3DSi

Pitch ~100nm

Partitioning a circuit in separated stacked levels can be made with different block sizes
3D sequential enables partitioning with all granularities

3DSI applications

High Performance

CMOS over CMOS Wirelength reduction
Boost CMOS (N/P) with alternative channel materials

More Moore

Energy Efficiency

Near memory computing/
In memory computing

Smart Sensors

e.g. miniaturized sensor arrays

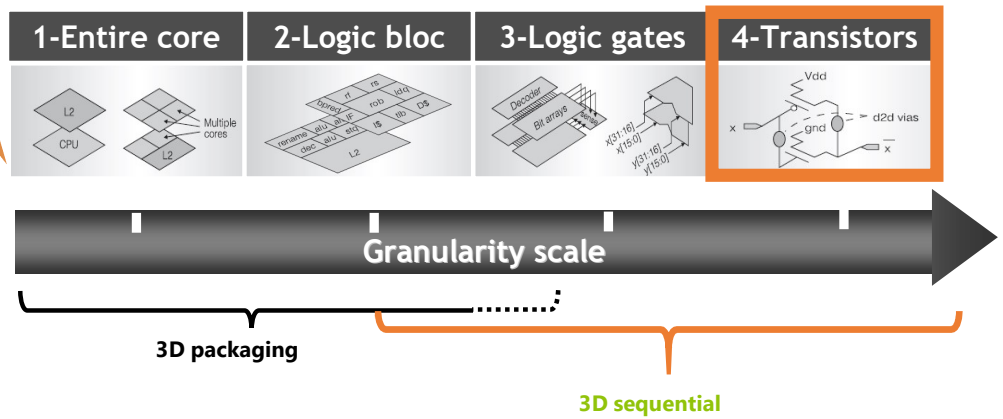
More than Moore

3DSI applications

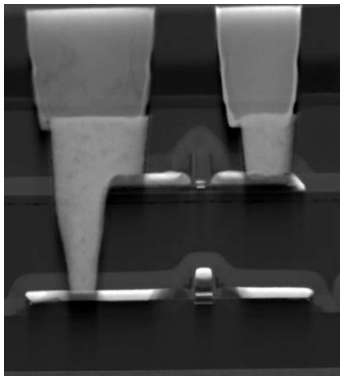
High Performance & Scaling for Computing

CMOS straddled on two stacked channels to address the ultimate pitch

More Moore



Digital/Digital



Mono-Si

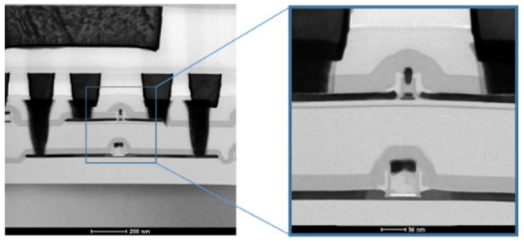
High µ mat. GaAs, Ge

X. Garros et al., IEDM 2019 (Leti)

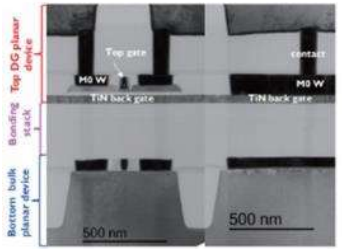
CMOS straddled on two levels

3D Seq→ ultimate performance boost

Mono-Si



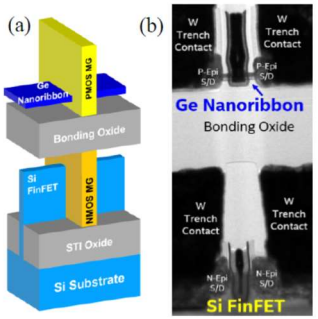
L. Brunet al., VLSI'16 (Leti)



A. Vandooren et al.,VLSI'19 (IMEC)

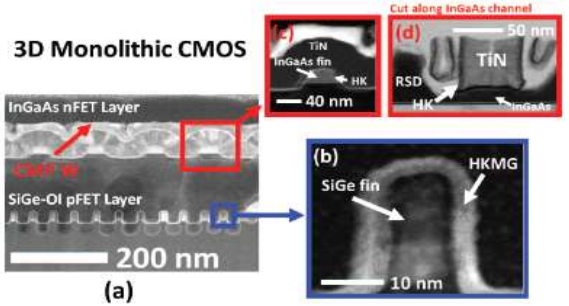
High µ mat. GaAs, Ge

n-Si /p-Ge



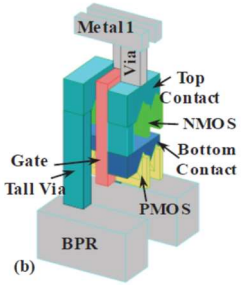
W. Rachmady et al., IEDM'19 (Intel)

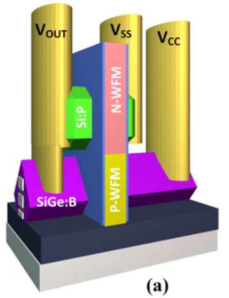
p-Ge /n-III-V



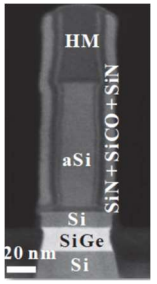
V. Deshpande et al., IEDM'15 (IBM+Leti)

CFET→ Ultimate cell scaling

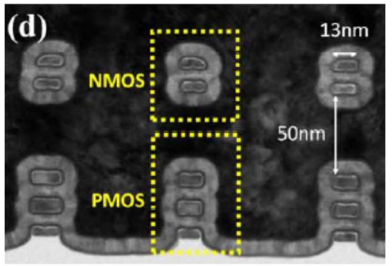




Mono-Si



S. Subramanian et al., VLSI'20 (Imec)



C-Y. Huang et al., IEDM'20 (Intel)

Key argument→Independent transistor's optimization

Simplifying alternative channel co-integration e.g. Ge for pFET & III-V for NFET

Key argument→Highest scalability

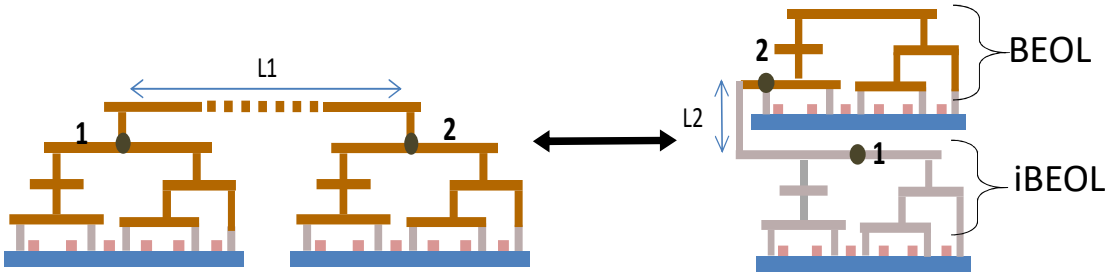
Self aligned bot & top patterning for active and gate

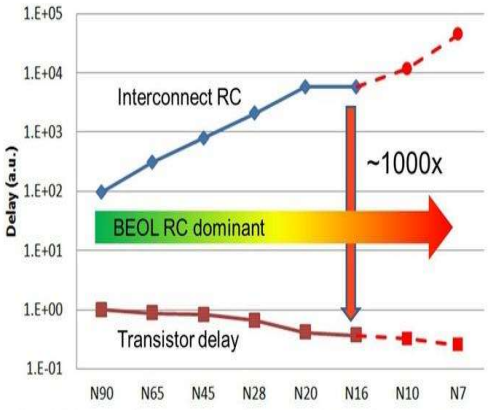
3DSI applications

High Performance for Computing

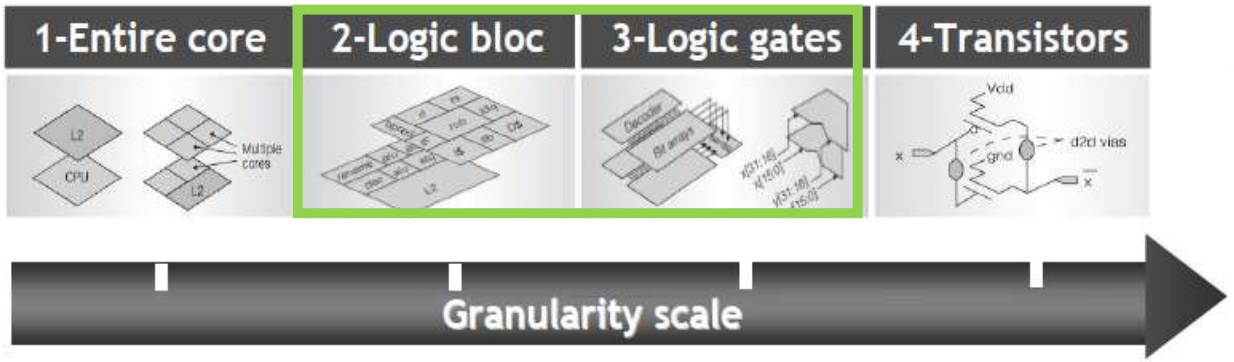
CMOS over CMOS to reduce interconnect delay

More Moore





G. Yeap, IEDM 2013 (Qualcomm)



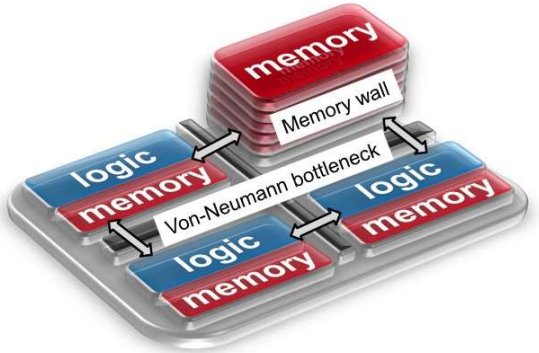
3D sequential applications

More Moore

Energy Efficiency

3D Sequential to solve the Memory Wall

Near memory computing / In memory computing



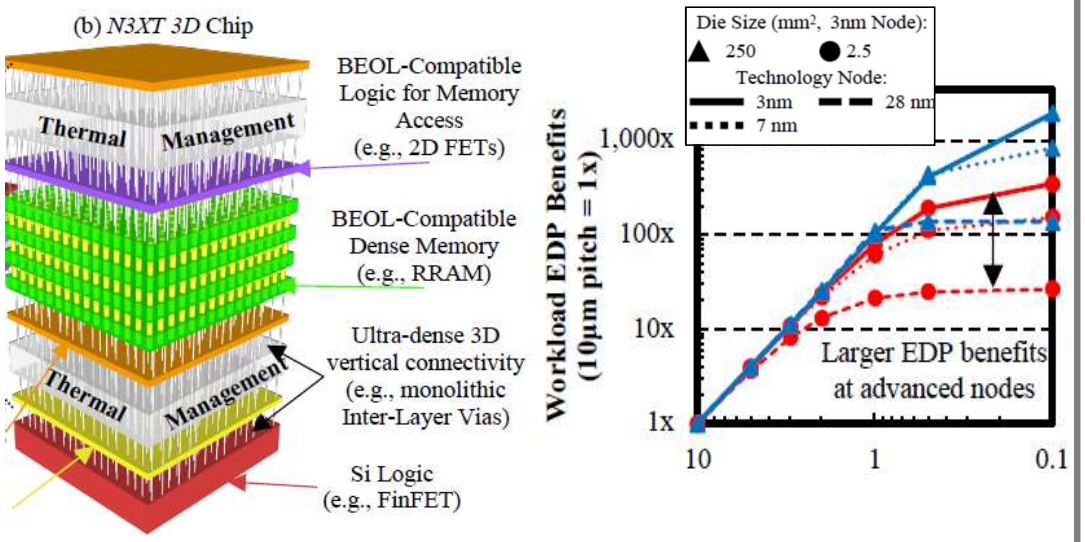
Operation	Energy
Addition of data (fixed point)	1x
Access data (onchip cache)	55x
Access data (offchip DRAM)	3500x

Pedram, IEEE D&T 2016

More than Moore

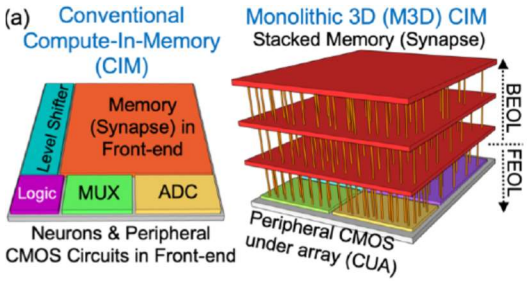
3DSI for Energy Efficient Computing

Near memory Computing
Fine grain memory and logic partitioning

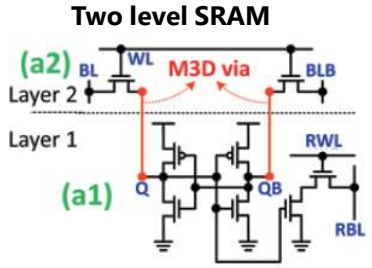


R.M. Radway et al., IEDM'21 (Standford)

In memory Computing

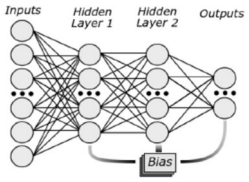


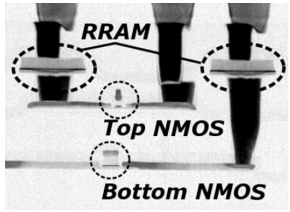
S. Dutta et al., IEDM'20 (ND univ)

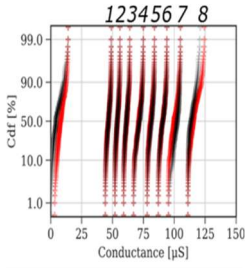


S.Srinivasa et al., VLSI'19 (NDL, TSRI)

Neuromorphic approach







E. Esmanhotto, IEDM'20 (Leti)

3DSI enables fine grain memory and logic partitioning
Energy Delay Product gain increases with more advanced nodes
Requires iBEOL in between layers. Stacked transistors thermal budget~400-500°C

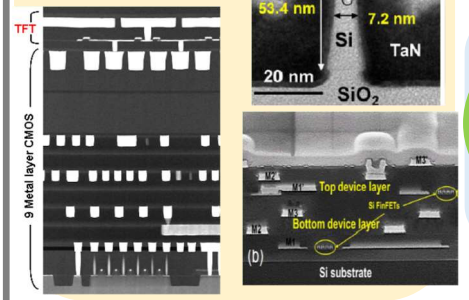
BEOL compatible materials for 3DSI logic & memory

BEOL FETs

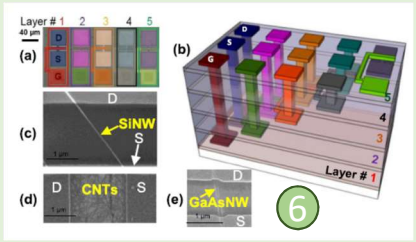
Poly-Si

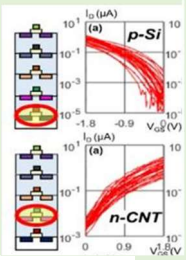
2 *PolySi FinFET*

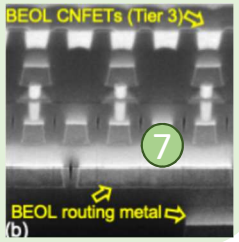
1 *TFT*



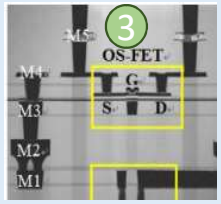
CNT

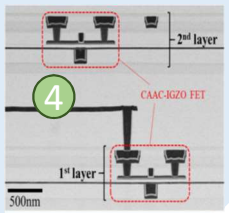


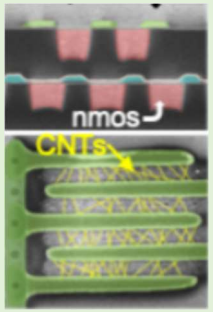




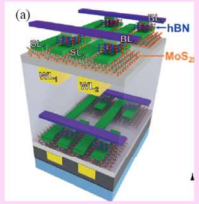
Oxide SC
IGZO, ITO,..

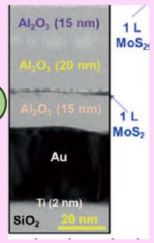






2D mat.
MoS_2,BN,.



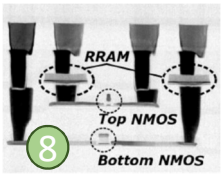


1) T. Naito et al., VLSI'10 (Toshiba)
2) P-Y. Hsieh et al, IEDM'16 (TSRI)
3) S-H. Wu et al., VLSI'16 (SEL)
4) M. Oota et al., IEDM'19 (SEL)
5) C-H Wang et al, IEDM'18 (Stand.)

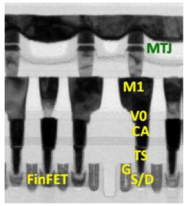
6) P-S. Kanhaiya., Trans. on Nanotech. 2019 (MIT)
7) T. Srimani et al., VLSI'20, (MIT)

BEOL memory devices

RRAM



MRAM



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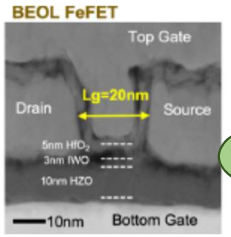
FeFET



10

8) E. Esmanhotto, IEDM'20 (Leti)
9) D. Edelstein et al., IEDM'20, (IBM)
10) S. Dutta et al., IEDM'20 (ND univ)

Energy Efficiency

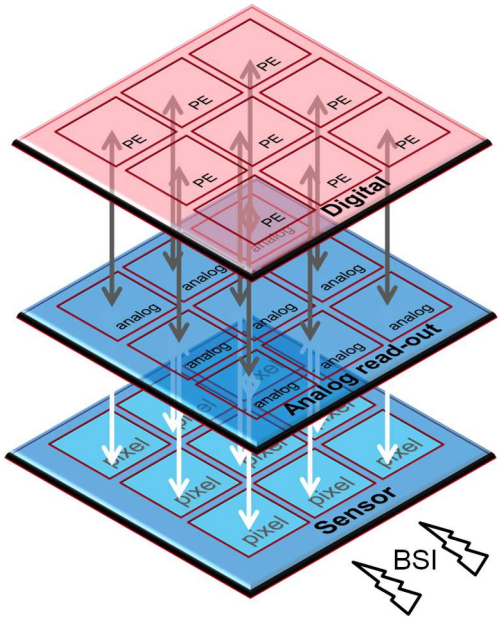
Cost reduction

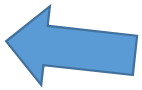
>2 device layer stacking: multilayer
→Ultra low TB devices, BEOL compatible
→Low cost devices preferred

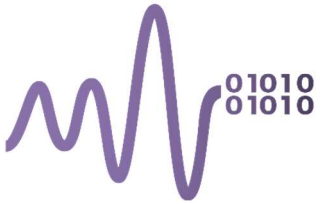
3D sequential opportunities

More Moore

Image Sensor







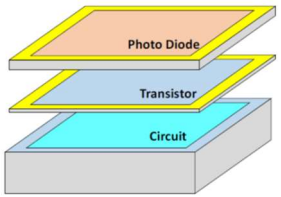
Smart Sensors

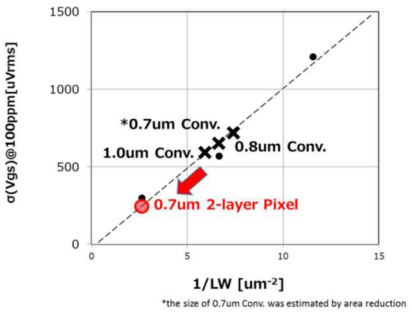
Miniaturized and efficient sensor arrays

More than Moore

3DSI demonstrators - small pixel image sensors

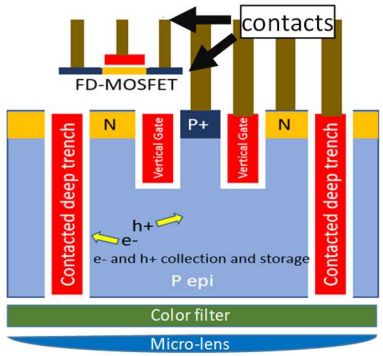
2-Layer Transistor Pixel Stacked CMOS Image Sensor
33M Pixels 0.7µm

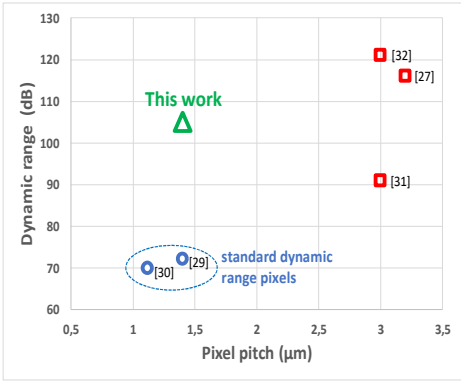




K. Nakazawa et al., IEDM 2021 (SONY)

Image Sensor with Back Side PhotoDiode
1.4µm High Dynamic Range pixel

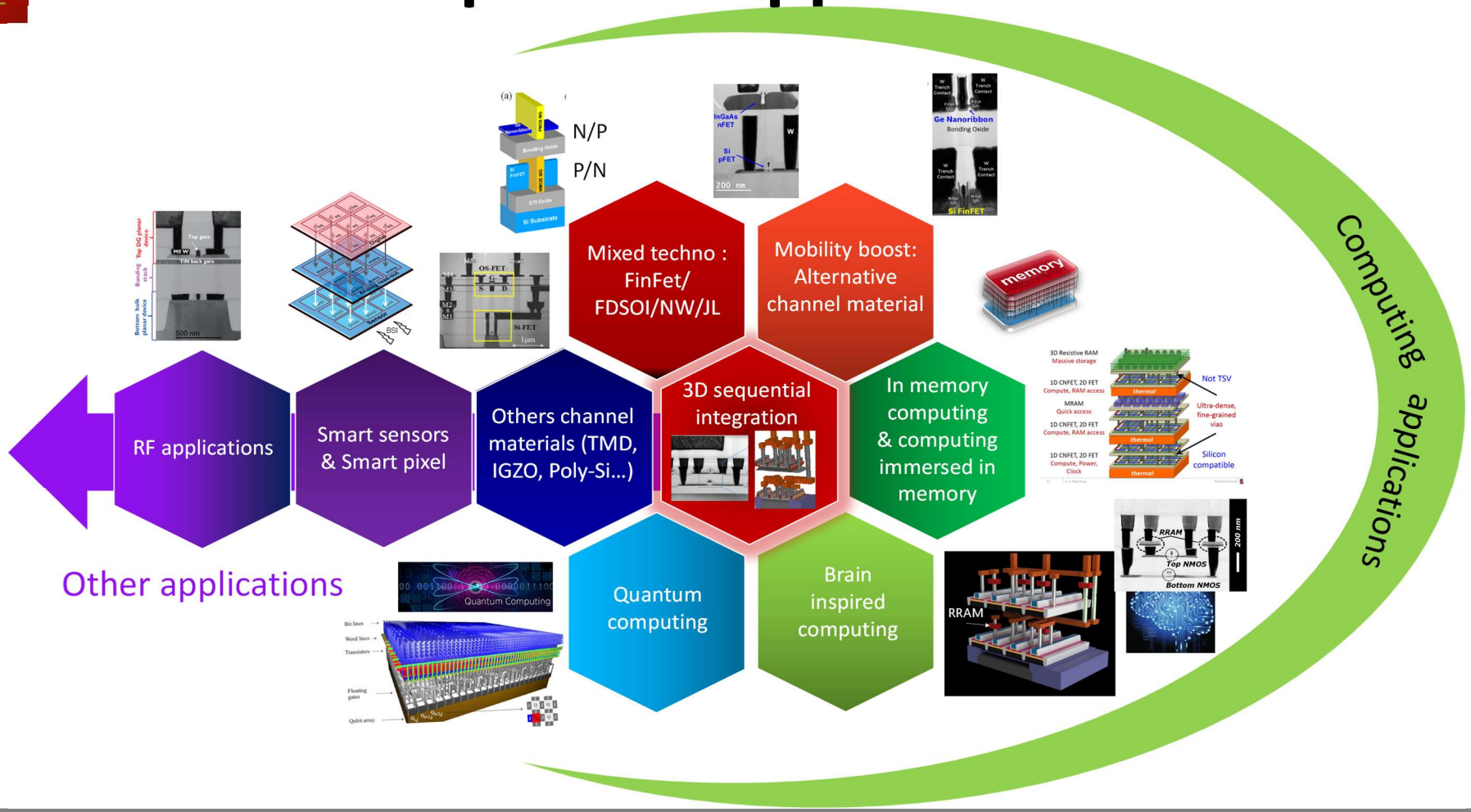




P. Batude[1], P. Malinge[2] , IEDM 21 ([1]Leti, [2]STMicroelectronics)

First industrial 3DSI demonstrators → image sensor with improved performance
3D seq offers further scalability and added value (smarter pixel)

3D sequential applications

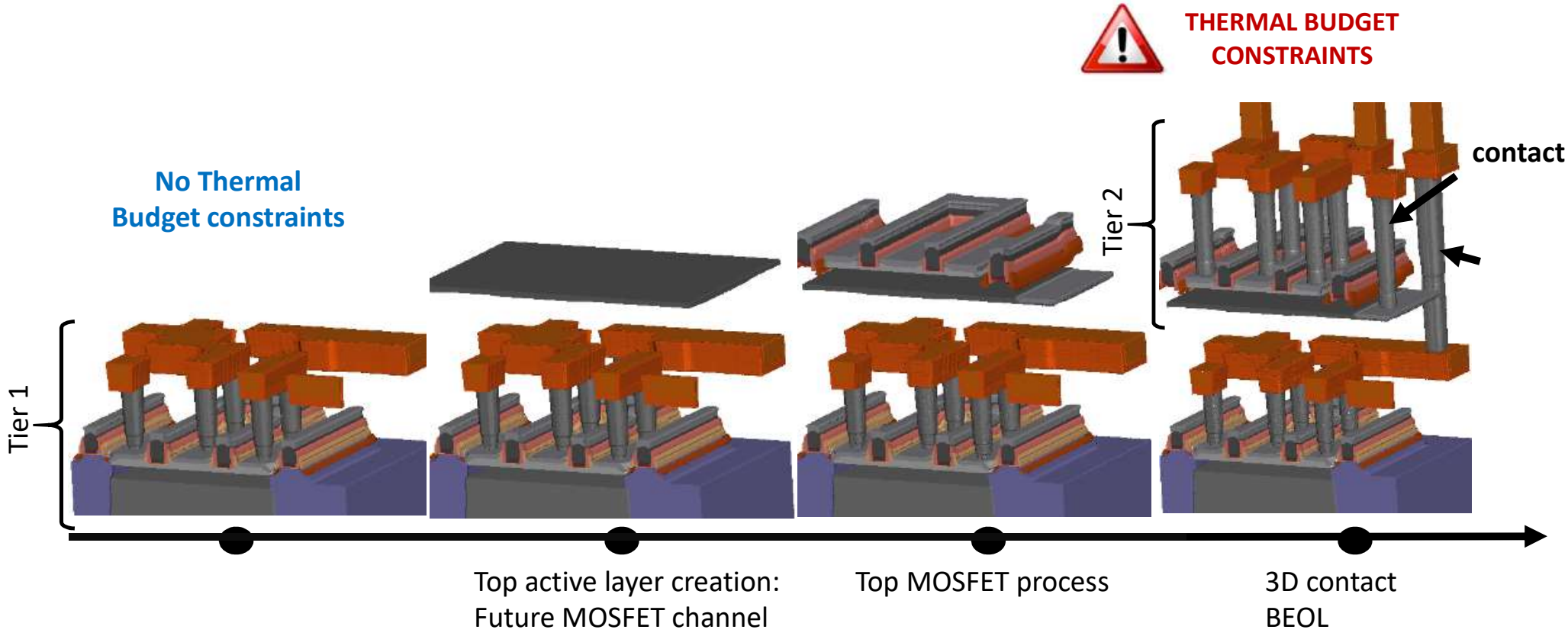


→ 3DSI offers a unique opportunity for More than Moore & Beyond Moore applications

Outline

- Introduction to 3D sequential integration
- Max thermal budget for the Top Tier
- Key process steps for a low temperature high performance 3DSi CMOS integration
  - Gate stack module
  - Junction engineering
  - Other processes required for RF applications
- Conclusion

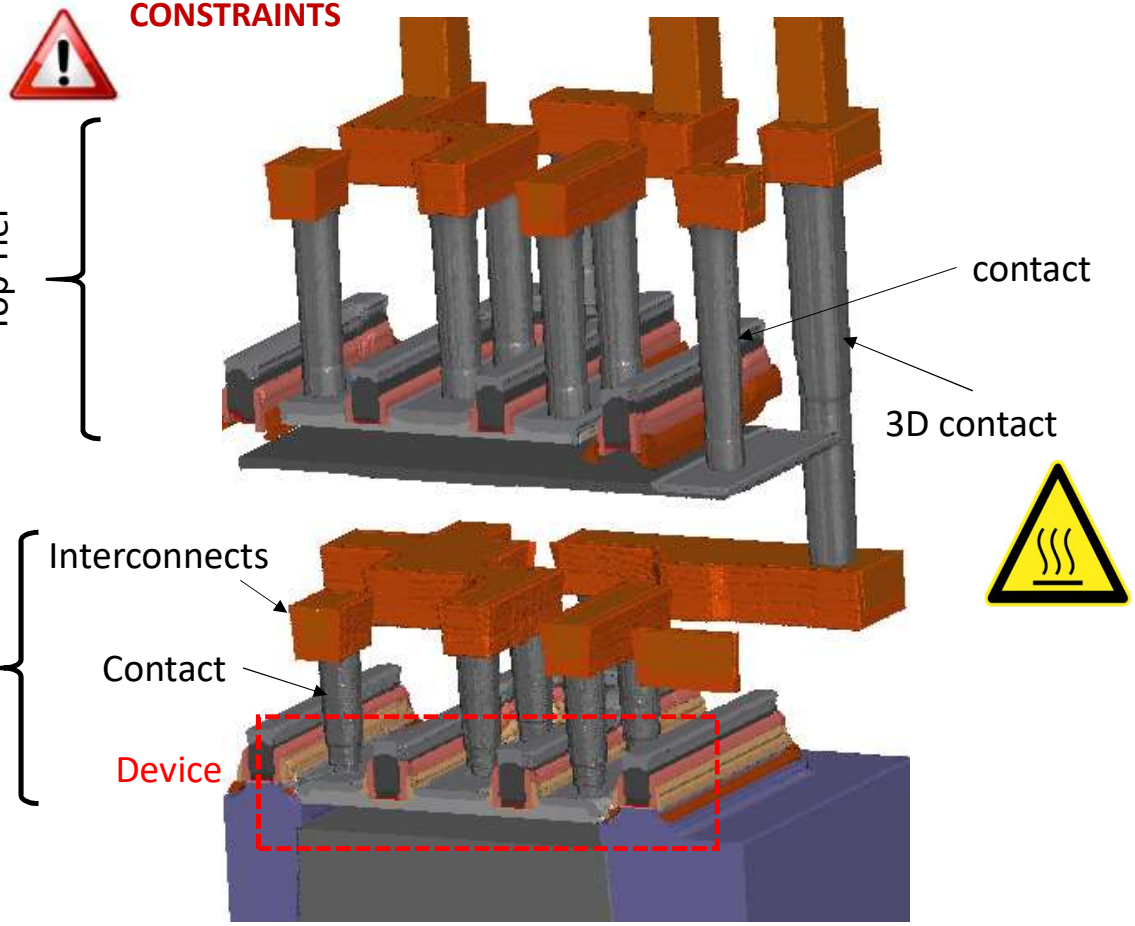
3D sequential integration flow – Si channel



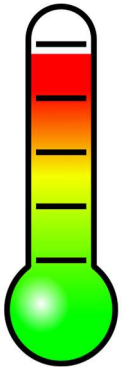
Also named 3D monolithic, 3D VLSI, CoolCube™ …

3D sequential integration flow – Si channel

THERMAL BUDGET CONSTRAINTS

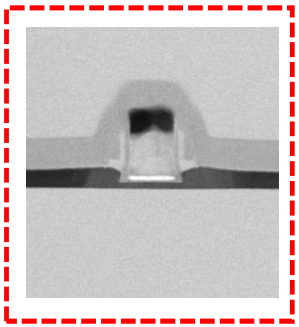


Max thermal budget for Top Tier process?



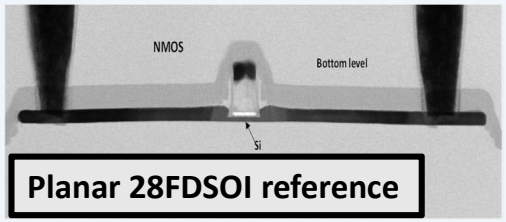
→Needs to preserve the stability of the Bottom Tier ie FET+ Interconnects

Thermal stability of the Si Bottom Tier? - MOSFET



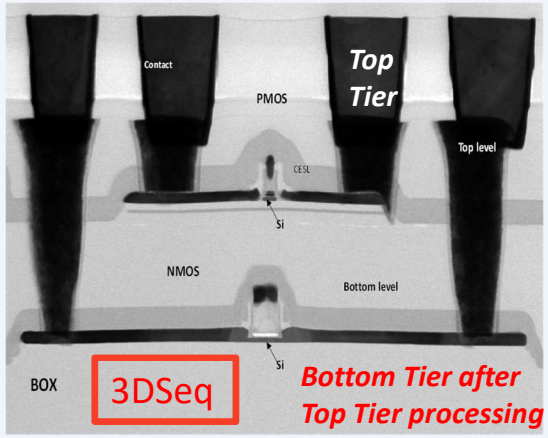
Single Device

1



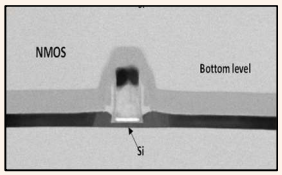
Planar 28FDSOI reference

VS



2

- 28nm FDSOI bottom device



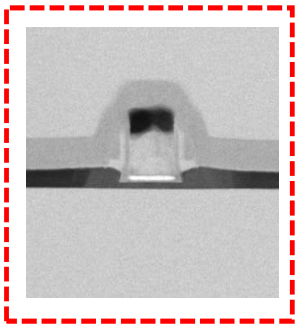
- Additional annealings (various T°C & durations)
- Cu/ULK 28nm BEOL processing

Thermal Budget

→Top Tier processed at 630°C-2h (spacer formation)

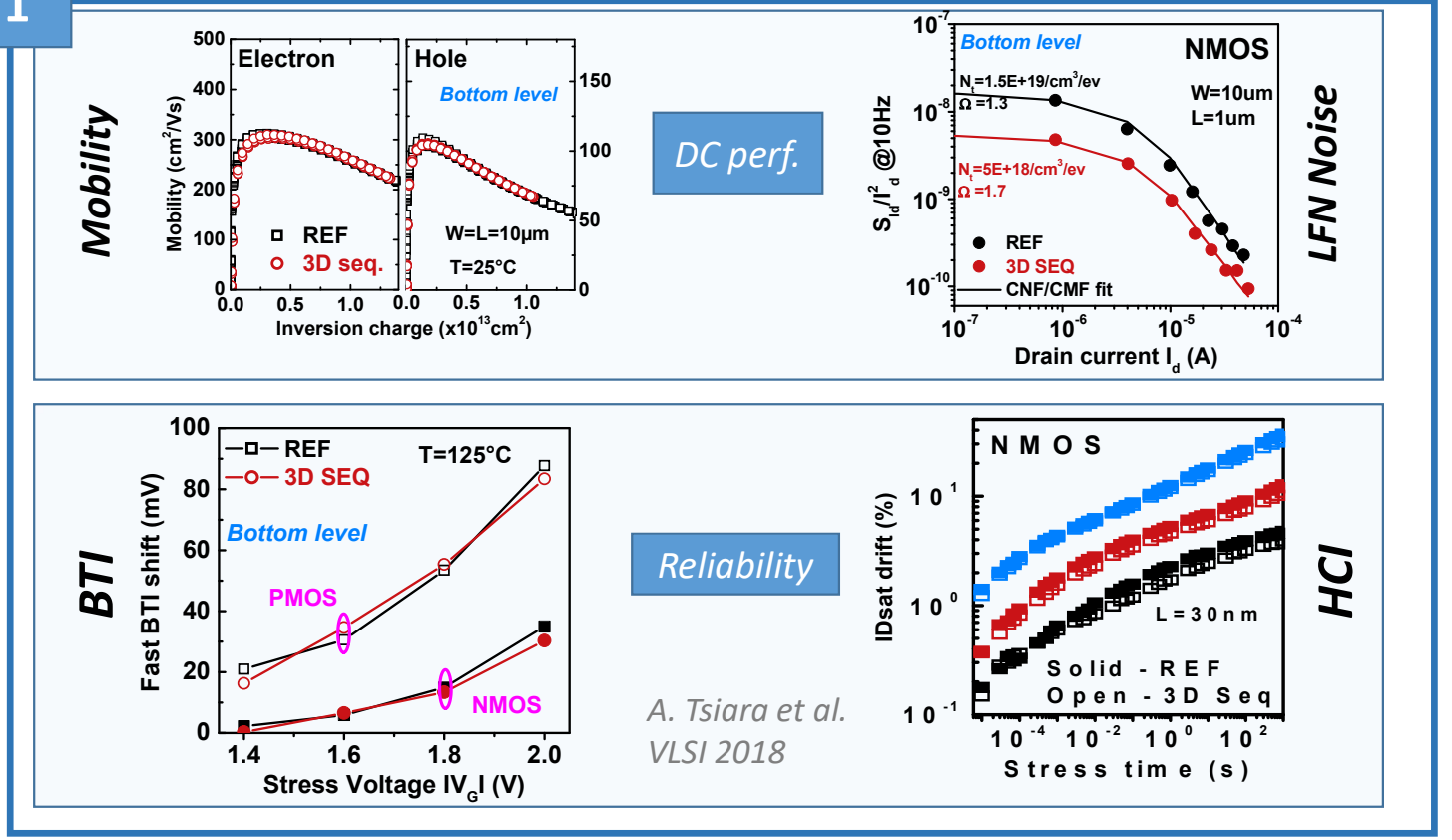
→Add. Anneals 450-600°C

Thermal stability of the Si Bottom Tier? - MOSFET



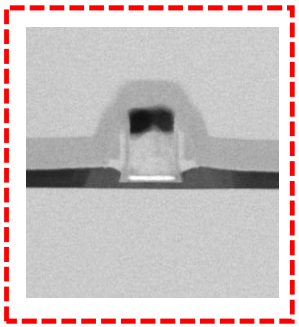
Single Device

1



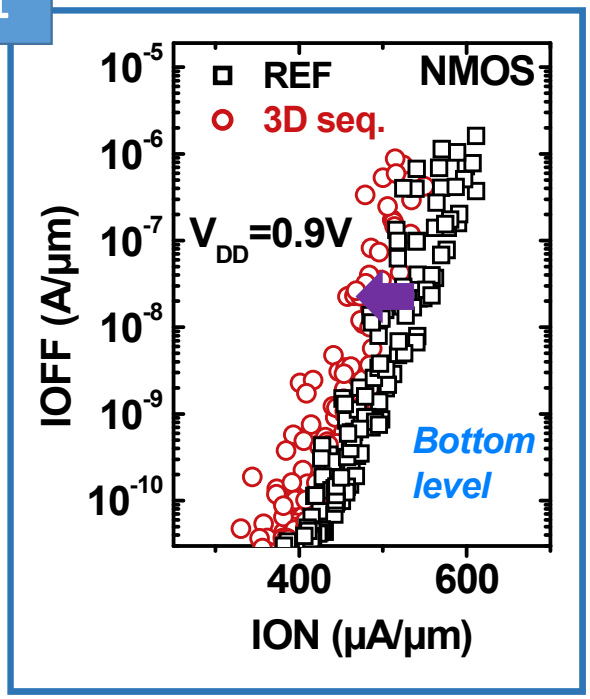
→Intrinsic MOSFET properties are preserved up to 630°C

Thermal stability of the Si Bottom Tier? - MOSFET



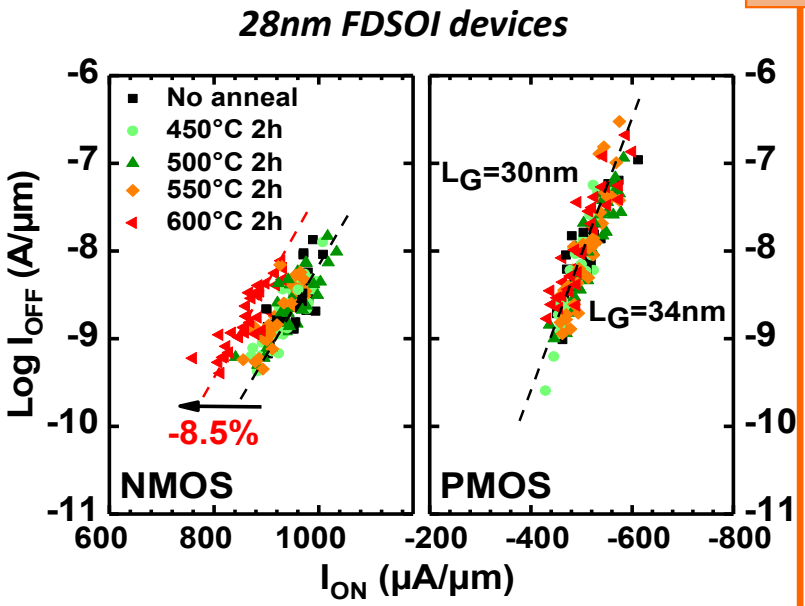
Single Device

1



A. Tsiara et al., VLSI 2018 (Leti)

2

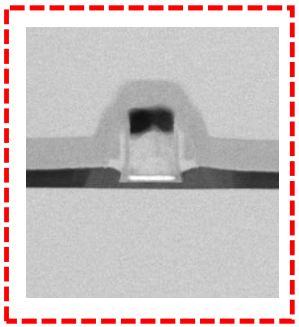


C. Cavalcante et al., VLSI 2020 (Leti)

- Max TB for short channel devices - 550°C-2H
- Perf. degradation at T>600°C

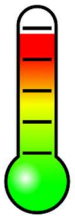
Thermal stability of the Si Bottom Tier? - MOSFET

2



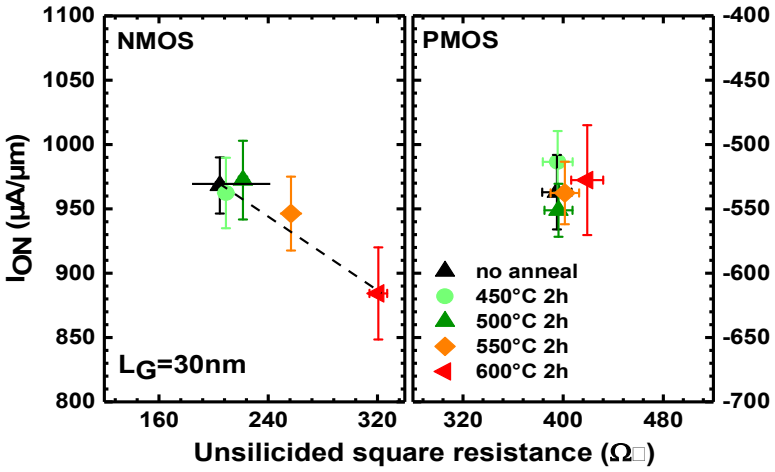
Single Device

Max TB

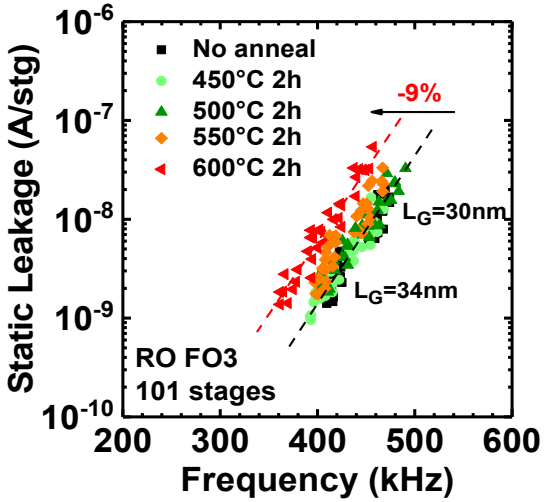


550°C-2H

28nm FDSOI devices



AC perf- ROs



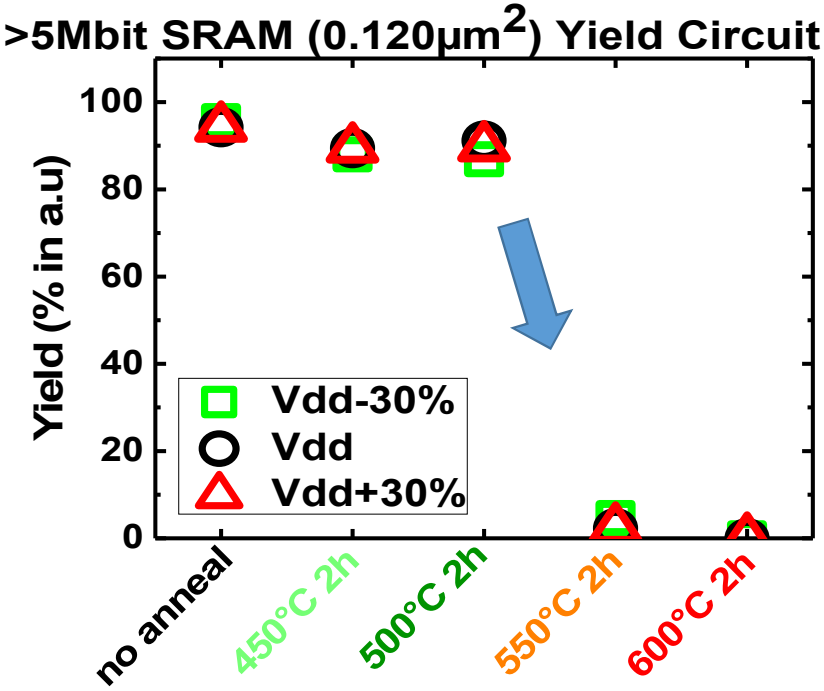
C. Cavalcante et al., VLSI 2020 (Leti)

ION correlated to *unsaliciliced* resistance
→ degradation due to dopants deactivation
→also impacts AC performance (leakage)

Thermal stability of the Si Bottom Tier? – SRAM array

Dense SRAM Array

- 28FDSOI
  5MB SRAM array
- Anneal post CMP, PMD
  (various T°C & durations)
- Cu/ULK 28nm BEOL
  processing



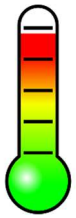
C. Cavalcante et al., VLSI 2020

→Yield reduction above 500°C-2H

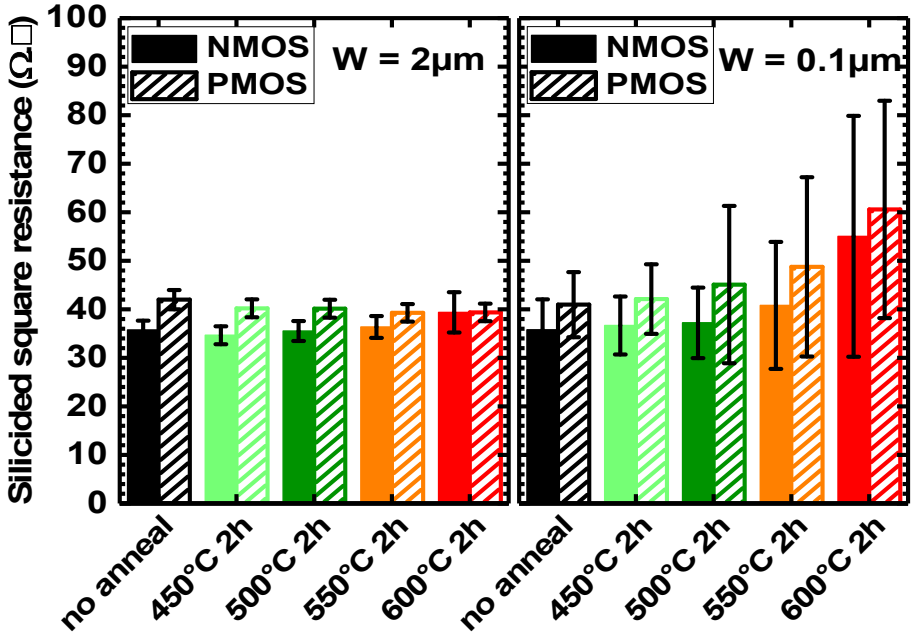
Thermal stability of the Si Bottom Tier? – SRAM array

Dense SRAM Array

Max TB

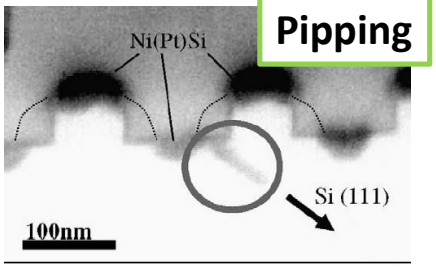


500°C-2H



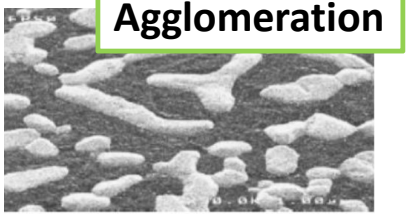
C. Cavalcante et al., VLSI 2020

Pipping



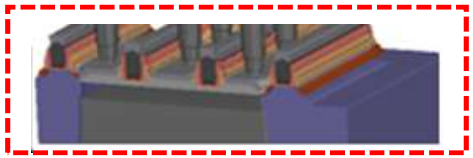
Phase change

Agglomeration

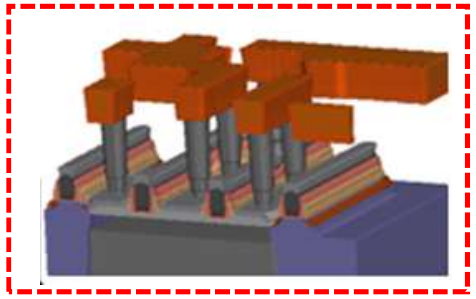


→Yield reduction above 500°C-2H
→ascribed to Salicide defects in dense structures

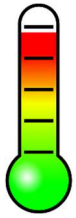
Thermal stability of the Si Bottom Tier? - Interconnects



Array



Array + Interconnects

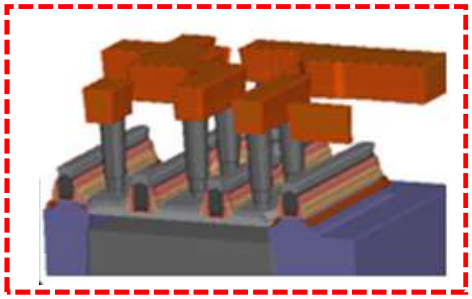


500°C-2H compatible with BEOL?

3

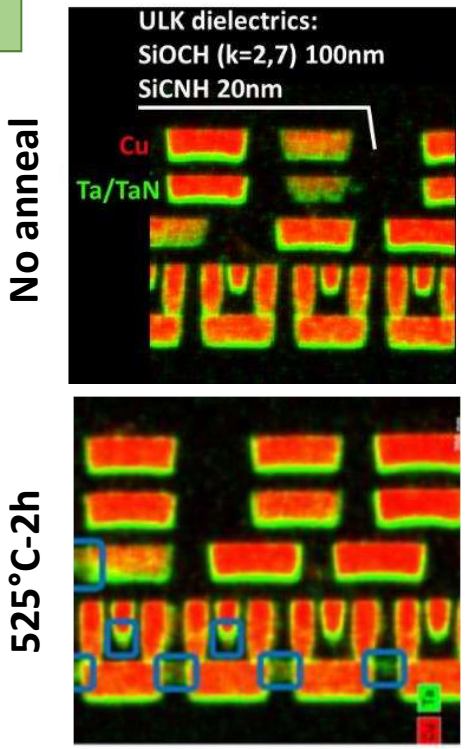
- 28nm FDSOI FEOL
- Cu/ULK 28nm BEOL
- Additional annealings (T= 450°C-525°C & durations)

Thermal stability of the Si Bottom Tier? - Interconnects

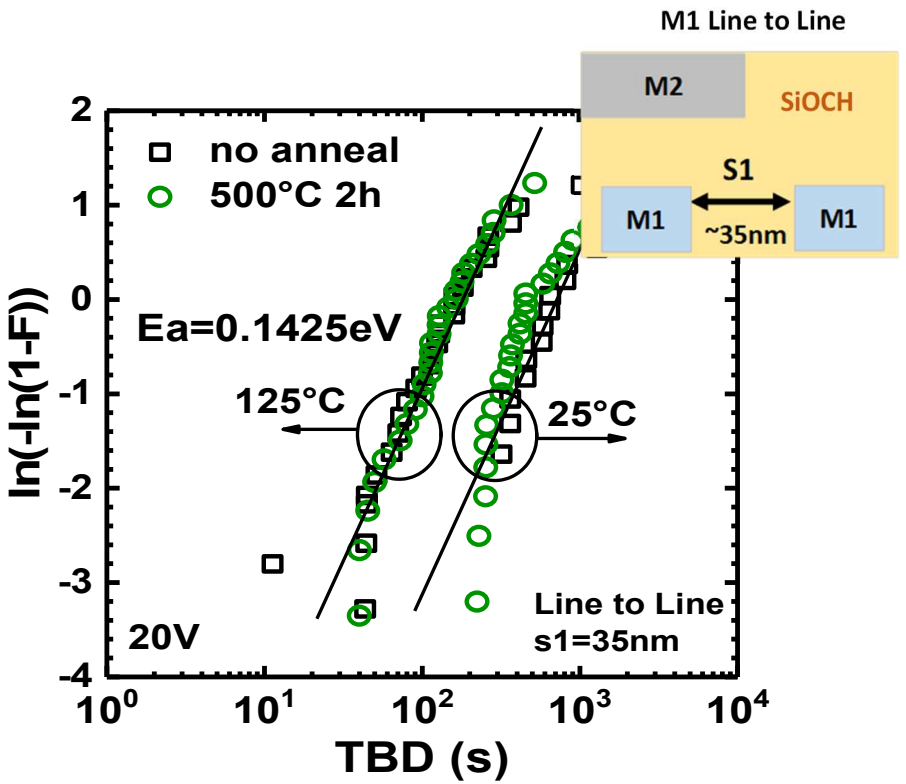


Array + Interconnects

3



S. Beaurepaire et al., MRS Spring, 2019

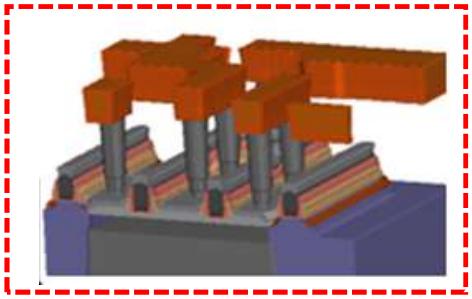


C. Cavalcante et al., VLSI 2020

→Interconnects are stable up to 500°C-2H

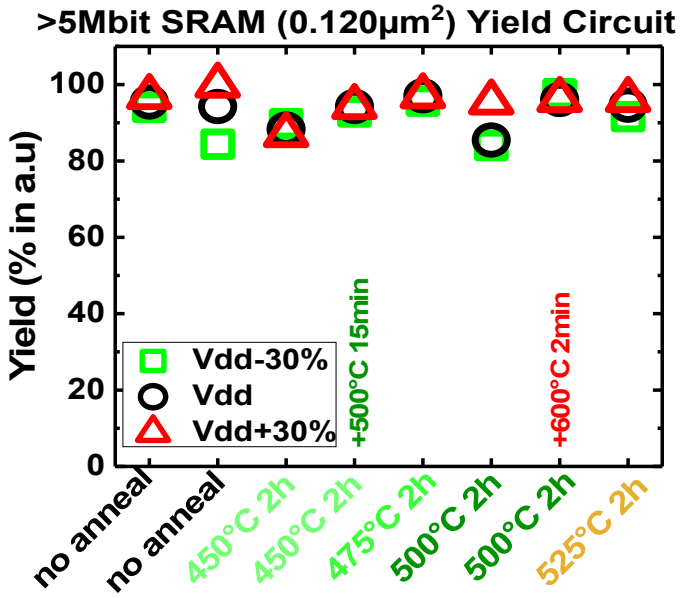
Thermal stability of the Si Bottom Tier? - FEOL+BEOL

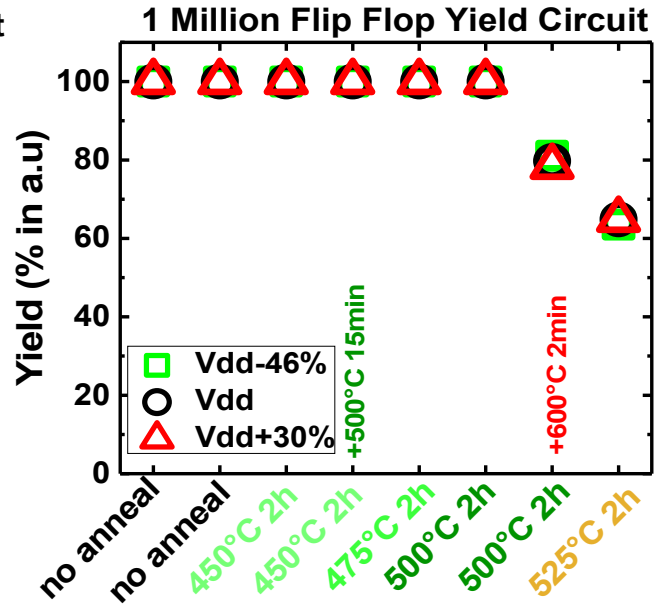
Anneals



Array + Interconnects

3



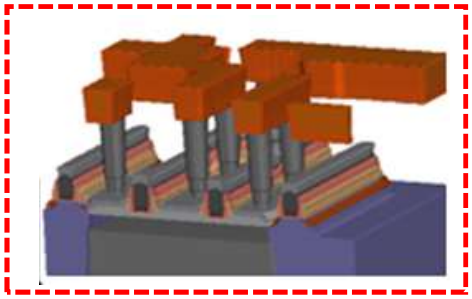


→Interconnects are stable up to 500°C-2H

→Confirmed by yield analysis on dense arrays

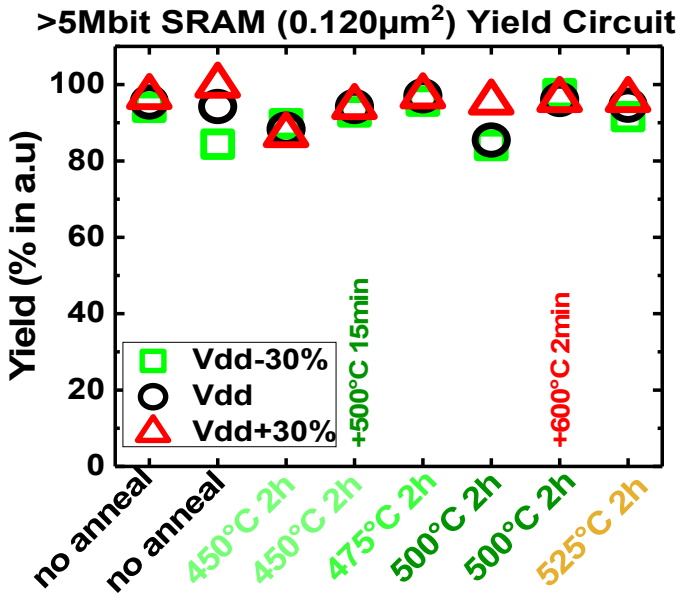
Thermal stability of the Si Bottom Tier? - FEOL+BEOL

Anneals

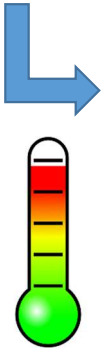


FEOL+BEOL

3



→FEOL stable up to 500°C-2h
→BEOL stable up to 500°C-2h

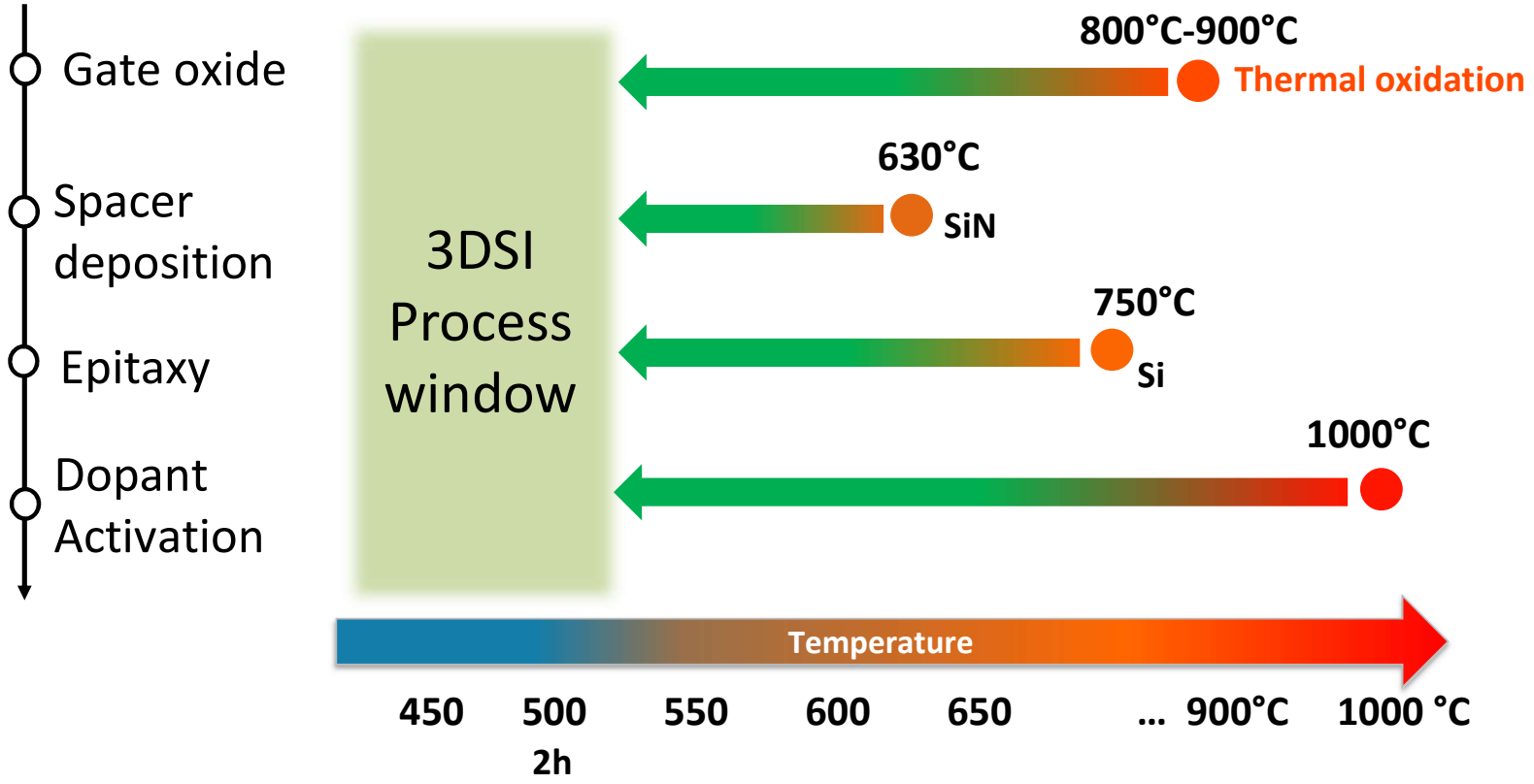


Safe thermal budget for Top Tier processing
500°C 2h

Outline

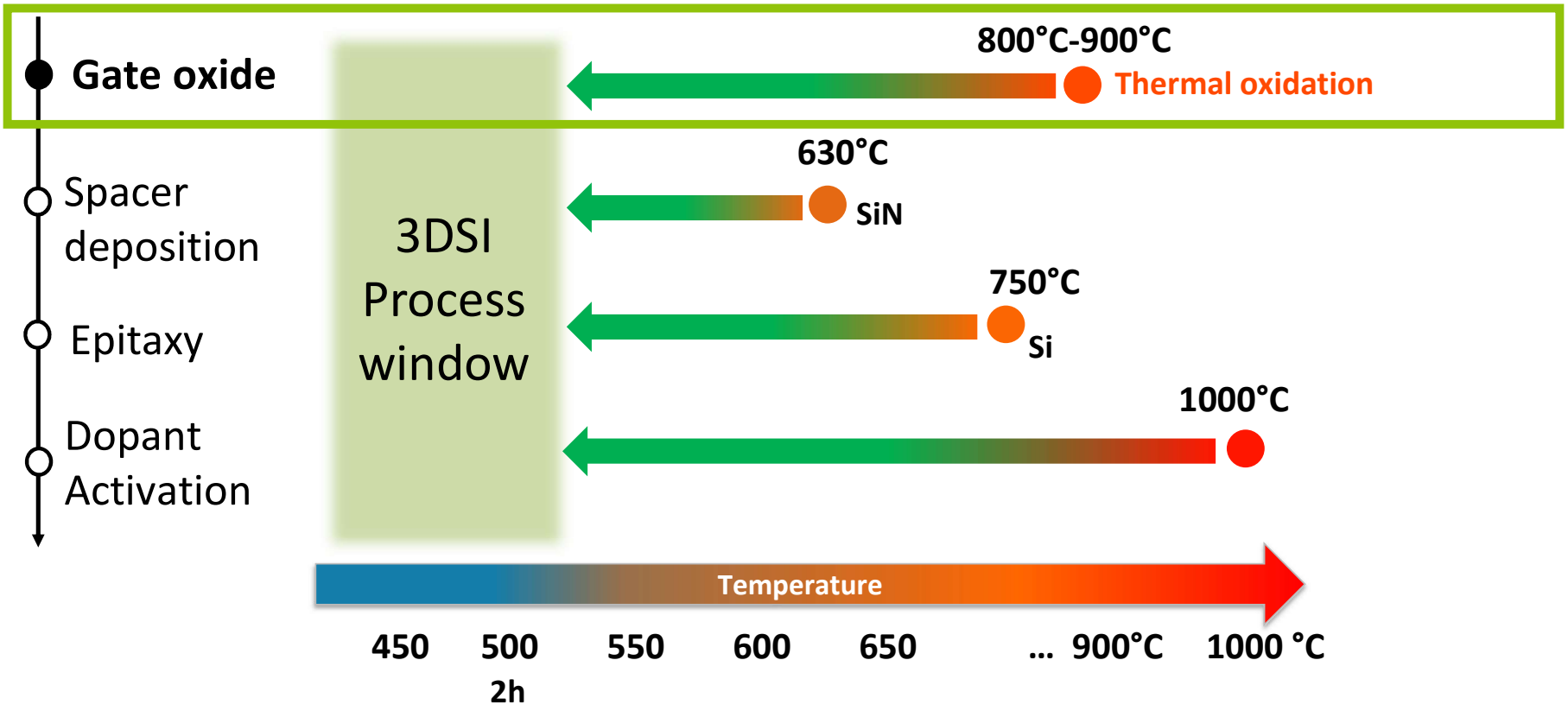
- Introduction to 3D sequential integration
- Max thermal budget for the Top Tier
- Key process steps for a low temperature high performance 3DSi CMOS integration
  - Gate stack module
  - Junction engineering
  - Other processes required for RF applications
- Conclusion

Low temperature process for Top Tier



→Each step of the Si process flow must be revisited to fabricate the Top Tier at 500°C

Low temperature process for Top Tier



→Each step of the Si process flow must be revisited to fabricate the Top Tier at 500°C

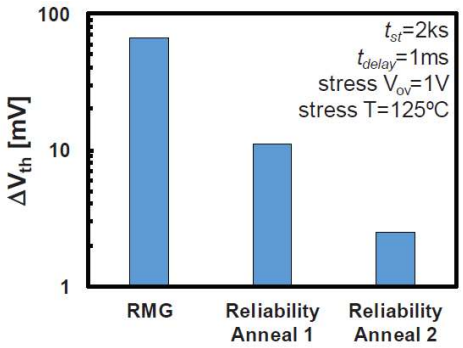
Gate stack challenges at low temperature

Gate oxide

- Main issue at 500°C→oxide reliability

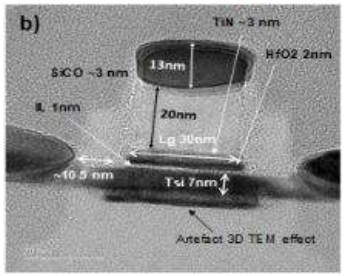
→ *Cannot use "Reliability anneals" at T>800°C to cure oxide defects*

→ *Same concern for both Gate First & Gate Last*



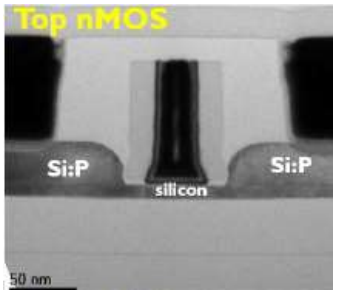
J. Franco et al., IEEE IRPS, 2017

Gate First



C. Fenouillet-Beranger et al., EDL,68, 2021 (Leti)

Gate Last /RMG



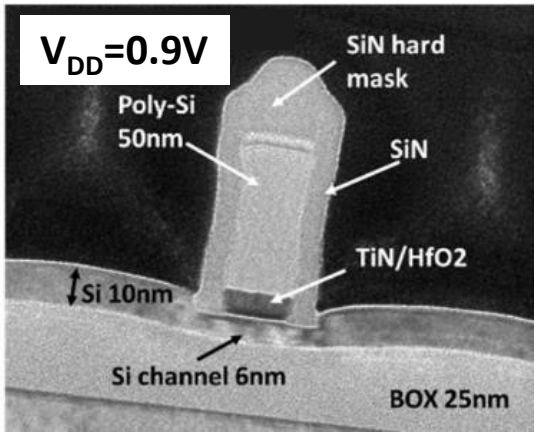
A. Vandooren et al., EDL,65, 2018 (IMEC)

Gate stack needs to be rethought

Gate stack challenges at low temperature

Gate oxide

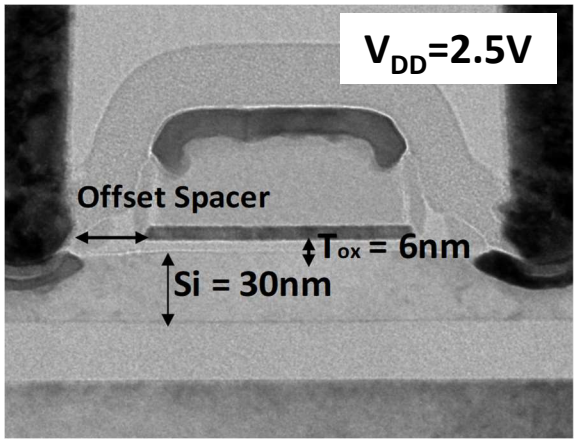
Digital CMOS



L. Brunet et al., IEDM 2018 (Leti)

Gate First

Analog



C. Cavalcante et al., IEEE VLSI-TSA 2020 (Leti)

Max TB 500°C-2H

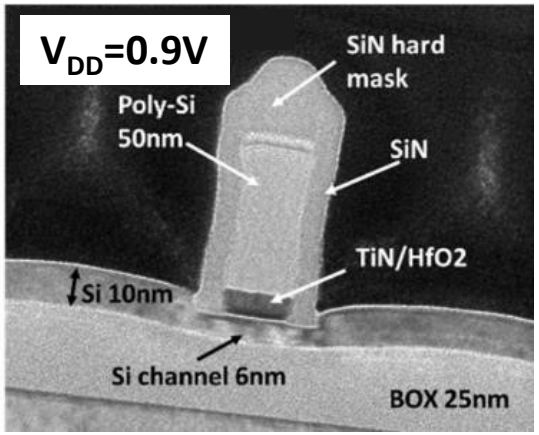
- N&PMOS L_G=30nm
- undoped Si film 6nm
- **thin oxide HK/MG**

- N or PMOS L_G=250nm
- doped Si film 30nm
- **thick oxide SiO_2~6nm**

Gate stack challenges at low temperature

Gate oxide

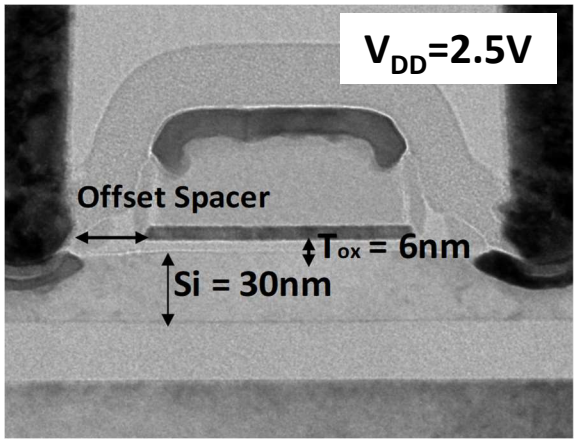
Digital CMOS



L. Brunet et al., IEDM 2018 (Leti)

Gate First

Analog



C. Cavalcante et al., IEEE VLSI-TSA 2020 (Leti)

Max TB 500°C-2H

Requirements		Digital	Analog
Performance	EOT	++	--
	Leakage	-	+
	LF Noise	-	++ (low Dit)
Reliability		++ (NBTI&PBTI)	+ (NBTI or PBTI)

Challenging

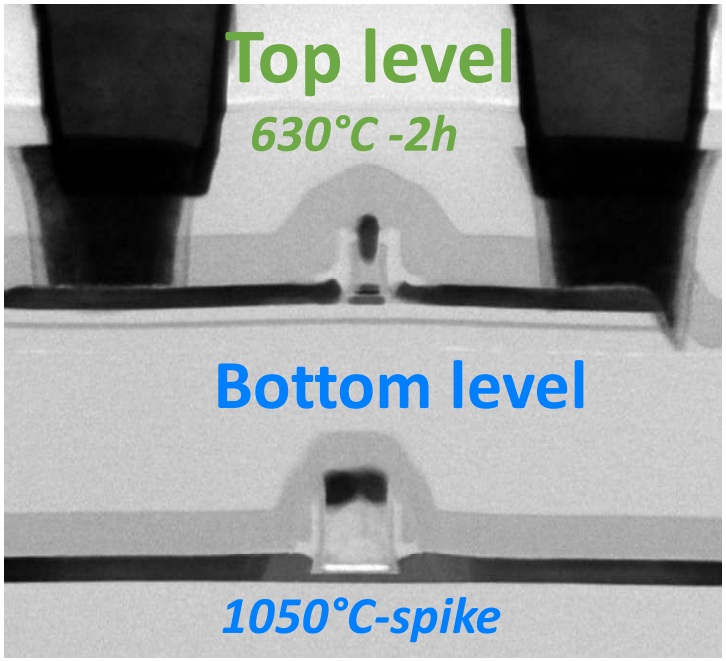
High

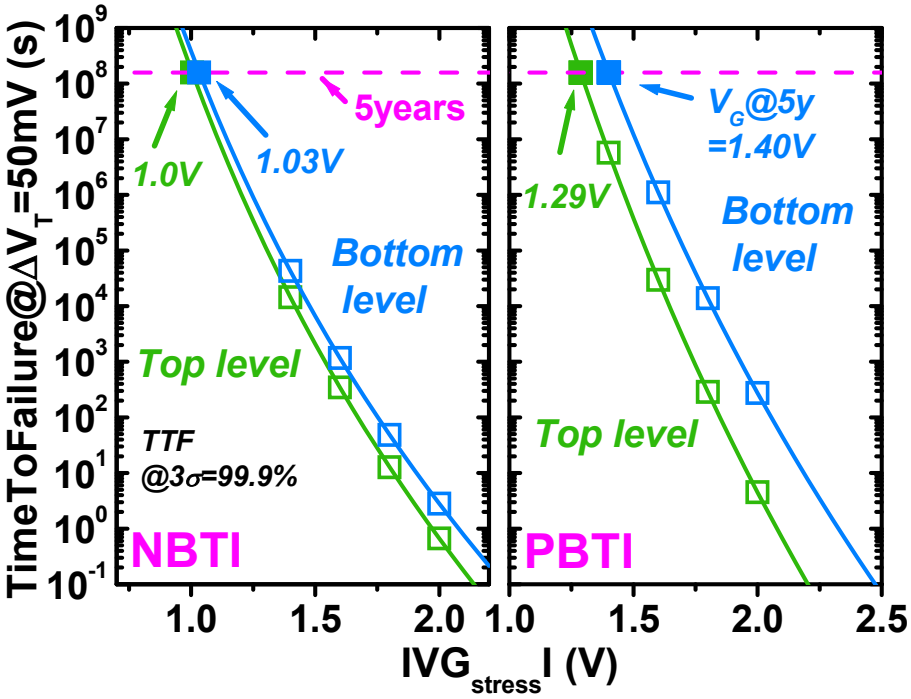
Low

Gate Oxide Reliability - true 3DSI integration

Digital

HK/MG





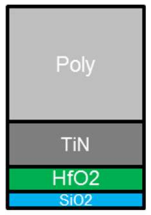
A. Tsiara et al., VLSI 2018 (Leti)

→Top Level (630°C-2h) meets the BTI requirements

→*But TB must be reduced to 500°C-2h*

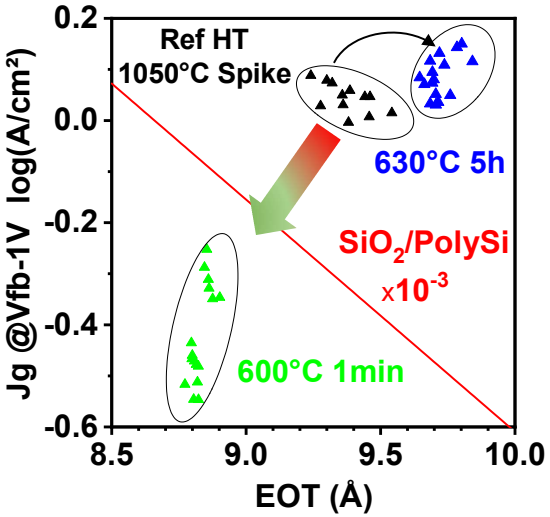
Impact of Thermal Budget on thin oxide - Digital

Digital

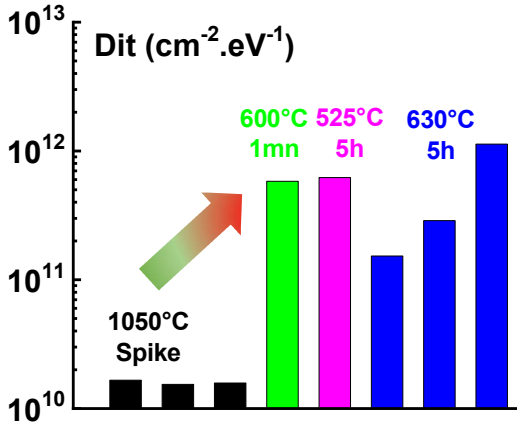


MOScap

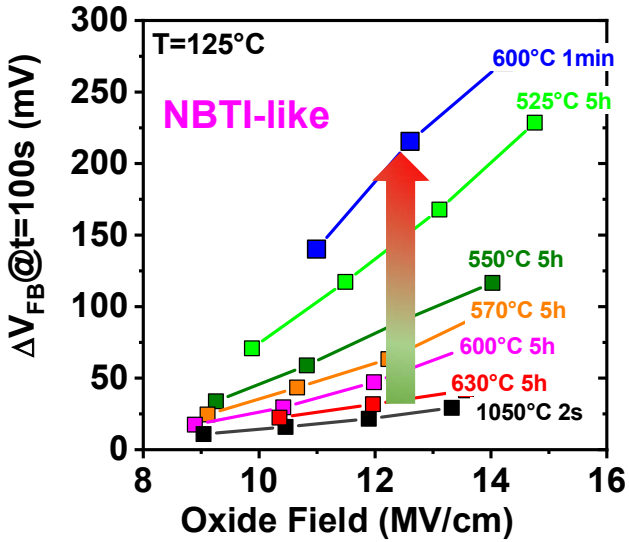
Oxide Performance



Interface Quality



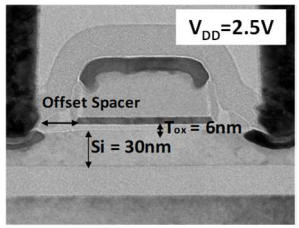
Oxide Reliability (NBTI)



→Reducing the Thermal Budget <600°C is favorable to improve gate stack perf. (lower EOT)
→ But also degrades interface quality and NBTI reliability

Impact of Thermal Budget on thick oxide - Analog

Analog



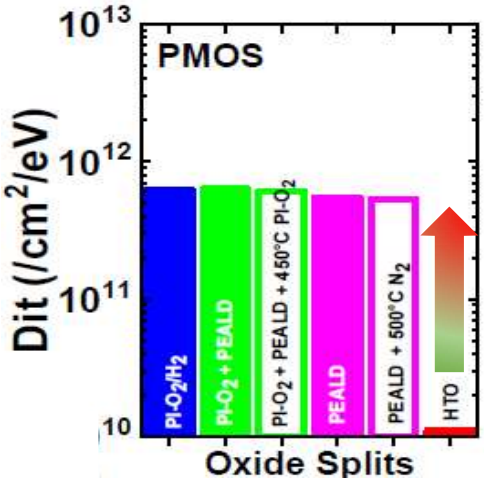
PMOSfet

SiO_2 6nm

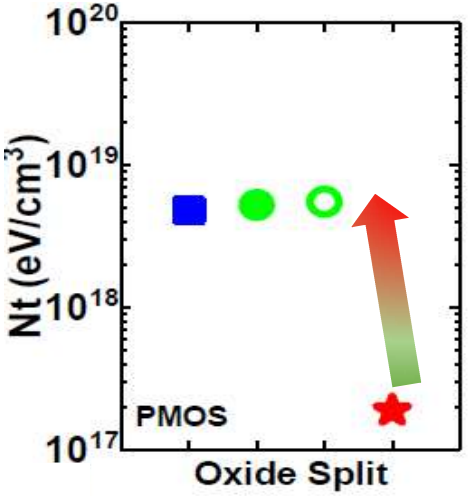
- $Pl\text{-}O_2/H_2$ *450°C*
- $Pl\text{-}O_2$+PEALD *400°C*
- $Pl\text{-}O_2$+PEALD *+450°C ann.*
- PEALD *200°C*
- PEALD *+500°C ann.*
- HTO Ref *1000°C*

Low Temp Plasma oxidation

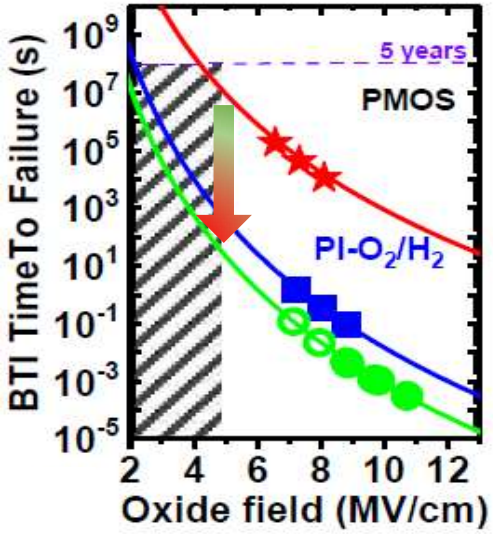
Interface Quality



LF Noise



NBTI reliability



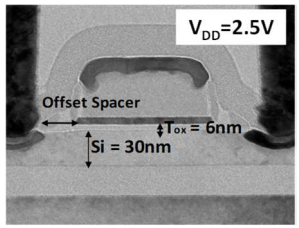
C. Cavalcante et al., IEEE VLSI-TSA 2020 (Leti)

→Same behavior for thick oxide

→ Reducing TB below 500°C degrades interface quality, Noise and NBTI reliability,

Impact of Thermal Budget on thick oxide - Analog

Analog



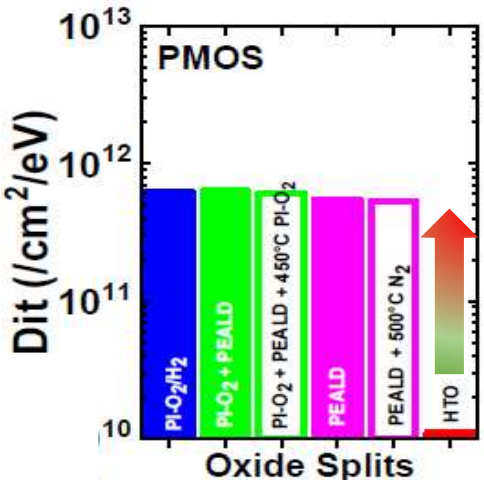
PMOSfet

SiO_2 6nm

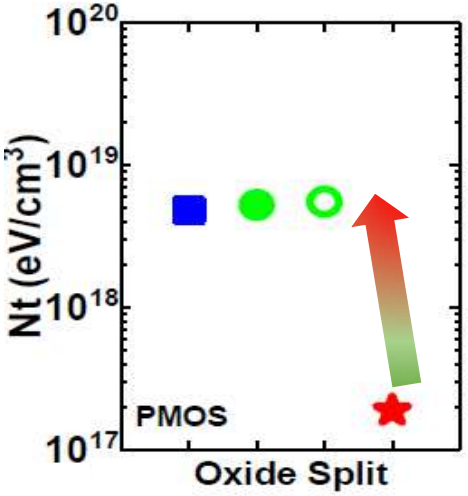
- $Pl\text{-}O_2/H_2$ *450°C*
- $Pl\text{-}O_2$+PEALD *400°C*
- $Pl\text{-}O_2$+PEALD *+450°C ann.*
- PEALD *200°C*
- PEALD *+500°C ann.*
- HTO Ref *1000°C*

Low Temp Plasma oxidation

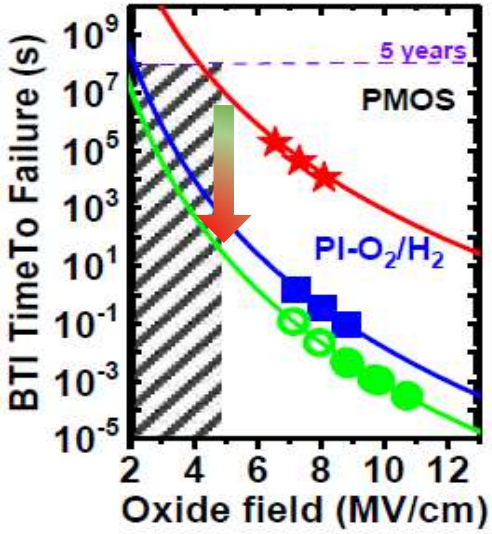
Interface Quality



LF Noise



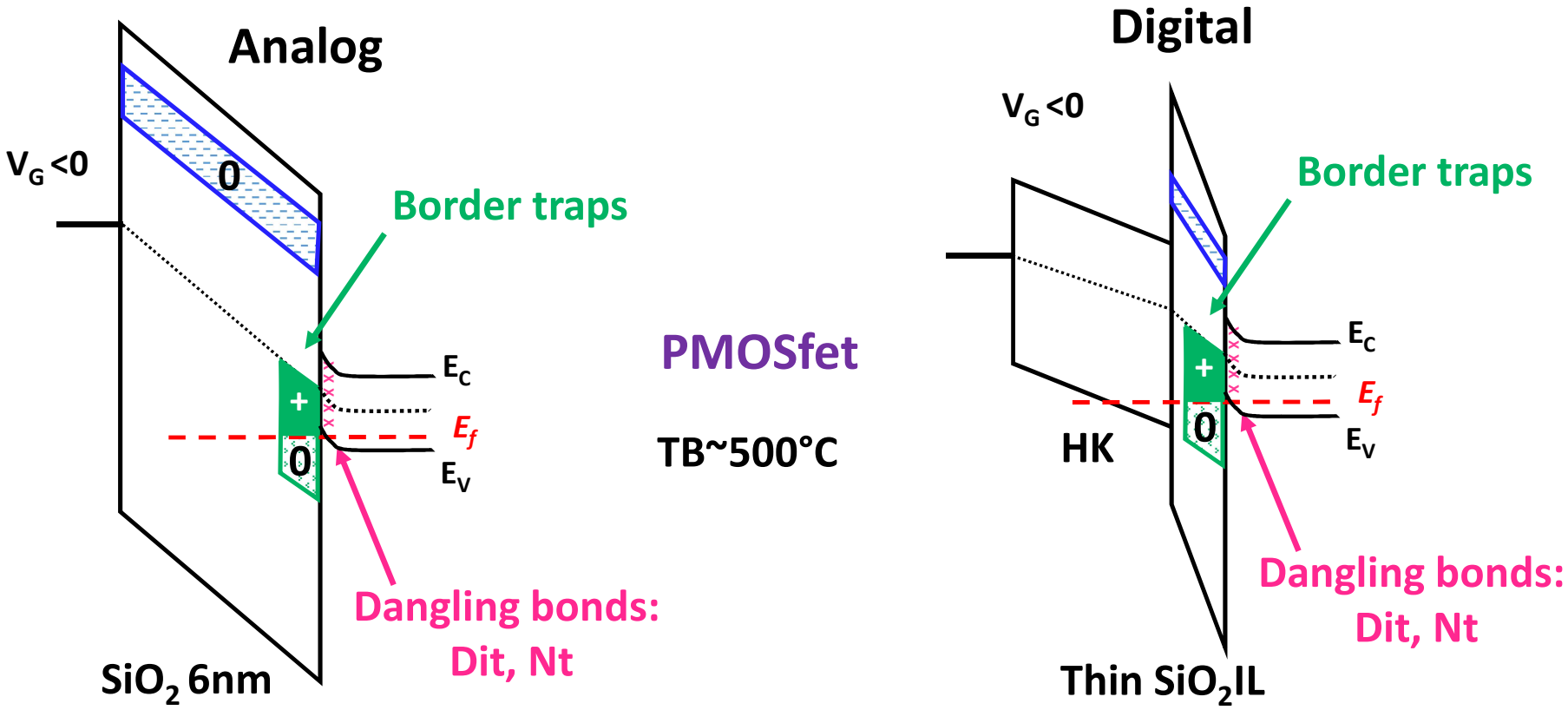
NBTI reliability



High Dit ⟷ **High Nt** ⟷ **Low NBTI lifetime**

→Great correlation between Dit, Noise and NBTI

Understanding of poor Low Temp PMOS reliability

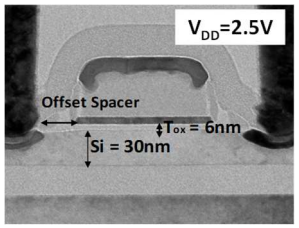


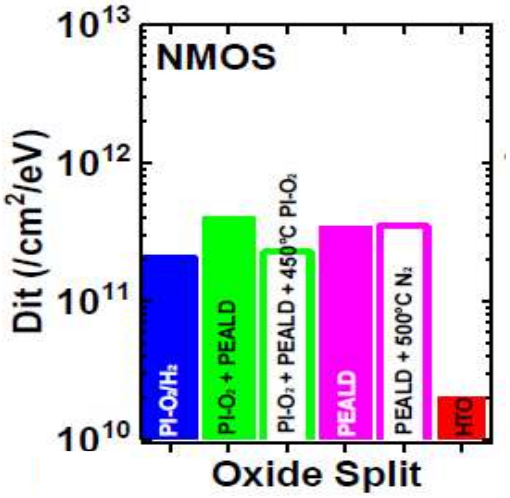
→ Same degradation for Analog & Digital gate stacks

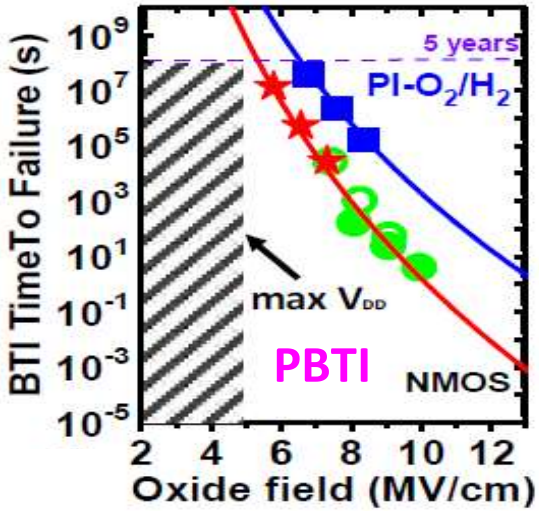
→*Higher Si Interface + Border Traps in SiO_2 or IL are responsible for poor PMOS reliability*

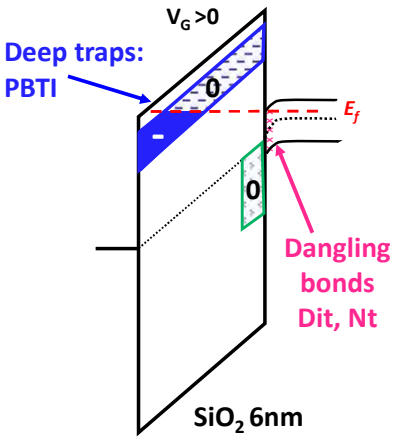
NMOS reliability at low temperature

Analog



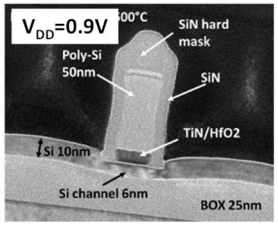


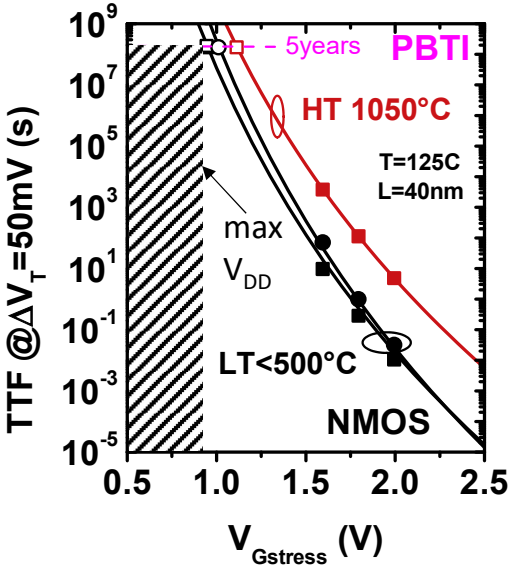




Dit ≠ PBTI traps

Digital





→PBTI reliability at T<500°C due to deep traps in bulk SiO_2 or bulk HK

→meet the requirements for both digital & analog applications unlike NBTI

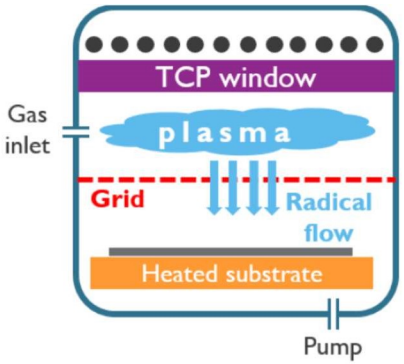
Gate stack reliability improvement strategies

- Multiple strategies to achieve sufficient BTI reliability in top-tier low temperature devices
  - Atomic hydrogen treatment (PMOS NBTI)
  - J-Less operation in accumulation mode → BTI improvement
  - Dipole insertion between SiO_2 and HfO_2
  - Back Bias forward in inv mode MOS → BTI improvement

Z. Wu et al, IEEE Trans on Elec Dev Vol 88, n°2, Feb 2021

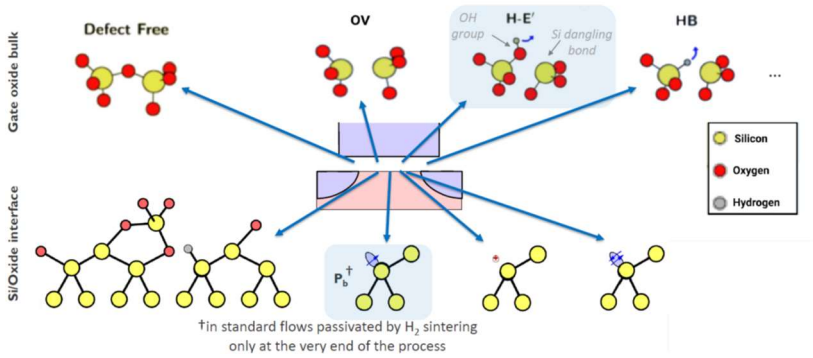
Multiple strategies to achieve sufficient BTI reliability in top-tier low temperature devices

NBTI solution - Low Temp Atomic Hydrogen anneal

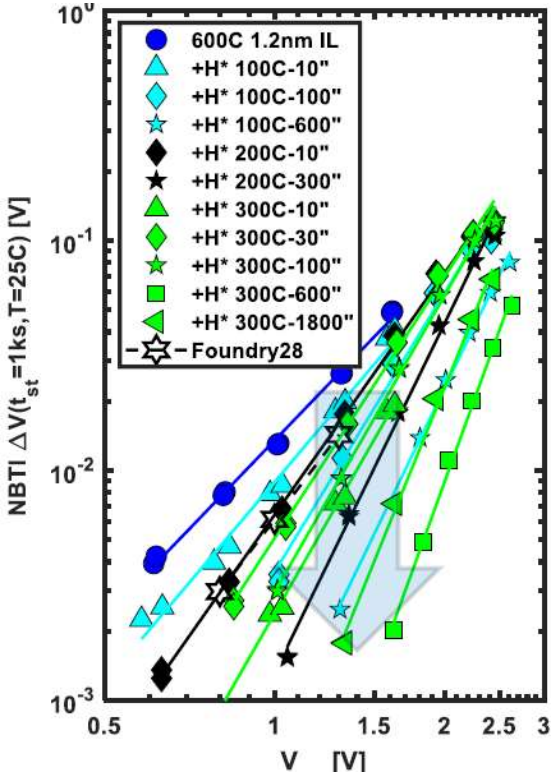


- IL formation
  - ISSG 600°C 1.2/1.8nm or chemOx 0.6nm
  - Additional ref.: ISSG 700°C, RTO 900°C
- **H* exposure (remote H_2 plasma)**
  - 100/200/300°C, 10"-1800"
- **[Sint. H_2 400°C-20' for EOT control]**
- 1.8nm HfO_2 dep. (300°C)
- 5nm TiN (450°C) + 60nm W dep. (430°C)
- Gate patterning
- Sintering H_2 400°C-20'

Microscopic defect structures in Si/SiO_2 system



Hydrogen radicals (H*) generated in a low-T remote plasma were used to passivate hole traps associated with the hydroxyl-*E'* (H-*E'*) SiO_2 defects in 1.2nm thick interface layers (IL).

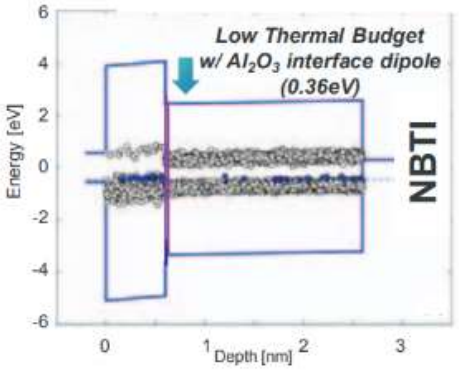


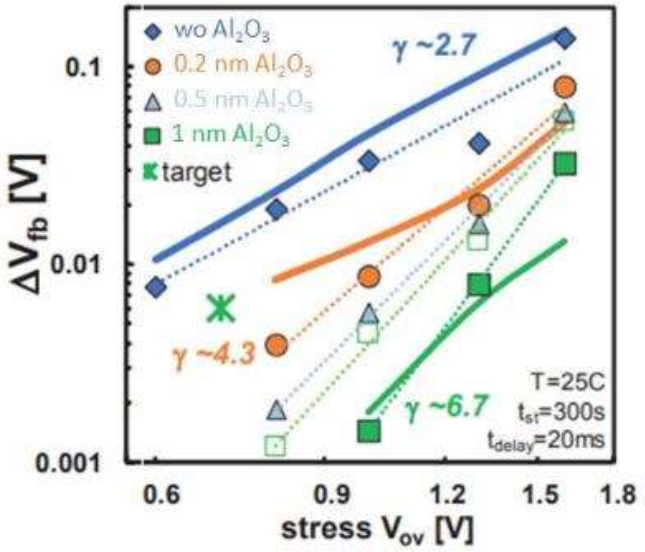
J. Franco et al., IEEE VLSI 2021 (IMEC)

→Remote Hydrogen plasma improves NBTI

Other NBTI reliability solutions

Al_2O_3 Dipole insertion between SiO_2 and HfO_2

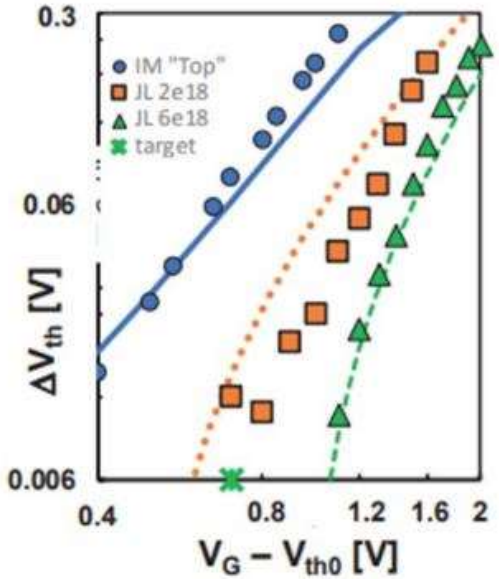




J. Franco, IEDM 2018 (imec)

Negative dipole former on SiO_2
Defect energy shift relatively to valence band
Shift of Vfb 0.4eV LaSiOx

Junction less device

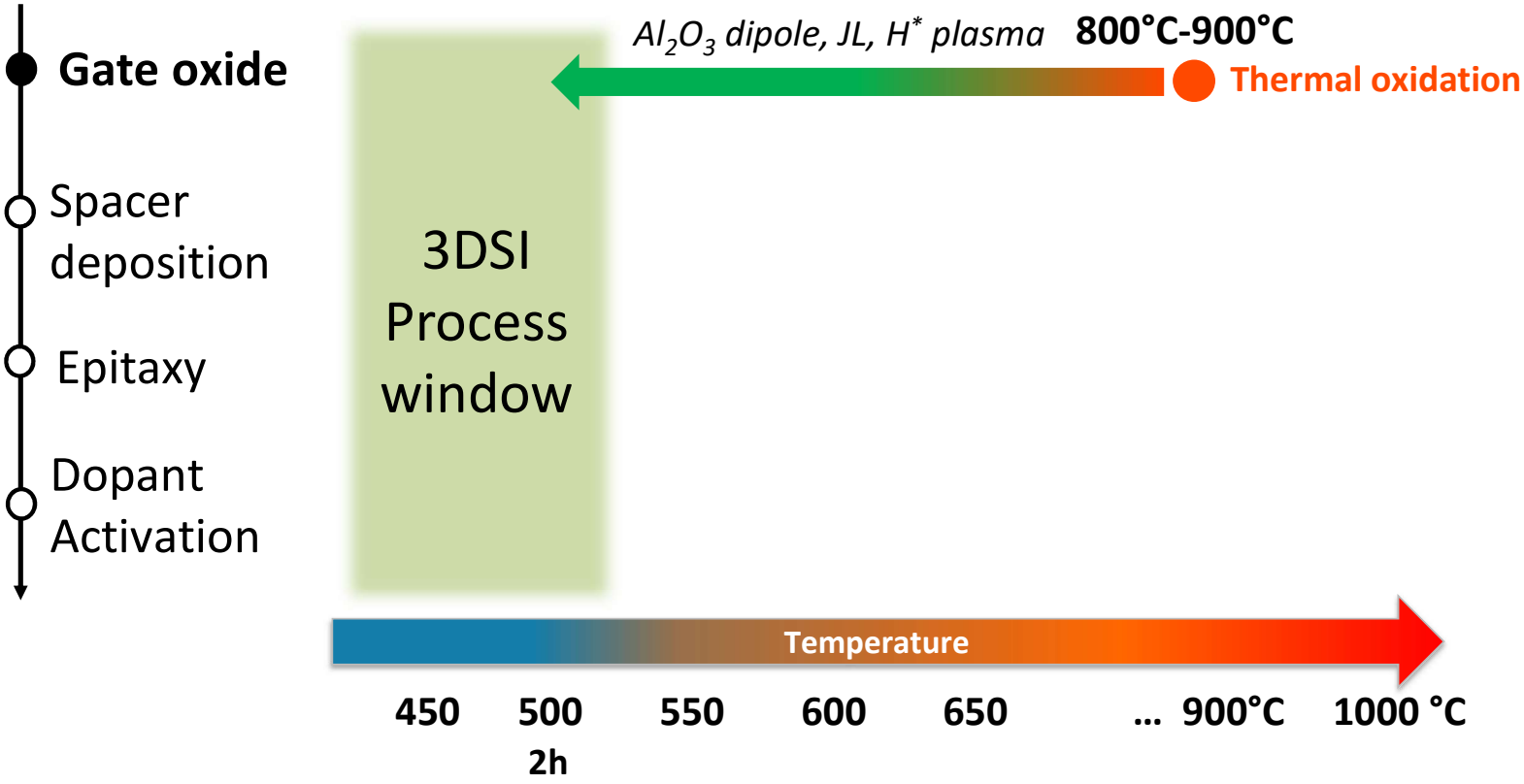


Highly-doped junctionless devices
Eox reduction in junctionless devices

J. Franco, VLSI 2018 (imec)

→Investigations path have been identified to meet NBTI reliability targets at 525°C

Summary on LT gate stack performance and reliability



→Reducing TB of the gate oxide at 500°C is challenging mainly because of NBTI concern
→But effective processes (dipole, H*plasma) can be used to achieve an efficient and reliable gate stack

Low temperature process for Top Tier

Gate oxide

Spacer deposition

Epitaxy

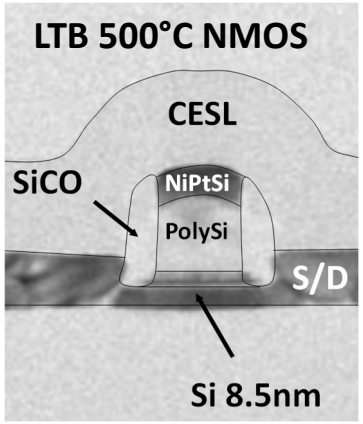
Dopant Activation

Al_2O_3 dipole, JL, H^* plasma **800°C-900°C**

Thermal oxidation

SiCO **630°C**

400°C **SiN**



Thin SiCO spacer 400°C

T. Mota Frutuoso et al., VLSI 2021 (Leti)

Temperature

450 500 550 600 650 … 900°C 1000 °C

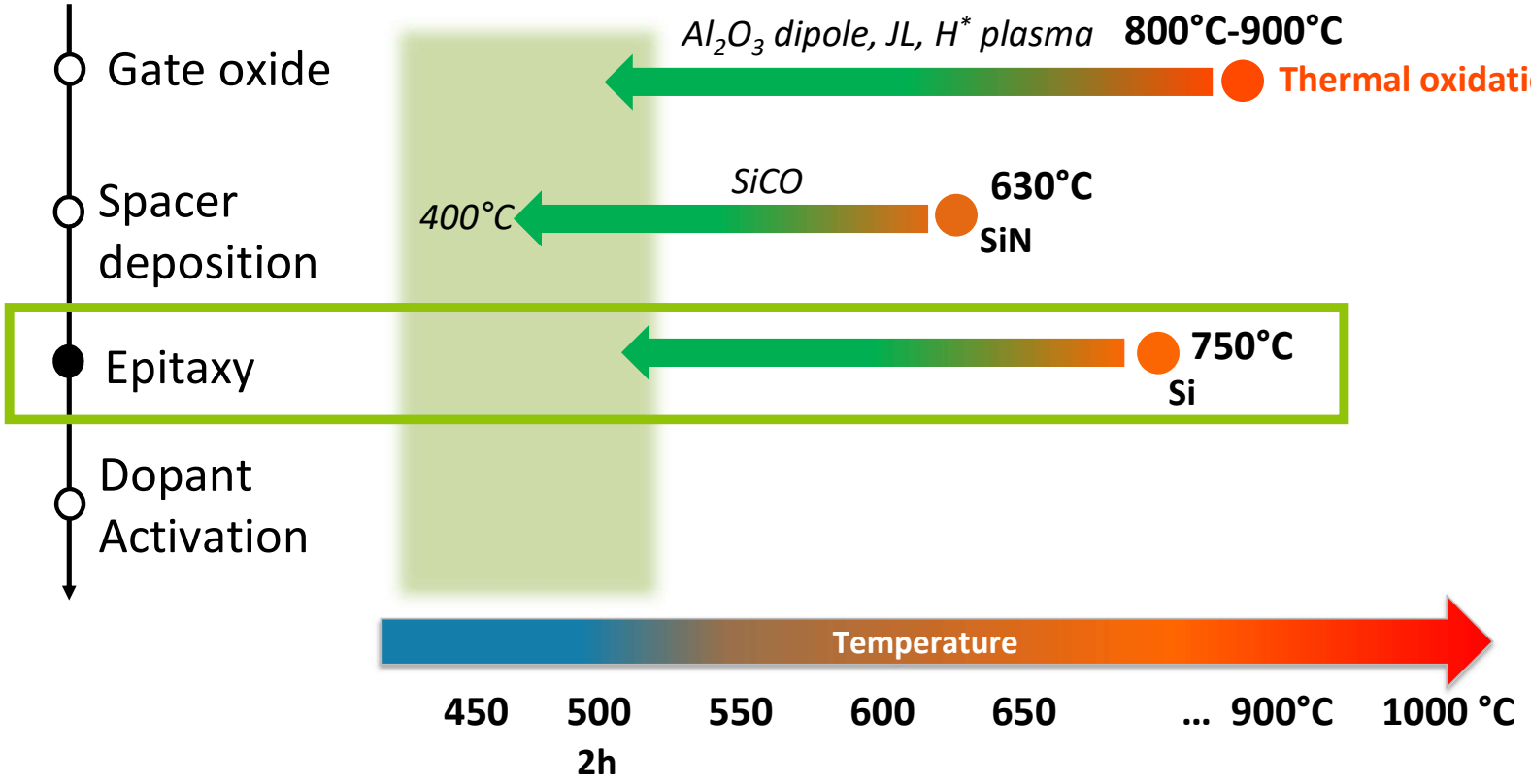
2h

→Low-k SiCO oxide deposited at 400°C can be used to replace 630°C SIN (see further)

Outline

- Introduction to 3D sequential integration
- Max thermal budget for the Top Tier
- Key process steps for a low temperature high performance 3DSi CMOS integration
  - Gate stack module
  - Junction engineering
  - Other processes required for RF applications
- Conclusion

Low temperature process for Top Tier



→New developments to reduce the temperature of the Si epitaxy to 500°C

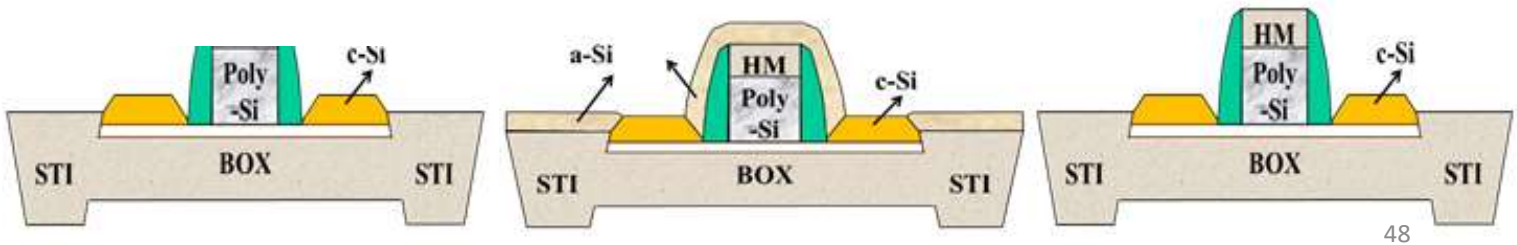
Low temperature epitaxy

	Standard selective Si epitaxy	≤500°C Si selective epitaxy
Surface preparation	HF last + bake (650°C and 800°C)	New strategy to be efficient at 500°C Siconi process removes surface oxyde / in situ clean prior to epitaxy
Deposition prescursor	DCS, SiH_4, Si_2H_6, and GeH_4	New precursors to obtain deposition rate of ~ 1nm/min at 500°C
Epitaxy process	Coflow recipe: dep & etch at the same time	Cyclic and Deposition Etch (CDE) Poly Si gates Hard Mask introduction

Selective Deposition

Non selective Deposition

Selective a-Si etching



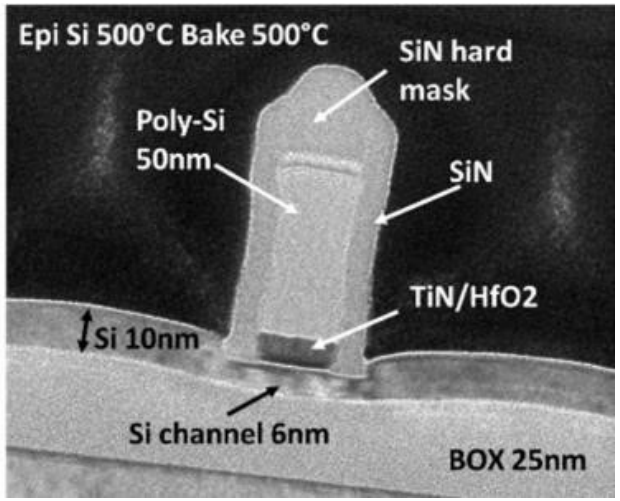
V. Mazzocchi et al., ECS 2018 (Leti, AMAT)

V. Mazzocchi et al., ECS 2018 (Leti, AMAT)

L. Brunet et al, IEDM 2018 (Leti, AMAT)

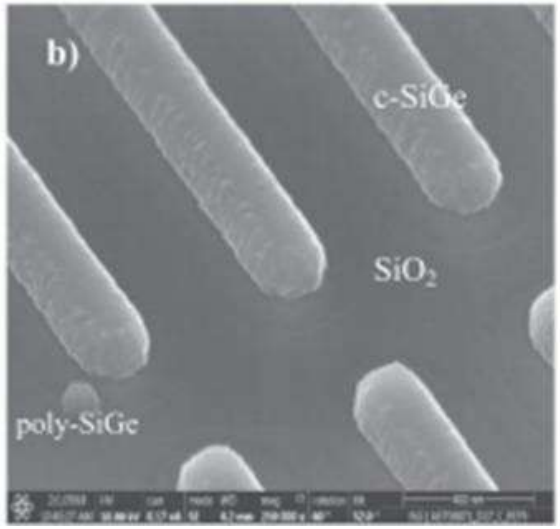
Low temperature epitaxy results

Si selective epitaxy



L. Brunet et al., IEDM 2018 (Leti, Applied Materials)

SiGe:B selective epitaxy

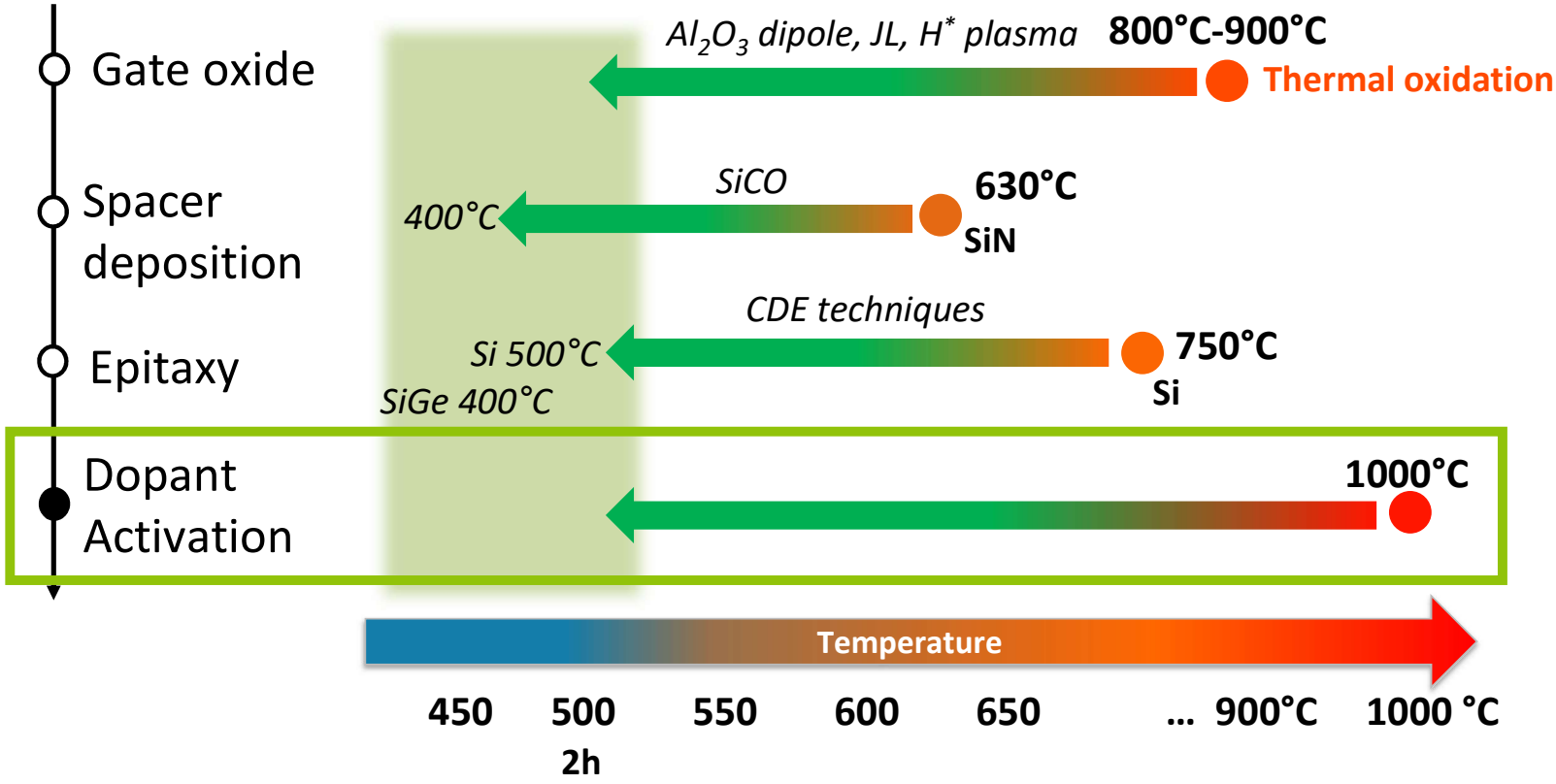


A. Hikavyy et al ., Semicond. Sci. Technol. 2019 (imec)

Si epitaxy at 500°C (including surface preparation) is demonstrated

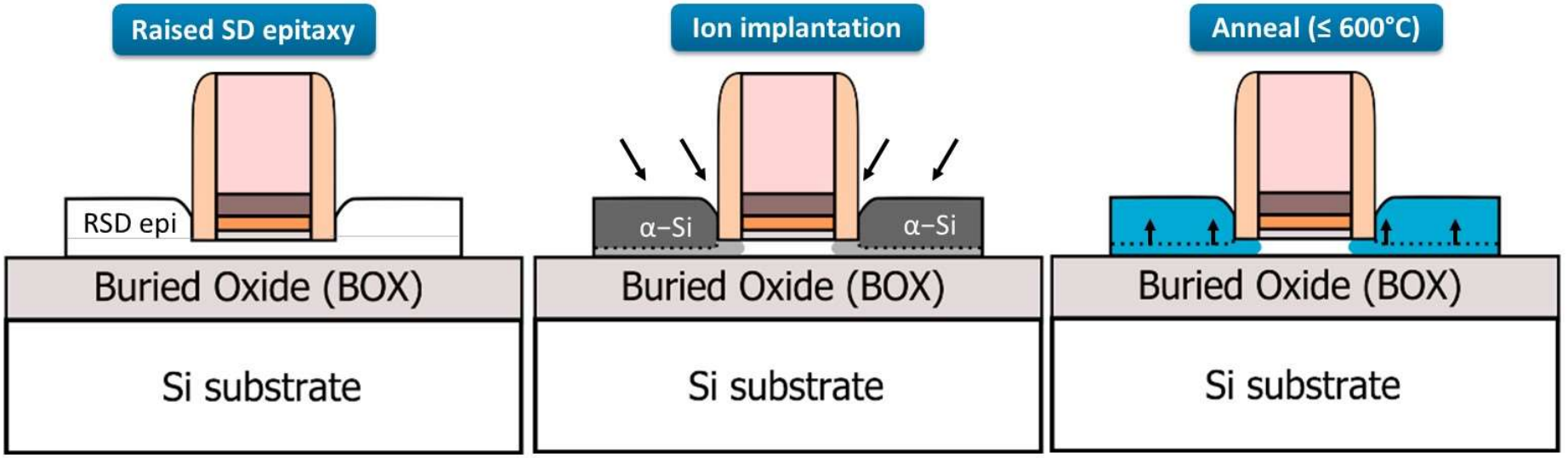
$Si_{0,3}Ge_{0,7}$:B & P epitaxy can be demonstrated at 400°C

Low temperature process for Top Tier



→New developments to reduce the temperature of the Si epitaxy to 500°C

Solid Phase Epitaxy Regrowth - extension last « Xlast »

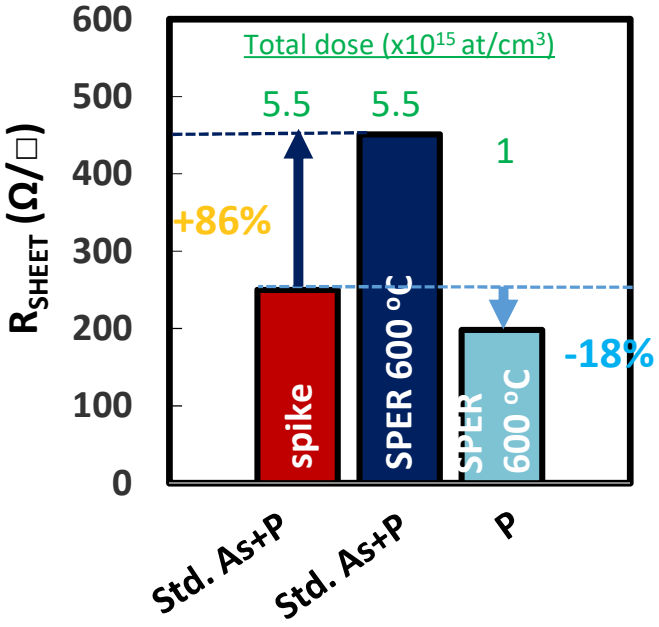


Amorphization

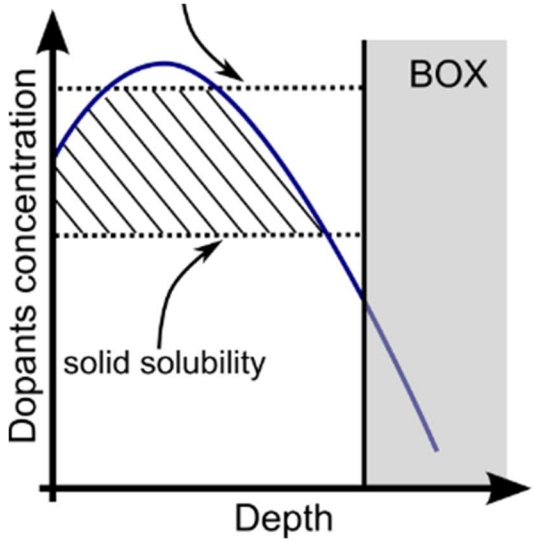
Solid Phase Epitaxy Regrowth (SPER):
→ Recrystallization
→ Dopant activation

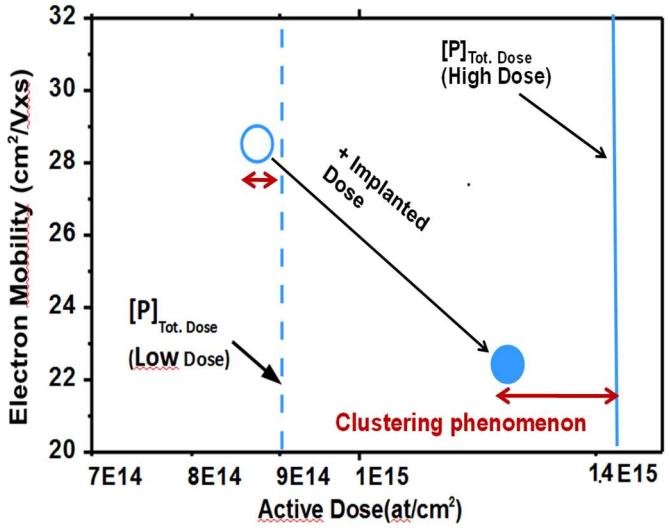
Junction formation→amorphization + SPER (450°C ≤ T ≤ 600°C)
Main issue : lateral diffusion under the gate (overlap)→Access resistance optimization
High activation only in recrystallized region→Minimize Tseed

SPER activation



L. Pasini et al., IWJT 2014 (Leti)

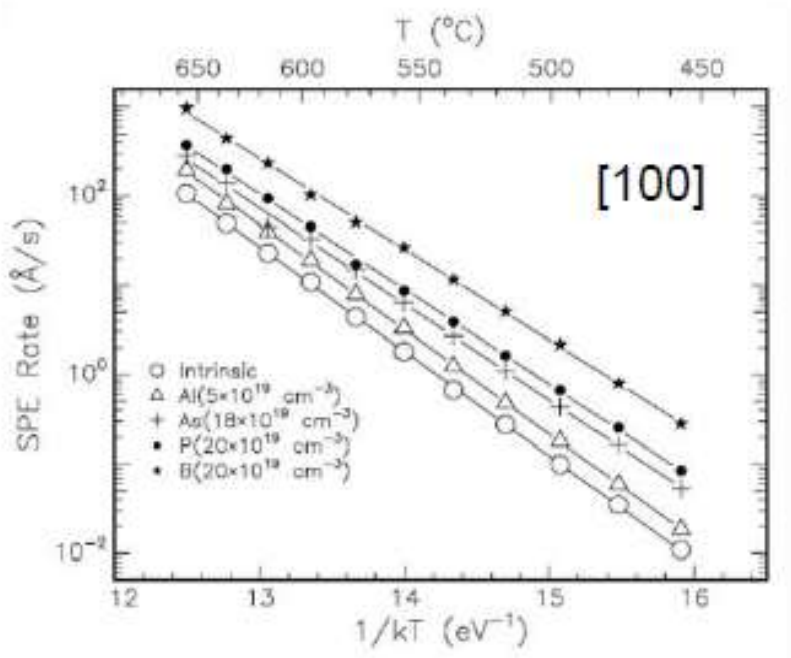




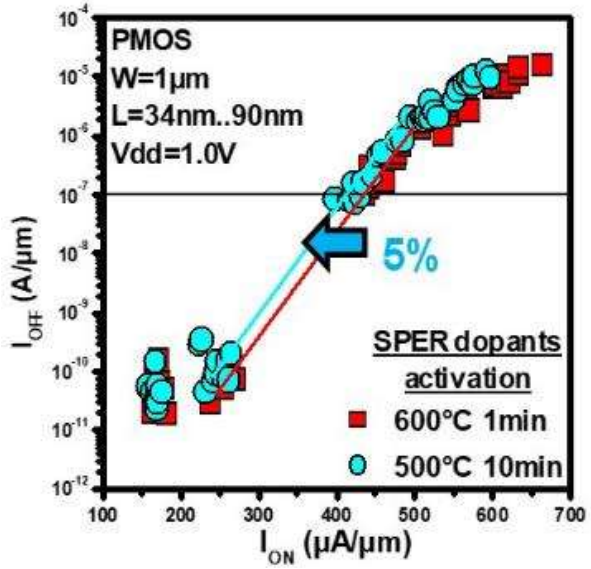
Doping profile need to be optimized due to weak diffusion & clusterization limit

$C_{Clusterization@\ 600°C}$ ~$3x10^{20}$ at/cm^3 for Boron and ~$6x10^{20}$ at/cm^3 for Phosphorous

Reducing SPER temperature



B-C. Johnson et al., Phys Rev B 2007

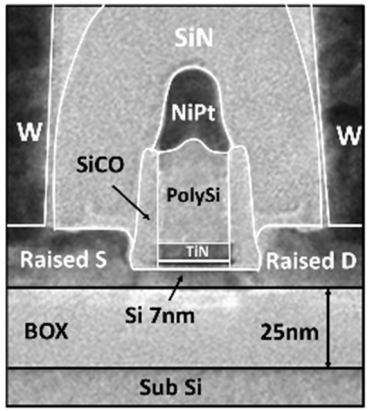


<100> oriented channel

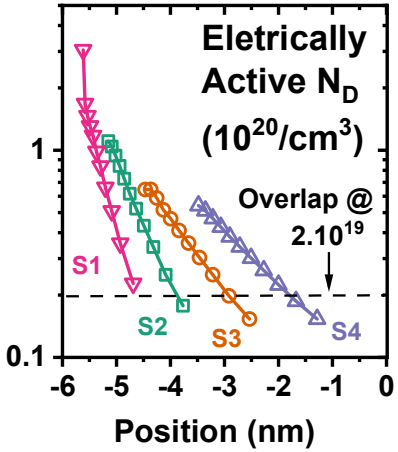
V. Lu et al., VLSI 2017 (Leti)

SPER rate depends on temperature, orientation, impurity type and concentration
SPER activation at 500°C validated on FDSOI devices

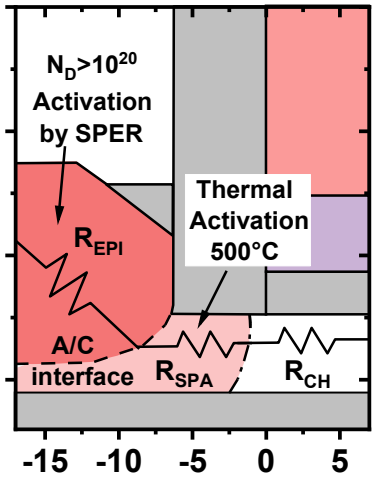
Junction optimization using SPER & Thermal Activation

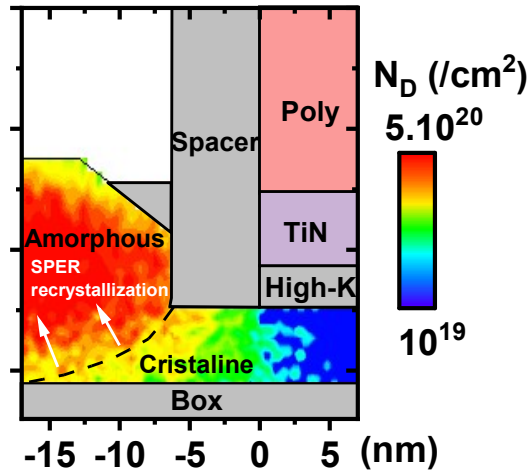


T. Mota Frutoso et al., VLSI 2022 (Leti)



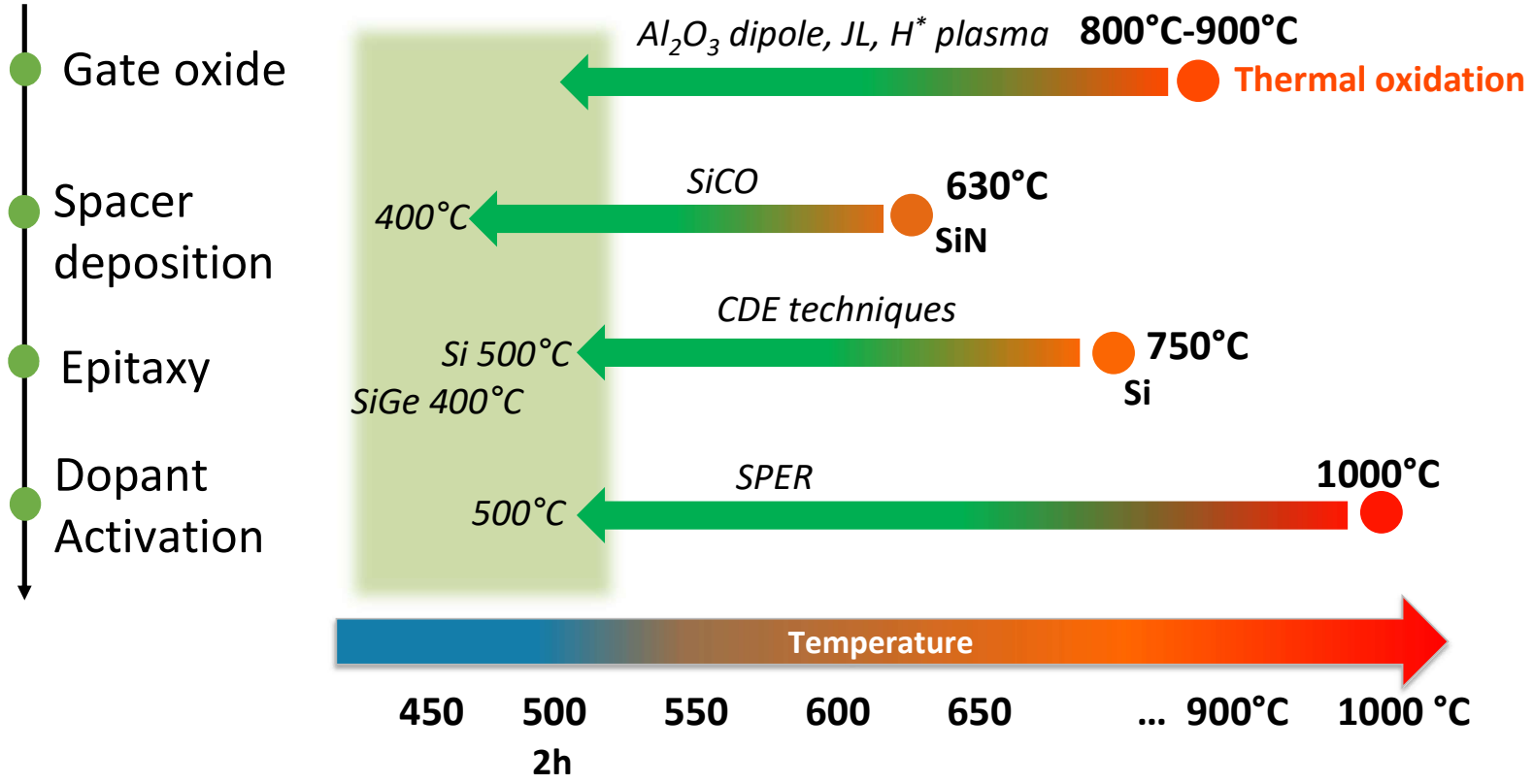
P imp.	Dose	Energy
S1	Low	Medium
S2	Medium	Low
S3	Medium	Medium
S4	Medium	High
S5	High	High





→Strategies to optimize junction profiles at T>500°C→ see student paper VLSI'22

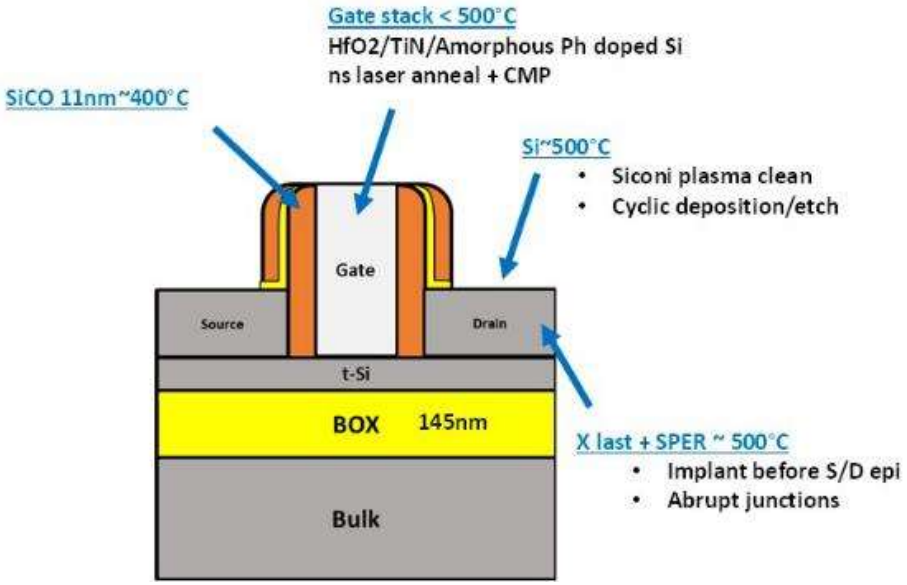
Low temperature process for Top Tier

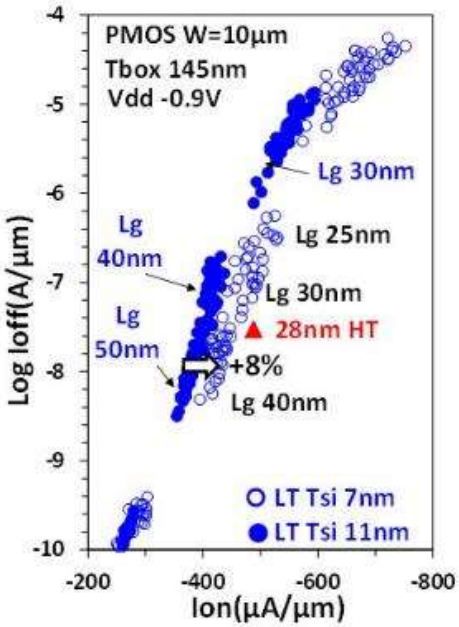


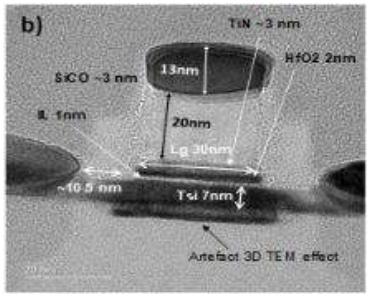
→New developments to reduce the temperature of the Si epitaxy to 500°C

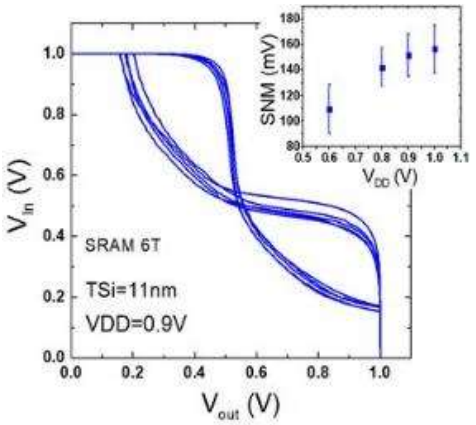
1st full 500°C CMOS FDSOI transistors

C. Fenouillet-Beranger et al., VLSI 2020 (Leti/Samsung)





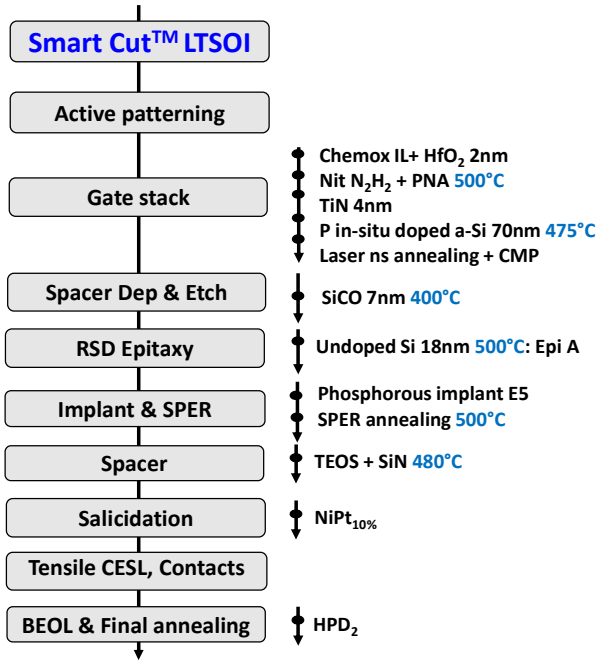




Full low temperature process for FDSOI devices ready
First functional CMOS FDSOI devices
RO and SRAM bitcell @ 500°C

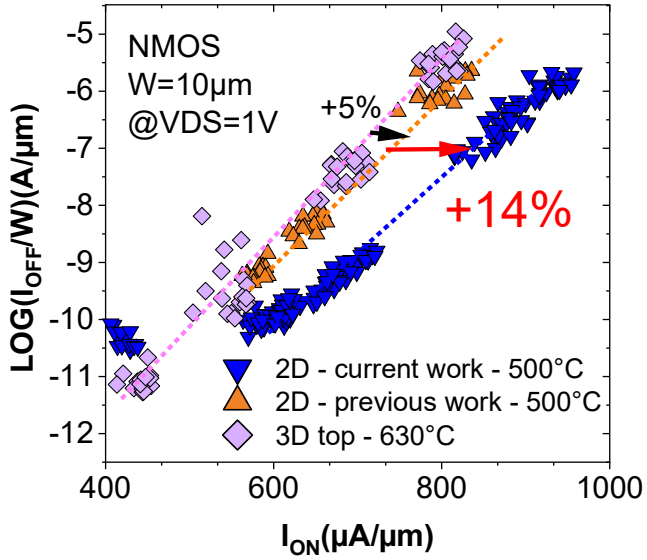
[Ref 28nm HT] N. Planes et al., IEEE VLSI 2012

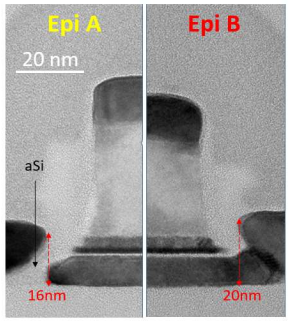
Full 500°C NMOS FDSOI transistors on LTSOI substrate

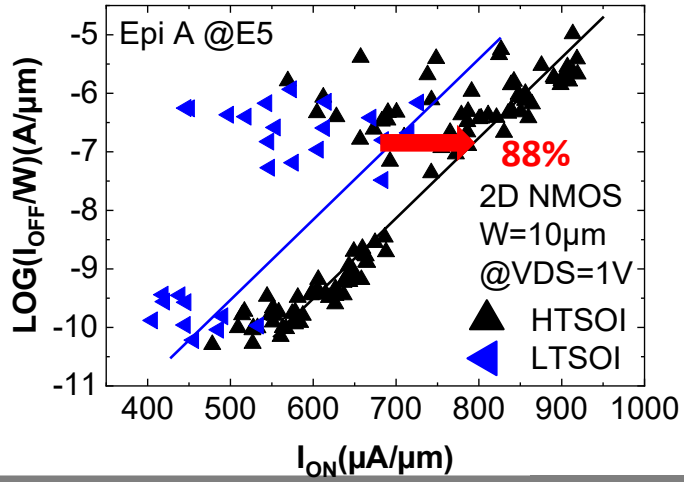


L. Brunet et al., IEEE VLSI 2021 (Leti)

Comparison to previous work







At equivalent RSD thickness & Implantation energy, optimized RSD epitaxy with less facet (Epi B) allows a clear yield & performance increase
LT integration on LTSOI at 88% of the HT substrate reference

Outline

- Introduction to 3D sequential integration
- Max thermal budget for the Top Tier
- Key process steps for a low temperature high performance 3DSi CMOS integration
  - Gate oxide
  - Junction engineering
  - Other processes required for RF applications
- Conclusion

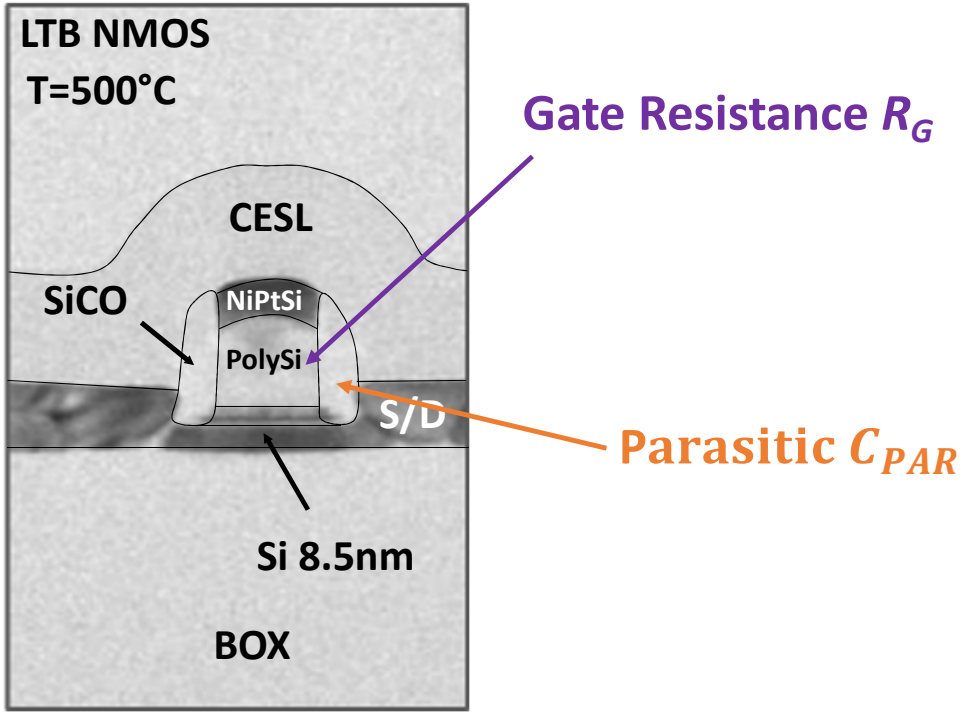
Other challenges for RF applications

RF FOMs

$$f_T = \frac{g_M}{2\pi \cdot C_{GG}} \propto \frac{1}{1 + \frac{C_{PAR}}{C_{OX}}}$$

$$f_{max} = \frac{f_T}{2\sqrt{R_G(G_{DS} + 2\pi f_T C_{GD})}} \propto \frac{1}{\sqrt{R_G}}$$

- also holds for dynamic operations in digital technologies



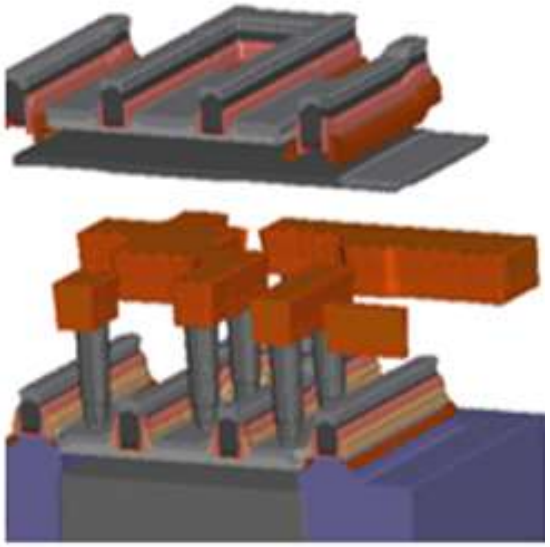
T. Mota Frutuoso et al., VLSI 2021 (Leti)

→Must find solutions to reduce R_G and C_{PAR} at low temperature <500°C

Gate resistance reduction using ns Laser Anneal

1200°C

Ex: Gate crystallization of the top tier

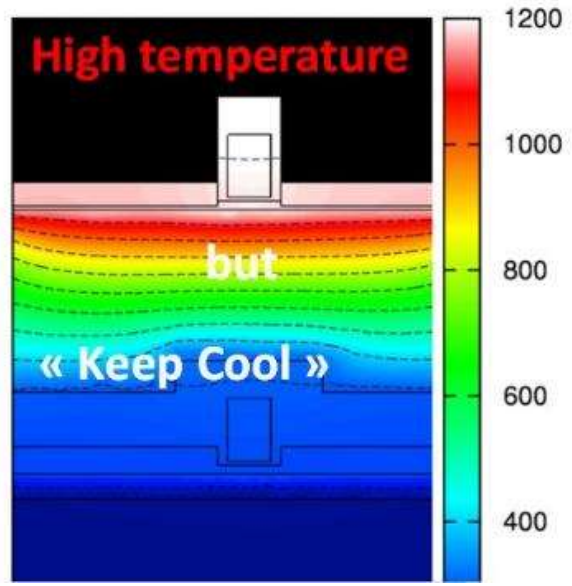


UV Nanosecond Laser Annealing (NLA)

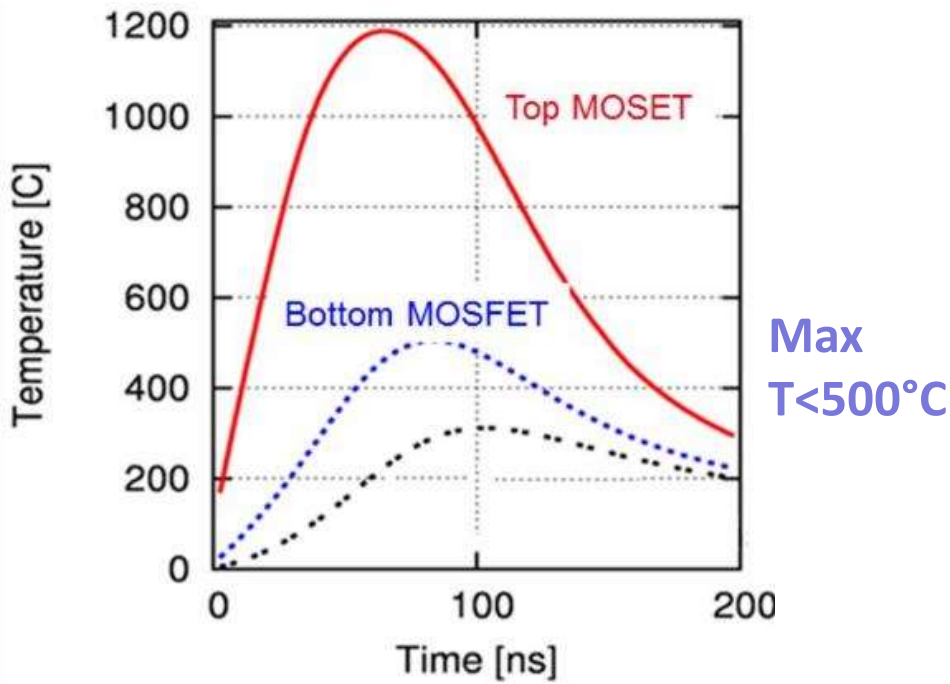
λ= 308 nm, 160ns pulse duration

L. Brunet et al, IEDM 2018; X. Garros et al., IEDM'19
S. Kerdiles et al, ECS Trans. 93, 2019.

Interest of ns Laser Anneal – Local Annealing



C. Fenouillet-Beranger et al., IEDM 2014 (Leti, SCREEN-LASSE)



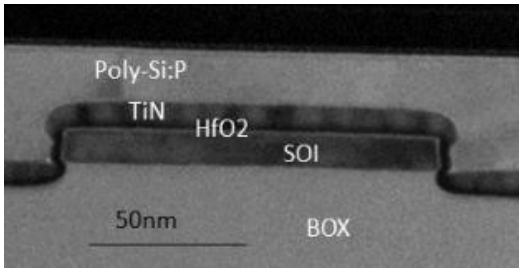
Max T<500°C

Main interest → preserves the stability of the Bottom Tier

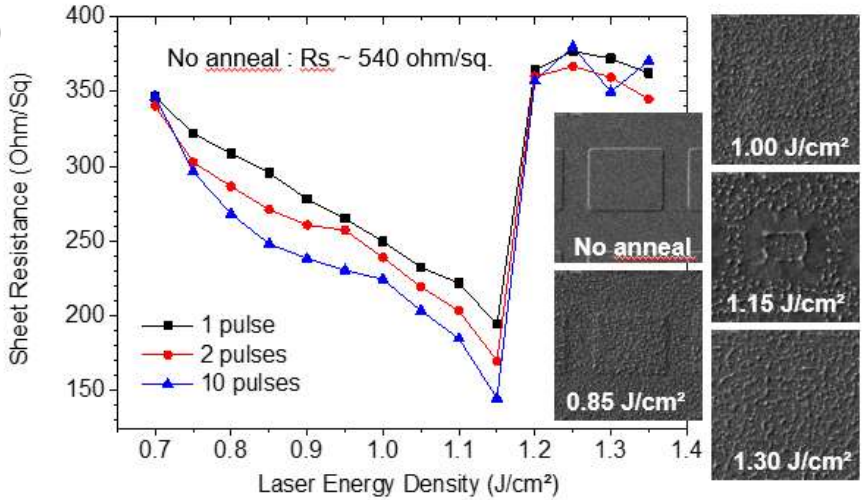
Local laser anneal with 1200°C on top layer and <500°C on bottom layer is possible
UV laser (308nm) / 100ns pulse / Standard Interlayer dielectric (SiO_2) thickness

Gate resistance reduction using ns Laser Anneal

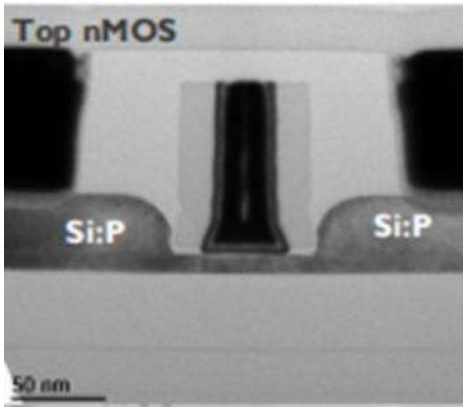
Amorphous in situ doped poly Si
melted by UV ns laser anneal
→ Dopant activation
→ Crystallization (100-300nm grain size)
→ Post CMP required



L. Brunet et al., IEDM 2018 (Leti)



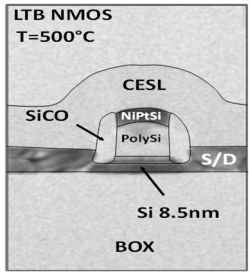
S. Kerdiles et al., ECS Trans 2019 (Leti)



A. Vandooren et al., VLSI 2018 (imec)

ns laser anneal is a potential solution for Poly gate stacks
Gate last process intrinsically offers low gate resistance

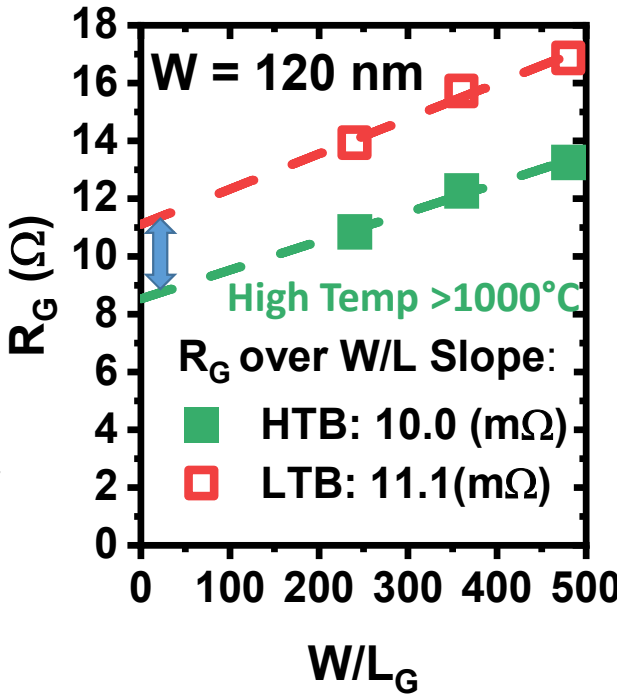
Gate resistance reduction using ns Laser Anneal



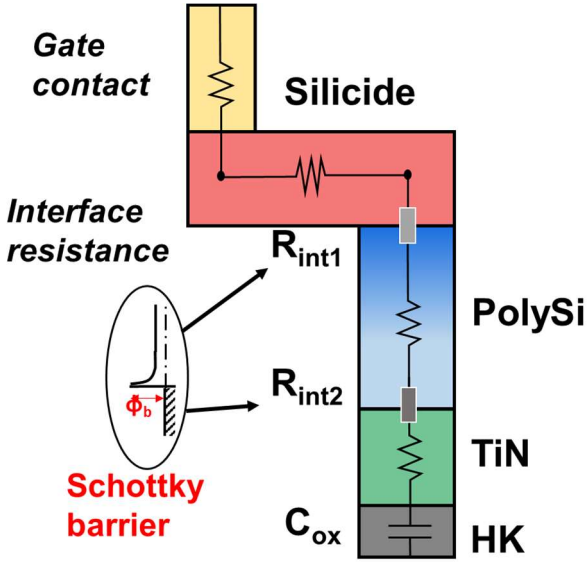
Same slope≈R_{PolySi}

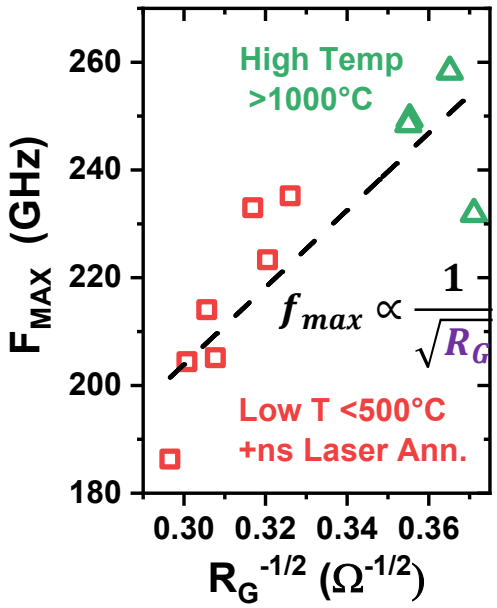
but ≠ Intercepts ≈R_{int}

Low Temp<500°C+Laser Ann



T. Mota Frutuoso et al., VLSI 2021 (Leti)



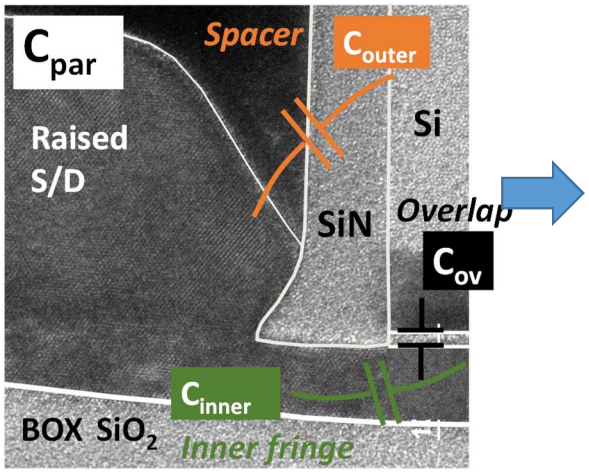


UV Laser anneal→allows to recover R_{PolySi} of HT references
→RF performance at T=500° close to HT references

Reduction of parasitic capacitances C_{par}

SiN spacer (630°C)

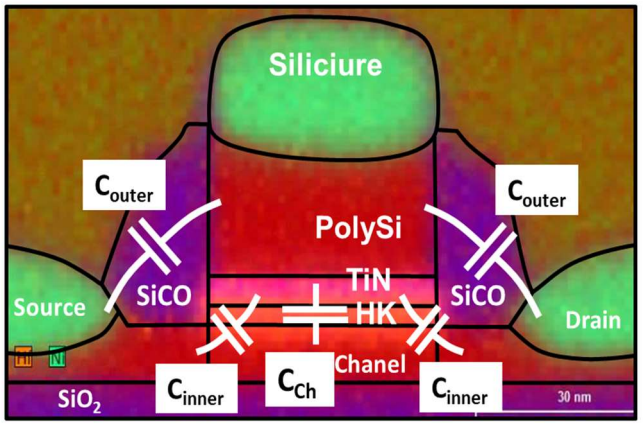
$\varepsilon_{r\,SiN}$ = 7.0



X. Garros et al., IEDM 2019 (Leti)

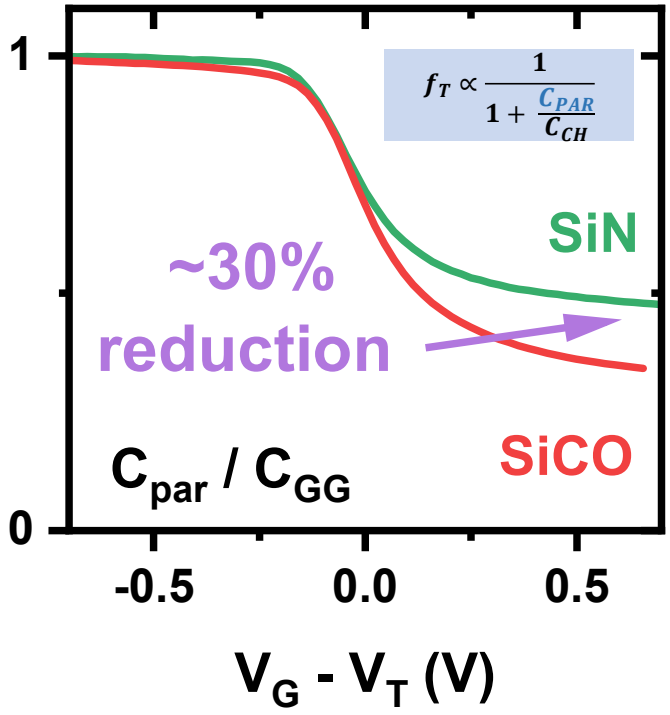
SiCO spacer (400°C)

$\varepsilon_{r\,SiCO}$ = 4.5



T. Mota Frutuoso et al., VLSI 2021 (Leti)

$C_{par}=C_{outer}+C_{inner}+C_{ov}$



→Replacement of SiN spacer by SiCO oxide deposited at 400°C

→Reduction of parasitic capacitance C_{par} of ~30%

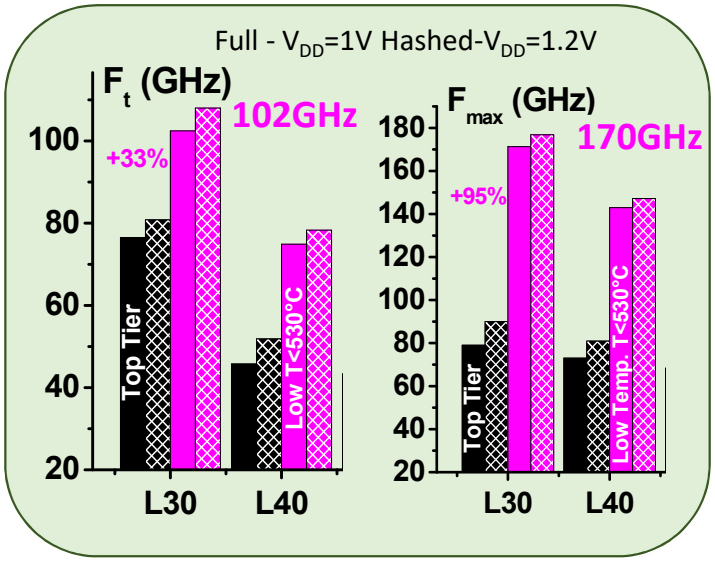
64

RF performance of Si-based Low Temp. transistors

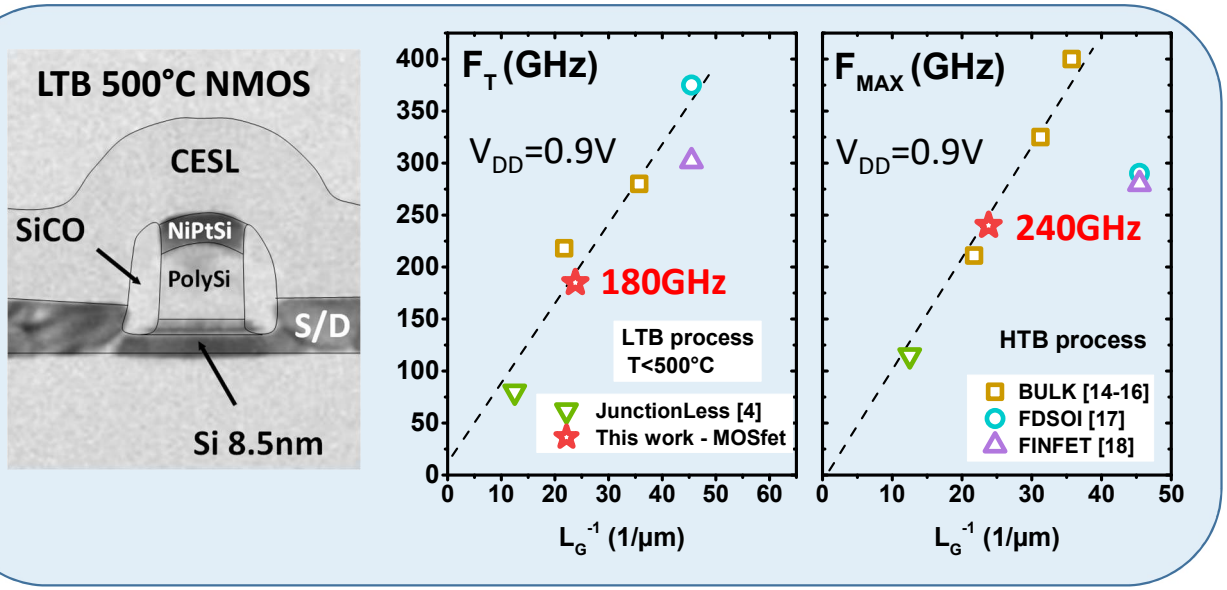
PMOS T<530°C

Digital

NMOS T=500°C



X. Garros et al., IEDM 2019 (Leti)



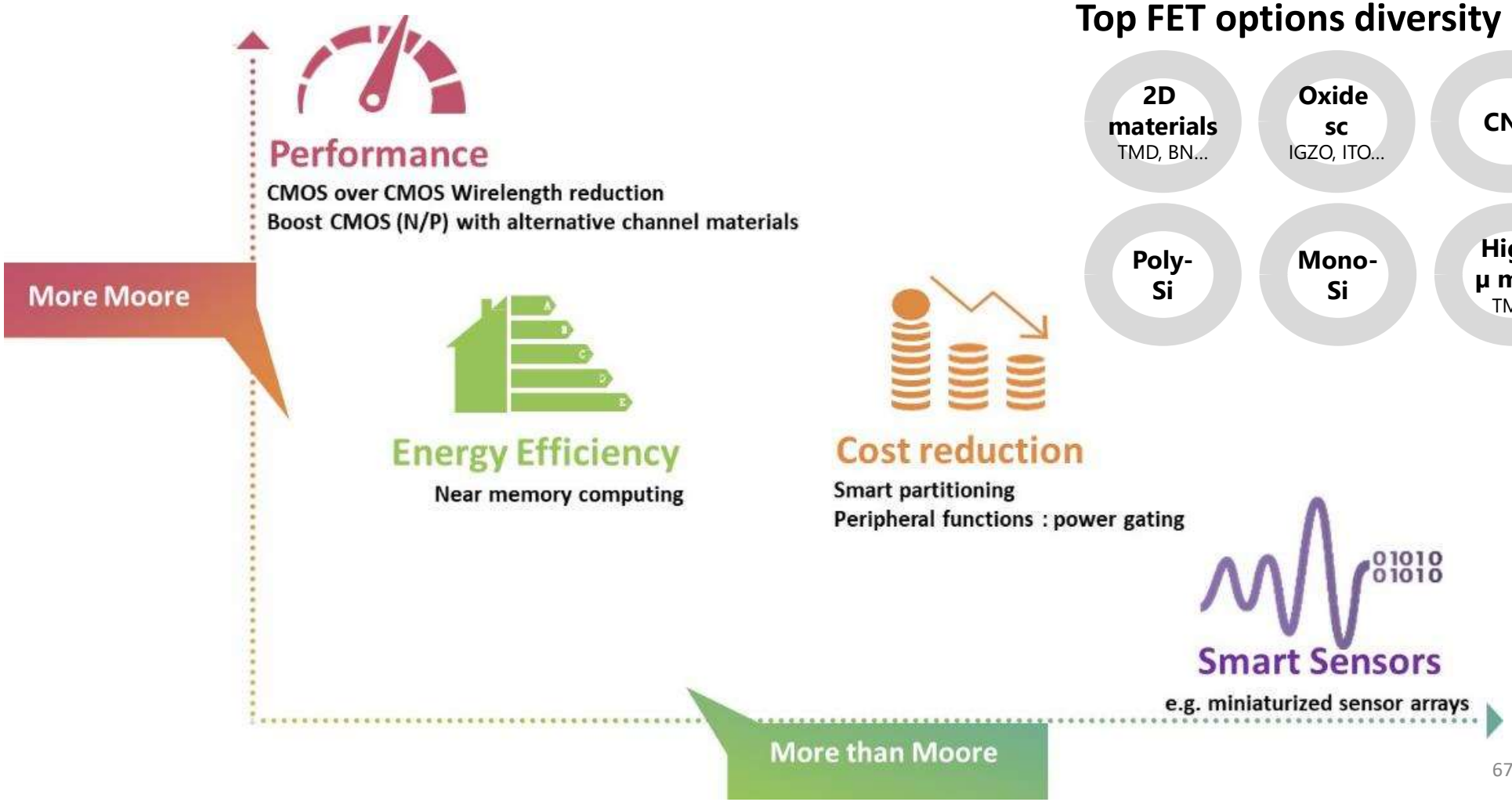
T. Mota Frutuoso et al., VLSI 2021 (Leti)

→Record RF performance for LTB technology, thanks to R_G & C_{par} reduction
→already equivalent to Si-based HT references at same Lg

Outline

- Introduction to 3D sequential integration
- Max thermal budget for the Top Tier
- Key process steps for a low temperature high performance 3DSi CMOS integration
  - Gate stack module
  - Junction engineering
  - Other processes required for RF applications
- Conclusion

3D sequential motivations



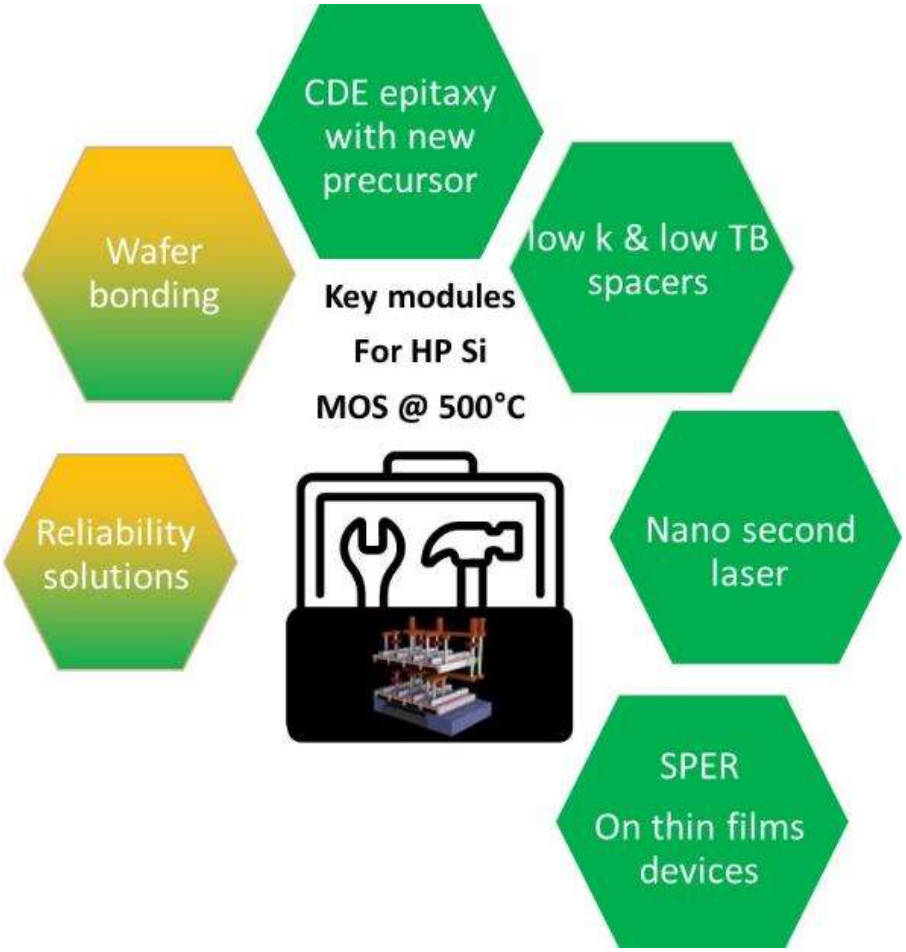
Top FET options diversity

- **2D materials** TMD, BN…
- **Oxide sc** IGZO, ITO…
- **CNT**
- **Poly-Si**
- **Mono-Si**
- **High µ mat.** TMD

Summary of LT process integration

- **LT 500°C tool BOX is ready and demonstrated**
- **300mm 3D Si mono demonstrated with great performance (DC and RF)**
- **Full Low temperature 500°C 3D sequential with Si mono still to be demonstrated :**
- **Low temperature gate stack reliability still the main issue but solutions envisioned**

	Introduction of Dipole between SiO_2 and HfO_2	Hydrogen treatment	J-Less transistor
NMOS	(Al_2O_3) ++	++	+ +
PMOS	(LaSiOx) ++	++	++



Thank you for your attention

Thank you to all co-authors and colleagues that have been working on CoolCube™

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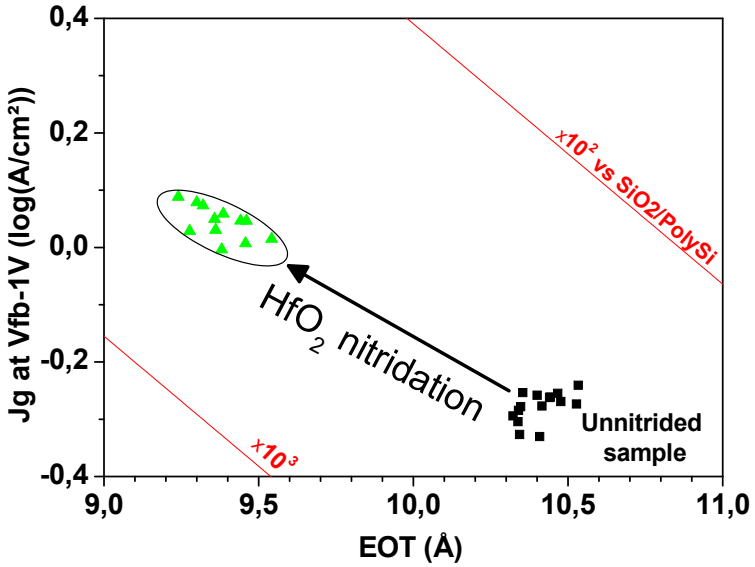
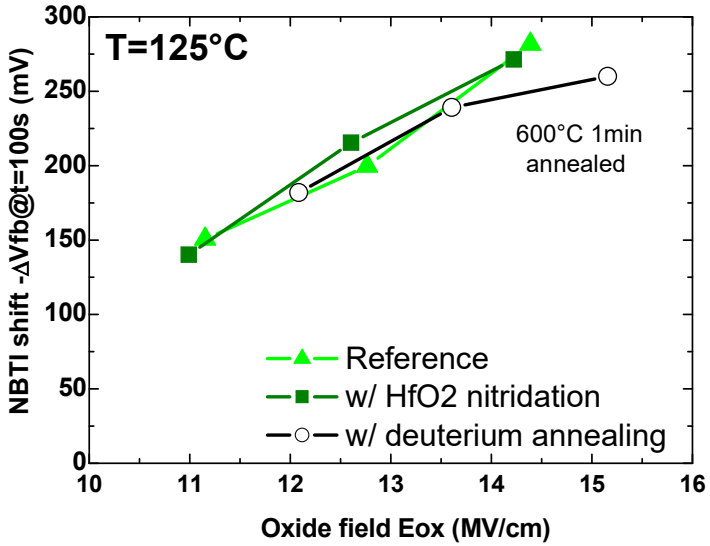
HfO_2 plasma nitridation for EOT reduction

HfO_2 nitridation in N2/H2 ambient at 250°C + PNA at 600°C 2min





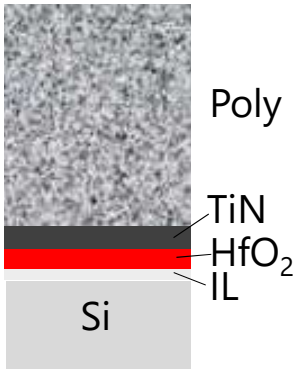
Plasma nitridation N2/H2

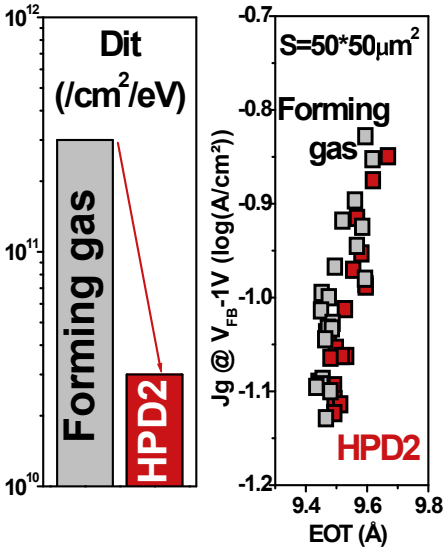
V. Lu et al., IEEE SISC 2015 (Leti)

→ Gain of ~1A EOT thanks to thinner IL with incorporation of N
→ But no NBTI reliability improvement

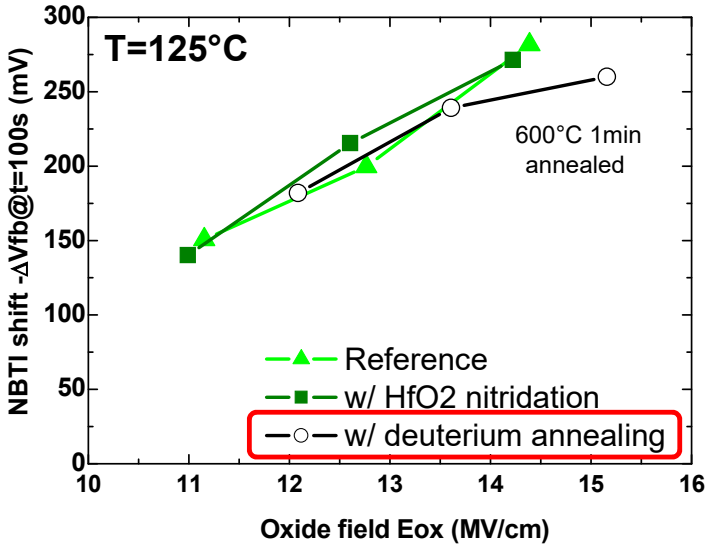
Forming gas Deuterium annealing

Digital device
LT gate stack





A. Tsiara IEEE VLSI 2018 (Leti)

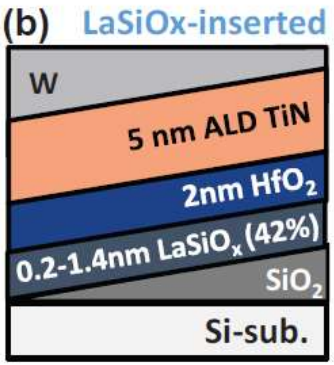


V. Lu et al., IEEE SISC 2015 (Leti)

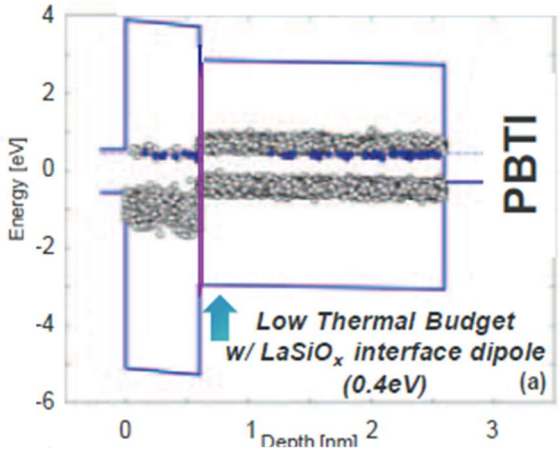
High Pressure Deuterium Anneal is efficient to heal interface traps on LT gate stack
→allows to reach LFN requirements but no NBTI reliability improvement

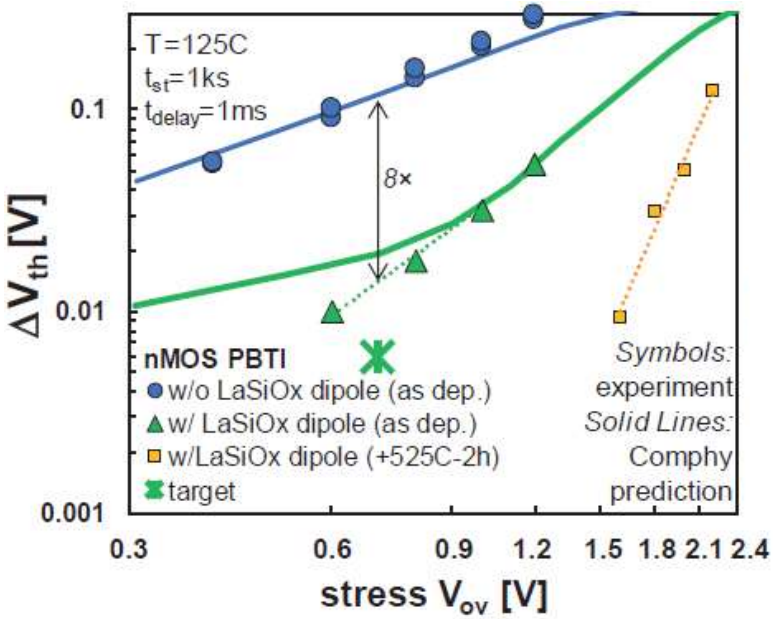
PBTI reliability solutions

LaSiOx Dipole insertion between SiO_2 and HfO_2



J. Franco, IEEE IRPS 2017 (imec)





J. Franco, IEDM 2018 (imec)

Up Shift of Vfb 0.4eV with LaSiOx for PBTI improvement
V_{TH} reduction

→Investigations path have been identified to meet NBTI reliability targets at 525°C