A D-band multi-channel Tx System-in-Package achieving 84.48 Gb/s with 64-QAM based on 45nm CMOS and low-Cost PCB technology

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***Abstract*— A high data-rate D-band transmitter module co-integrating a dual channel transmitter IC in 45 nm CMOS PDSOI technology and an antenna is presented. The proposed system-in-package is based on an innovative channel bonding technique and is fabricated using a low-cost printed circuit board process. The IC consists of two up-conversion chains including on-chip millimeter-wave local oscillator generators. The emitted signal is composed of eight channels, each one having 2.16 GHz bandwidth, organized in two sets of 4 channels at the IF band (around 61.56 GHz) that are up-converted to two adjacent sub-bands centered at 148 GHz. Then, the two sub-band signals are combined off-chip using a substrate integrated waveguide diplexer and radiated by a patch antenna array realized on the same package. The output spans from 139.3 to 156.6 GHz. The total equivalent isotropic radiated power is 8.3 dBm. A 84.48 Gb/s data rate is achieved with 64 QAM. The module consumes 600 mW from a 1-V supply and occupies a compact area of 12×6 mm^2.**

***Index Terms*— D-band, high data rate, front-end transmitter, 64-QAM, power amplifiers, LO generation, mixer, CMOS 45 nm**

I. Introduction

TRANSCEIVERS operating in the D-band (110-170 GHz) are key blocks to unleash high-capacity short-range wireless links providing data rates up to 100 Gb/s with moderately complex modulations schemes [1]-[8]. In this band, high-performance systems are often realized using III-V technologies. However, these technologies are not suitable for high-volume production of full transceivers, due to their high costs and usually large power consumption. On the other hand, lower cost D-band transceivers in CMOS technology suffer from lower output power and gain. A hybrid solution was presented in [8] where a CMOS transmitter is boosted by an external InP HBT PA to increase the output power. The use of the D-band spectrum is motivated by the availability of a large bandwidth that can be exploited to implement very high data-rate wireless links. Energy efficiency is also an important figure of merit, since this type of links will have to be deployed in small cells with limited DC power available. Therefore, appropriate circuit and module architectures to optimally balance the trade-offs between large bandwidth operation, acceptable output power and energy efficiency are crucial. At the module side, some of the previous works beyond 100 GHz use either low-efficiency on-chip radiating elements [2] or bulky stand-alone antennas [4]-[6]. Another aspect sometimes neglected in previous works is the local oscillator (LO) signal generation. The LO phase noise becomes a limiting factor for wideband high-order modulation. Most works in the literature use external high-performance LO generators. Realizing a high performance millimeter-wave (mmW) LO generator integrated on the transceiver chip is still an open issue.

In this work, a wireless transmitter is proposed with the aim to tackle the previously mentioned trade-offs. Figure 1 shows the proposed wireless transceiver, including a CMOS transmitter (TX) integrated circuit (IC), a diplexer and the antenna. In order to cover a large bandwidth at D-band, achieve good performance and reasonable power consumption while using CMOS technology, the TX leverages on channel-bonding techniques, so that only a fraction of the total bandwidth is handled by each channel. The proposed TX IC is composed of two up-conversion channels that are combined off-chip, at the

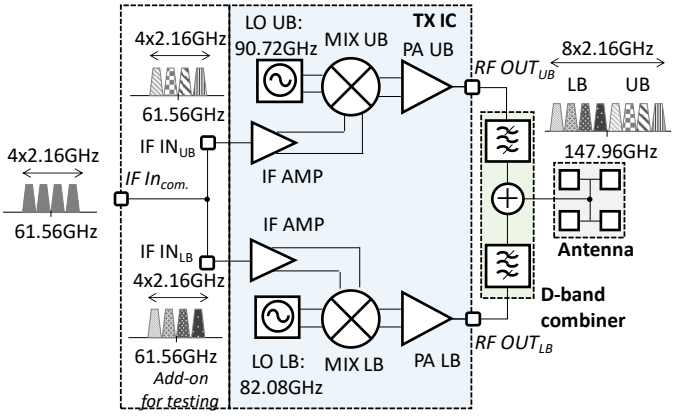

Fig. 1. Proposed TX module architecture and frequency plan.

This paragraph of the first footnote will contain the date on which you submitted your paper for review. This paper is an expanded version from the 2021 IEEE RFIC Symposium, Atlanta, GA, USA, June 7-9, 2021. This work was supported in part by Intel.

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module board. This architecture imposes an additional constraint, since multiple mmW LO signals are required. However, by using innovative frequency generation techniques based on frequency multiplication [9], the required multiple LO signals can be efficiently generated on-chip from a common signal at a much lower frequency. In this work, each of the two transmit lanes includes its own LO generator. The concept of channel bonding is extended to the intermediate frequency (IF) band that is centred around 61.56 GHz. The input of the two TX lanes is found at the same IF band, which is expected to be provided by a baseband to V-band channel-bonding up-converter (not covered in this paper). The IF signals are hence composed of four channels of 2.16 GHz.

Reducing the cost of the overall transmitter is also a primary goal of this work. The TX IC is mounted on a low-cost multilayer printed circuit board (PCB) comprising a substrate integrated waveguide (SIW) diplexer that implements the channel bonding operation, and a 2×2 patch antenna array that provides a moderately high gain (10 dBi as in [10]) in a small area. Actually, this TX module is intended to be used as the feed of a transmitarray antenna [11] to reach the high gain required for medium range D-band point-to-point links [12].

A data-rate of 84.48 Gb/s with multi-channel single carrier 64-QAM is demonstrated over-the air by combining the proposed transmitter module and a commercial D-band down-converter receiver.

This paper is an extended version of [13] presented at the 2021 RFIC Symposium. The paper is organized as follows. In Section II, the TX IC is presented with a detailed description of each of the sub-blocks: LO generation, IF section and power amplifiers (PA). Section III covers the TX system-in-package module with specific sub-sections describing the power combiner, the antenna and some test fixtures used to separately characterize each building block of the module. Section IV presents the experimental results obtained with the proposed transmitter module. Conclusions are drawn in Section V.

II. TX Integrated Circuit

The TX IC is a two-channel up-converter based on the work of [14] with improved PAs and IF section. Channel-bonding is first implemented for the IF input signal. It is composed of 4 baseband (BB) channels of 2.16 GHz up-converted around 61.56 GHz, each one conveying 1.76 Gsymbols/s. The second channel-bonding step is realized by up-converting and combining the two sets of 4 channels at IF into two adjacent sub-bands at D-band, namely, lower band (LB) and upper band (UB). Compared to [14], in this work, the power combining operation is performed off-chip. This architecture enables a total of 2×4×1.76 GHz×6 bit/symbol = 84.48 Gb/s, using single- carrier 64-QAM on each channel. The two IF signals are up-converted to the LB and UB using a couple of mixers and dedicated LOs operating at 82.08 and 90.72 GHz, respectively, as shown in Fig. 1. These LOs are generated from a common 4.32 GHz reference input using integer frequency multiplication by 19 and 21, respectively. Next, the LB and UB signals are separately amplified by two different power amplifiers (PAs). The spectrum of the resulting aggregated signal ranges from 139.32 to 156.6 GHz.

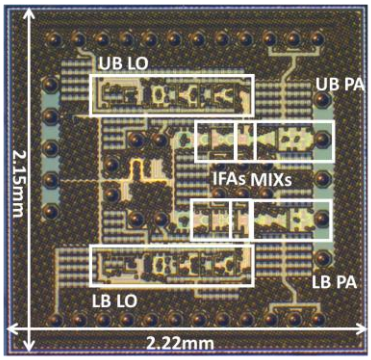


Fig. 2. TX die photograph.

The two required intermediate frequency (IF) inputs are connected to the same pad for testing purposes in the fabricated TX IC prototype. Fig. 2 shows a die photograph of the TX IC in 45 nm CMOS PDSOI. The total circuit area is 4.8 mm^2 including IOs, on-chip biasing and a SPI digital interface for bias control. All transistors in the circuit, if not otherwise stated, are 40-nm long and have finger-width of 1 µm. The total width is shown on the schematics of Fig. 5-Fig. 7. Wherever neutralization technique is applied, NMOS capacitors with half the size of the main NMOS transistors are used. All transformers are realized with the uppermost thick metal layers.

A. LO generation sub-block

Low phase noise mmW signal generation is very challenging. Classically, mmW LO signals are generated using PLLs integrating a high frequency VCO at the required LO frequency, but the phase noise degrades faster than 20log(f) with increasing VCO frequency (f). This is due to the reduced quality factor of the VCO passive components at mmW frequencies. An alternative is to realize the LO generator with somehow lower frequency PLL followed by integer frequency multiplication. In this work, a technique inspired by this principle is used. It starts from a significantly lower frequency PLL at 4.32 GHz that is internally multiplied by high integer factors (19 and 21) to obtain the two required LO signals of 82.08 and 90.72 GHz. The principle of operation of this technique was presented in [9] and extended to multi-LO generation in [15]. The frequency multiplication operation is done in three steps as shown in Fig. 3. First, the low frequency sine-wave reference signal is transformed into a square duty-cycled signal by a duty cycle controller (DCC). To do that, a 50

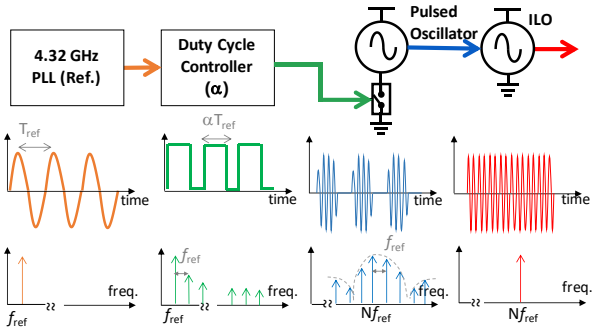


Fig. 3. Bloc diagram of the frequency multiplication technique using a pulsed oscillator and injection locked oscillators (ILOs).

Ω input impedance comparator is used. It provides a square signal with f_{ref} frequency and a duty cycle of α ($\alpha \in [0,1]$) from the sinusoidal input signal. The duty cycled signal switches on-and-off a pulsed oscillator by acting on its current source. The pulsed oscillator is designed to operate at f_{FO} close to the desired mmW LO frequency (82.08 or 90.72 GHz, depending on the TX lane) when operated continuously on, as a free-running oscillator. Switching on-and-off, the oscillator creates a pulsed signal that is constituted by a periodically repeated oscillations train (PROT). The PROT signal spectrum has harmonic terms at large integer multiples of f_{ref}, as shown in Fig. 3. The third step consists in selecting one of the harmonic terms of the PROT signal spectrum that is found at the integer *N* multiple of f_{ref}. This is done using an injection locked oscillator (ILO) that is tuned to a free running frequency near the desired *N*-multiple of f_{ref}. The rejection of adjacent terms around the desired *N*-multiple of f_{ref} can be improved by using a second ILO (ILO2) tuned like the first one (ILO1), as shown in Fig. 4. Thus, the resulting output signal is a pure sine-wave signal that copies the phase and frequency characteristics of the reference signal multiplied by *N*.

The schematic of the LO generation building block is shown in Fig. 5. The input signal of 4.32 GHz (REF IN) feeds the gate of a transistor in the source network of a SPO. This transistor acts as a switch to turn on and off periodically the oscillator. The SPO is based on a gyrator oscillator. The other admittances connected to the SPO main transistor drain, source and gate nodes are sized to set its self-oscillation frequency (SOF) around the desired LO frequency. For SOF tuning purposes, a varactor is used at the source of the SPO main transistor. It has to be noticed that the LO frequency does not depend on the varactor value nor the SOF of the SPO. The SPO varactor is hence used to adjust the centre of the spectral envelope of its multi-harmonic output signal, rather than the location of the harmonic terms that are exact integer multiples of the REF IN signal frequency. A single-ended cascode buffer with a balun load is inserted between the SPO and the next stage that comprises an ILO based on a cross-coupled LC tank oscillator. An inter-stage pseudo-differential common source buffer follows it. The ILO has a varactor in its resonant tank to tune its selectivity curve close to the desired SPO output harmonic frequency. The first ILO stage is followed by a second identical stage for further LO spurs suppression. An output buffer consisting on a pseudo-differential cascode stage is used to increase the LO power provided to the mixer. Both LB and UB LO generators have the same structure and active device sizes, differing only in passives and varactor values.

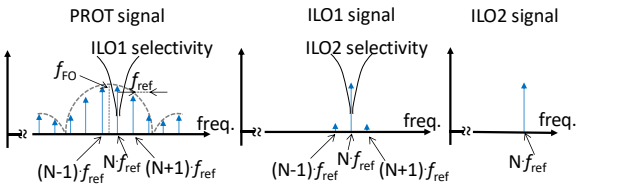


Fig. 4. Frequency domain PROT signal and ILOs outputs after locking on the N-th harmonic of the f_{ref} injection frequency.

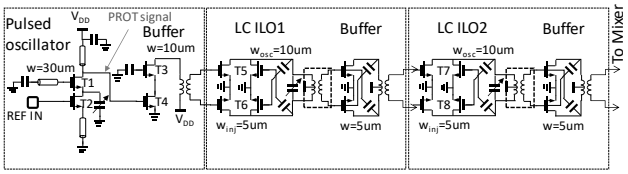


Fig. 5. LO generation circuitry

B. IF section

Figure 6 shows the IF sections and mixers circuitry. The LB and UB mixers are equal except for the loading transformer. They comprise a double balanced Gilbert cell with PMOS current bleeding. The first stage of the IF amplifier is sized differently in LB and UB to equalize the overall gain for the two bands and compensate for the lower PA gain in the UB. The combined mixer and IF section simulated conversion gain is shown in Fig. 6, right, as a function of the mixer output frequency. The figure also shows the input splitter used to obtain the IF signal for each of the TX IC lanes from the common IF input pad. This add-on is only for testing purposes.

C. D-band PAs

Figure 7 shows the circuit schematic of the LB and UB PAs. They consist of four stages of common source pseudo-differential cells with 4-ways combining technique, from the third stage for the LB PA and from the second stage for UB PA. This method is used to increase the output power of the PAs. The differential signal from the first stage of LB PA and the second stage of UB PA are divided into two differential signals, using a 4-way transformer-based splitter. The output 4-way transformer combines the power of the four last stage signals and converts them to single-ended mode. In order to ensure the stability of the PAs and enhance their reverse isolation, a cross-coupled capacitive neutralization technique is used. The passives are sized differently in the LB and UB PAs. The LB and the UB PAs simulated gain at 1-dB compression point are 13.2 dB for the LB at 143 GHz, and 12.2 dB for the UB at 153 GHz.

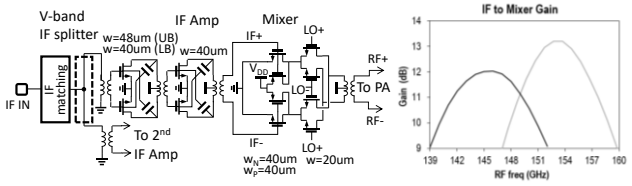


Fig. 6. IF section schematic (left) and simulated conversion gain from IF input to mixer output (right).

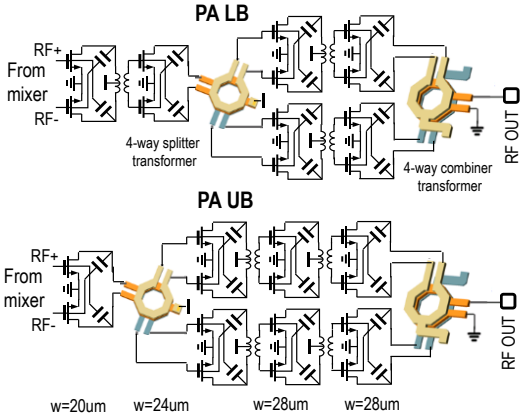


Fig. 7. PAs circuit schematic.

III. TX MODULE: BUILDING BLOCKS AND INTEGRATION

The proposed system-in-package is composed of the previously described CMOS TX IC in 45-nm PDSOI technology, a SIW diplexer, and a 2×2 patch antenna array, as shown in Fig. 8. The LO reference (REF IN) and IF signals are provided using an SMA and a V-band edge-launch connector, respectively. The IC is flip-chipped on the top-side of the PCB using C4 micro-bumps. The stack-up of the module board comprises two 127 µm-thick Astra MT77 layers with double-side Cu-metallization (18 µm) and a 128-µm thick bonding layer, as shown in Fig. 9. The nominal permittivity and loss tangent of the substrates are 3 and 0.0017 at 20 GHz, respectively. The minimum conductor width and spacing are 75 µm. The TX module size is 12×6 mm^2, and the total test board size, including bias and input lines, is 80×57 mm^2.

The two IC output signals (LB and UB) are delivered to the diplexer using microstrip transmission lines (TL) followed by a transition to SIW (see Figs. 8 and 10). The multiplexed signal excites a 2×2 array of aperture-coupled patches at the bottom-side of the PCB. The design of each passive component and their characterization is detailed in the next sub-sections.

A. *On-board D-band Diplexer*

The two D-band signals (LB and UB sub-bands) at the output of the IC are combined on the PCB using an SIW diplexer [16]. It consists of two SIW passband filters operating at two adjacent bands and a combiner based on an asymmetric T-junction, as shown in Fig. 10. The two LB and UB filters are sized differently to operate around 143 GHz and 152 GHz, respectively. The filter at each input rejects the opposite input sub-band signal and improves isolation. The T-junction is based on SIW feedlines to reduce the insertion losses and perform the combination of the filtered signals. The SIW structures are realized between layers m1 and m2 using 80 µm diameter vias (via1 of the PCB stack-up shown in Fig. 9). Stand-alone versions of the filters and diplexer have been characterized using on-wafer probes and a vector network analyzer with D-band extenders. Figure 11 shows the measured S-parameters of the filters. The S_{21} of the LB filter achieves a maximum value of -1.9 dB and exhibits a large -3-dB bandwidth of 21 GHz, between 134 GHz and 155 GHz. The UB filter shows a maximum S_{21} of -2.8 dB with a -3-dB bandwidth larger than 22 GHz. The measured S-parameters of the diplexer are shown in

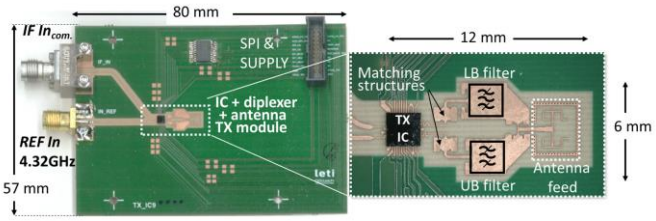


Fig. 8. Realized TX system-in-package.

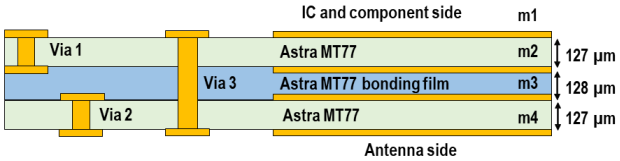


Fig. 9. Stack-up of the module board.

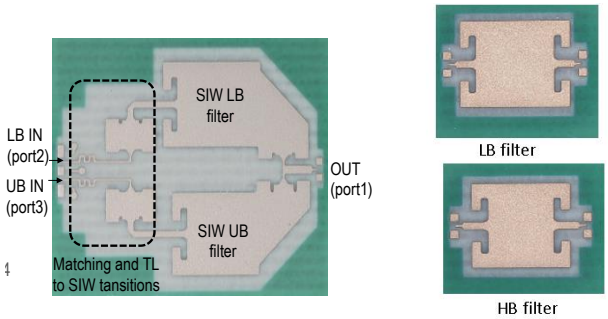


Fig. 10. Photographs of the diplexer and associated filters.

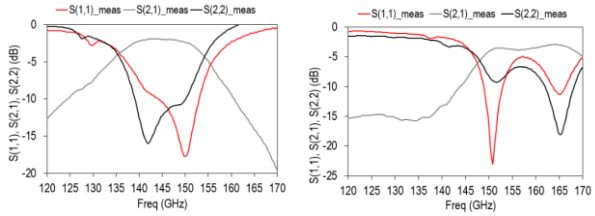


Fig. 11. Measured frequency responses of the LB and UB filter.

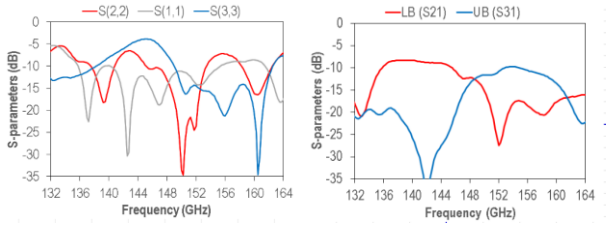
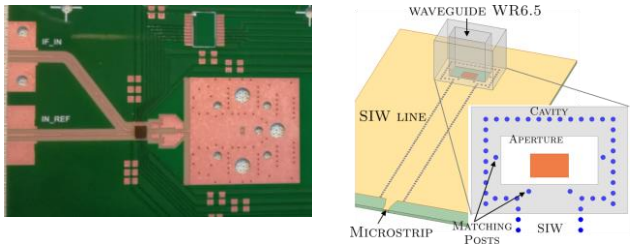


Fig. 12. Diplexer reflection (left) and transmission (right) coefficients.

Fig.12. A good matching at each port of the proposed diplexer can be observed on the return loss curves. The measured S_{21} shows an insertion loss of about 9 dB for the LB channel at 143 GHz. From the S_{31} curve, we can see that the UB channel has an insertion loss of 11 dB at 152 GHz. The UB filter in the diplexer has slightly lower performance than the LB filter. This is attributed to the increase of the losses in the substrate at D-band and to a more relevant impact of fabrication tolerances.

B. *Testing fixtures and module integration*

A dedicated board (see Fig. 13a) was designed to characterize the power delivered to the antenna, i.e. at the output port of the diplexer, by the TX IC. To this end, the antenna was replaced by a transition from microstrip line to a standard D-band rectangular waveguide (WR6.5), orthogonal to the board. The transition comprises in turns two transitions, as illustrated in Fig. 13b. The first converts the quasi-transverse electromagnetic (qTEM) mode of the microstrip line into the



(a) (b)

Fig. 13. (a) Top view of the board for characterizing the power delivered to the antenna, comprising a microstrip-to-SIW-to-WR6.5 transition. (b) View of the transition and detail on the SIW-to-WR6.5 launcher.

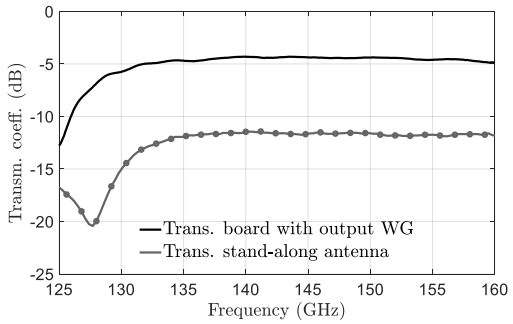


Fig. 14. Measured transmission coefficients of the transitions used in the board shown in Fig. 13 and for the stand-alone antenna characterization.

fundamental one of a SIW realized between m1 and m2. The second transition launches the field into the orthogonal rectangular waveguide. In particular, the SIW line is terminated on a via-fence cavity. An aperture of size equal to the waveguide section is realized in the cavity, on m1, beneath the WR6.5 flange. The field conversion and transmission coefficient are enhanced by a patch in the aperture and matching posts, as shown in Fig. 13b and originally proposed in [17]. The diameter and pitch of the vias in the SIW structures are 80 µm and 180 µm. Tolerances of ± 25 µm on the positions of the vias were observed. The length of the SIW line is 10 mm. A similar transition with a longer SIW line (27.3 mm) was fabricated for characterizing the stand-alone antenna prototype described in Section III-C. Both transitions were characterized using thru-reflect-line standards. The measured transmission coefficients are shown in Fig. 14. They are both flat in the -10-dB matching bandwidth, i.e. between 135 GHz and 160 GHz.

C. Antenna in package

The output microstrip line of the diplexer described in Section III-A excites the feed network of the antenna, on m1. The antenna structure and a picture of the radiating elements are shown in Fig. 15a. The array of four patches on m4 is square and the period along both axes is 1.25 mm, i.e. 0.67 λ_h, where λ_h is the free-space wavelength at 160 GHz. A small array was selected to obtain a relatively broad main beam. In this way, the TX module can be used as a feed for high-gain lens antennas, ensuring an effective illumination even at short focal distances [10], [18]. The patches are parallel-fed using a one-to-four microstrip power divider on m1 and four slots in the ground plane on m2. The slot width and length are 0.18 mm and 0.80 mm, respectively. The propagation of surface waves in the electrically thick dielectric slab between the ground on m2 and the patches limits the operating bandwidth. Via-fence cavities around each patch can effectively mitigate this issue. This solution has been demonstrated even for PCB antennas at D-band, but its realization was enabled by a high-resolution semi-additive processing (mSAP) [19]. Instead, the design rules of the low-cost PCB technology selected in this work, hindered the realization of four cavities. Thus, a single rectangular cavity surrounding the array was designed, using through-hole (via3), except in a small area around the input microstrip line. The lengths of the cavity edges are 3.3 mm and 2.9 mm along *x*- and *y*-axis, respectively. Full-wave simulations using a finite element solver were run to optimize the design. The simulated -10-dB matching bandwidth, considering the input line

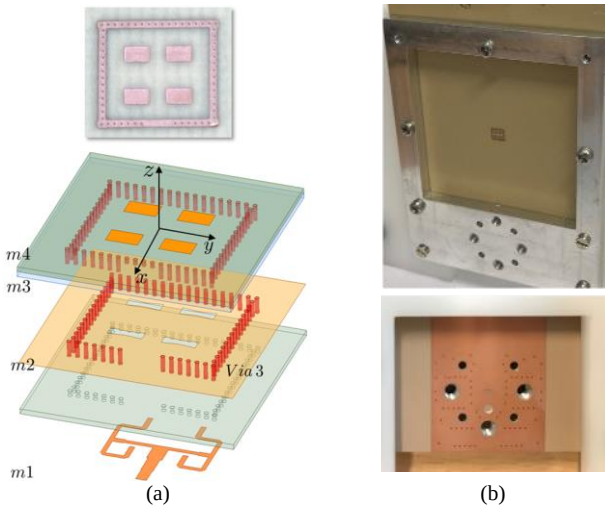


Fig. 15. (a) Exploded view of the aperture-fed patch array of the TX module and photograph of the patches on M4. (b) Picture of the stand-alone antenna prototype (top) and detail of the waveguide input transition on M1 (bottom).

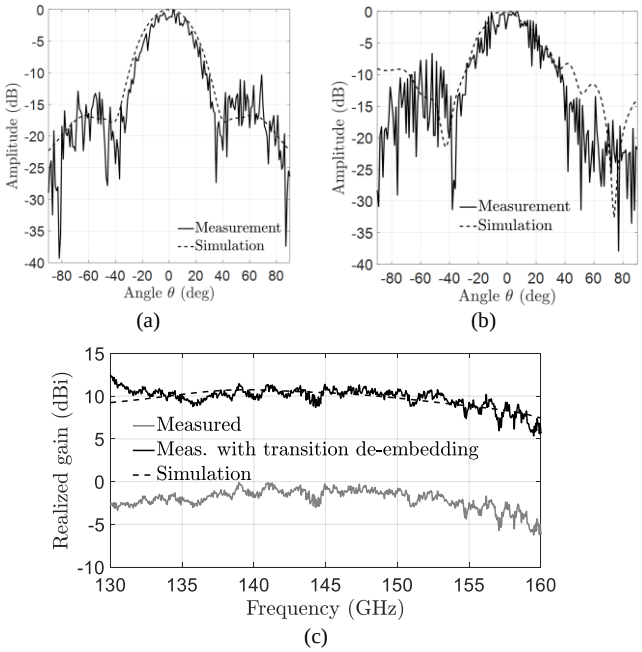


Figure 16. Measured and simulated radiation patterns at 154 GHz of the waveguide-fed patch array: (a) *yz*-plane and (b) *xz*-plane cut. (c) Measured and simulated broadside realized gain against frequency.

impedance as reference impedance, spans from 130 to 160 GHz. The passive prototype shown in Fig. 15b was fabricated and tested to characterize the stand-alone antenna performance. The sizes of the board and of the ground plane are the same of those in the TX module. The array feed network is excited using the transition presented in Section III-B. A detail of the input transition (m1 layer), with the holes for fixing the WR6.5 flange, is shown in Fig. 15b. The input waveguide is assembled to the board using screws and a mechanical frame on the opposite board side. The radiation pattern was characterized using a far-field free-space range setup in an anechoic chamber, with a 3-m distance between the reference transmitter and the antenna under test (AUT). In general, a good agreement between experimental and numerical results was observed. As an example, measured and simulated normalized patterns at 154

GHz are compared in Fig. 16a (H-plane cut) and Fig. 16b (E-plane cut). The asymmetry of the E-plane pattern is due to the feed and to residual surface-wave propagation. The large ripples observed at low amplitude levels are partially due to reduced dynamic range and to the interaction of the AUT with the measurement setup. The H-plane half-power beamwidth decreases from 42° to 34° between 130 GHz and 160 GHz. The measured realized gain of the AUT in the broadside direction is shown in grey in Fig. 16c. The realized gain of the patch antenna array used in the TX module is estimated by de-embedding the insertion loss of the input transition (see Fig. 14) in the stand-alone AUT. It tightly matches the results of full–wave simulations (see solid and dashed black lines in Fig. 16c) and varies less than 2 dB in the 130-156 GHz band. The peak gain is 10.7 dBi. The bandwidth and gain performance are comparable to those achieved by similar D-band antennas-in-package that leverage on more costly processes and substrates ensuring smaller design features (50 µm), such as high-density interconnect PCB technology [18], semi-additive processing [19] and liquid-crystal polymer (LCP) solutions [20].

IV. Characterization of the TX Module

Figure 17 shows the setup used to characterize the overall TX module. The multi-channel input signal is generated using an Arbitrary Waveform Generator (AWG) and an I/Q mixer up-converter. The TX output signal is measured over the air using a 20 dBi horn antenna and a commercial D-band down-converter, whose output signal is either connected to a spectrum analyzer or to a sampling scope for signal acquisition. For continuous wave measurements, the input IF signal is provided by a single-tone mmW generator.

A. LO signal generation

The LO signals performance is indirectly characterized at the D-band output. To this end, a single tone of 61.56 GHz and -15 dBm is injected at the IF input of the module. For this input signal, the TX emits a single tone at the centre frequencies of the LB and the UB. The input signal is generated using a high-performance lab-top mmW generator, so that its phase noise does not affect the measurement. Thus, the phase noise characteristics of the two signals radiated by the TX module are determined by the internal LO generators of each TC lane. Figure 18 shows the phase noise and spectrum of the two LO signals. The spectra are key to validate the rejection of the adjacent LO terms at N-1 and N+1 integer multiples of the desired frequency. Such undesired terms are rejected by more than 30 dB. A phase noise of -100 dBc/Hz @1MHz offset is measured for both LO generators on the received signal. Such a low phase noise is required for transmitting 64-QAM symbols with acceptable error vector magnitude (EVM) values.

B. TX module continuous wave characterization

Single-carrier TX module measurements are shown in Fig. 19. The gain of the overall TX module is calculated by dividing the equivalent isotropic radiated power (EIRP) by the IF input power for each frequency. The EIRP was obtained by measuring the received signal at 12 cm. The propagation path losses were calculated and added to the received signal power to evaluate the EIRP. Similar results were obtained for other distances ranging from 5 to 15 cm. The gain of the TX module,

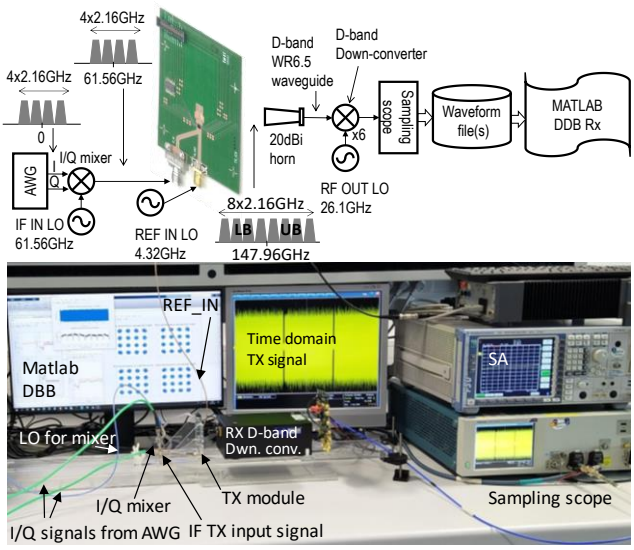


Fig. 17. TX module characterization setup.

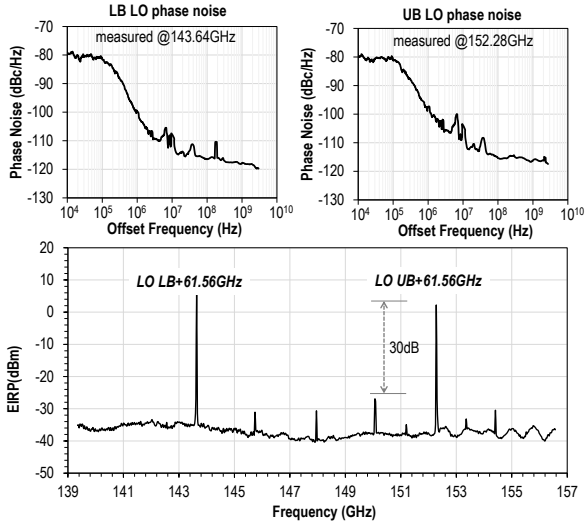


Fig. 18. On-chip LO generation performances.

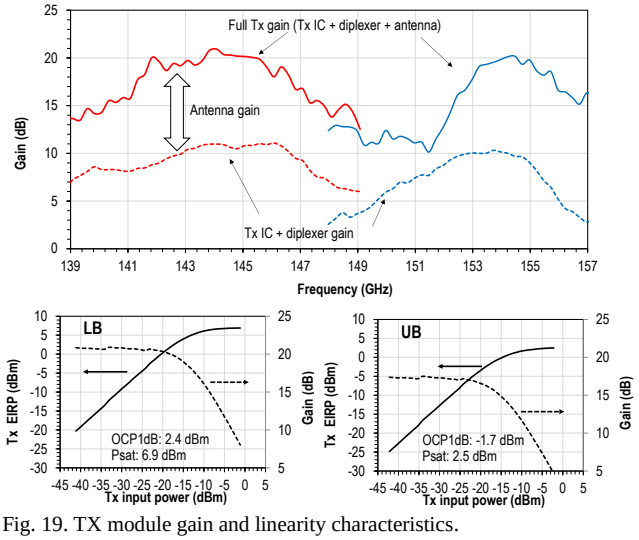


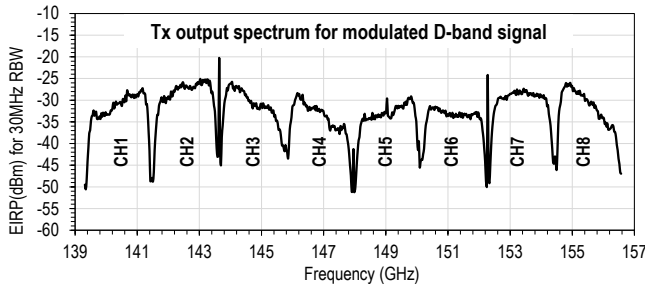
Fig. 19. TX module gain and linearity characteristics.

measured over the air, is shown in solid lines in the upper plot of Fig. 19 and is compared to that measured on the modified TX board with WR6.5 output presented in Fig. 13a. The output

power of this second board is measured directly at its WR6.5 output. After de-embedding the transition losses, the difference between the gain curves measured on the two boards is about 10 dBi. It corresponds to the antenna gain. A dip in the antenna gain retrieved from these over-the-air measurements is observed around 150 GHz. This dip was not observed in the gain of the stand-alone antenna (see Fig. 16c). It is attributed to the impact of fabrication tolerances and on the diplexer-to-antenna interconnect. Figure 19 shows also the over-the-air measured output 1 dB compression point (OCP1 dB). It is 2.4 dBm for the LB and -1.7 dBm for the UB, which results in a total EIRP for the TX module at the 1dB compression point of 3.8 dBm. The combined EIRP at P_{sat} in then 8.3 dBm.

C. *Modulated signal test*

Next, multi-channel BB modulated signals are applied at the TX IF input and the transmitted constellations and spectrum are measured at the receiver (RX) using a 20-dBi horn antenna. Some channels of the IF multi-band signal are boosted to partially compensate the variation of the TX gain across its full-band as well as the AWG data converter frequency response. The RX is placed at a distance of 7 cm for 16-QAM modulation and 5 cm for 64-QAM modulation in order to have constant and proper SNR ratio for EVM measurement. The TX IF input power is adjusted in both cases with 10 dB of back-off below the worst case TX input compression point (-15 dBm). Figure 20 shows the TX spectrum, where the signal level corresponds to the EIRP measured with a 30 MHz resolution filter. The multi-channel baseband signal generated by the AWG contains preamble and scattered pilots. They are used to estimate the propagation channel and other signal characteristics. The samples received by the scope are sent to a multi-channel digital baseband (DBB) receiver software implemented in Matlab. The latter includes separate channel equalization, carrier frequency offset and I/Q mismatching compensation, and eventually demodulates the received symbols. A data rate of 84.48 Gb/s is achieved for multi-channel 64-QAM. The EVM is below 10 % for all the channels for a TX to RX distance of 5 cm. Similar



CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8
140.40GHz	142.56GHz	144.72GHz	146.88GHz	149.04GHz	151.20GHz	153.36GHz	155.52GHz
1.76Gbauds	1.76Gbauds	1.76Gbauds	1.76Gbauds	1.76Gbauds	1.76Gbauds	1.76Gbauds	1.76Gbauds
EVM=9.7%	EVM=10.3dB	EVM=11.2%	EVM=10.7%	EVM=9.0%	EVM=10.1%	EVM=9.8%	EVM=9.5%
7.04Gb/s	7.04Gb/s	7.04Gb/s	7.04Gb/s	7.04Gb/s	7.04Gb/s	7.04Gb/s	7.04Gb/s
EVM=9.1%	EVM=9.4%	EVM=9.6%	EVM=9.0%	EVM=9.3%	EVM=9.8%	EVM=9.0%	EVM=8.6%
10.5Gb/s	10.5Gb/s	10.5Gb/s	10.5Gb/s	10.5Gb/s	10.5Gb/s	10.5Gb/s	10.5Gb/s

Fig. 20. Measured TX spectrum, constellations, and main performance.

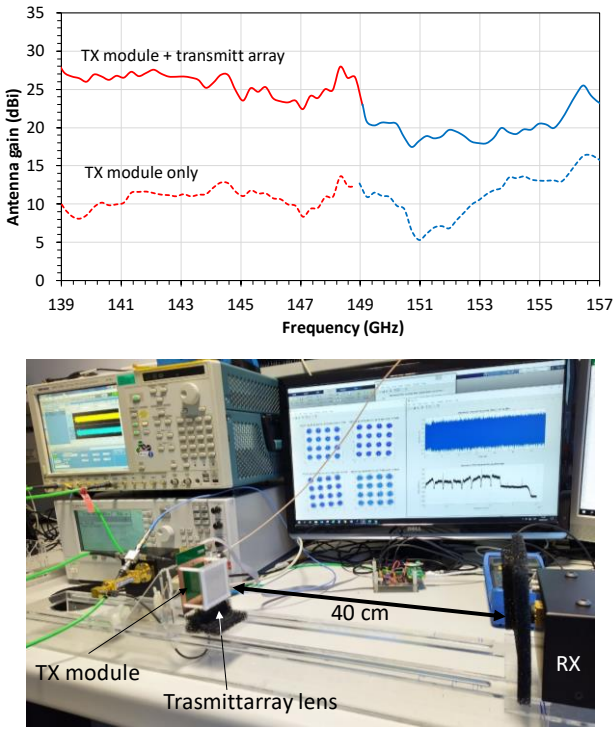


Fig. 21. Link range extension using a flat lens antenna. Antenna gain retrieved from continuous-wave measurements (top), measurement setup and measured 16-QAM constellation in the LB (bottom).

EVM performance is obtained using a multi-channel 16-QAM signal at a longer distance of 7 cm.

D. *Range extension with transmit array*

The TX module can serve as focal source for a flat lens antenna, also known as transmitarray (TA), to extend the range of the link. In the experiment shown in Fig. 21, an existing TA previoulsy demonstrated in [11] and fabricated using the same low-cost PCB process than the module is added at a distance of 3 cm from the module. The overall antenna gain is obtained as in Section IV-C. The output power measured over the air is divided by the output power measured on the waveguide terminated TX module of Fig. 13a. The gain values shown in Fig. 22 are obtained after deembedding both the path loss and the WG transition insertion loss. The TA boosts the EIRP by 16 dB at the LB. Please, note that the TA was not specifically optimized for this module. It optimally works at lower frequencies and its gain drops beyond 149 GHz. Nevertheless, it increases the TX antenna gain in the LB, which enables a sixfold extension of the link distance (40 cm) preserving similar signal peformance for 16-QAM modulation (see Fig. 21).

E. *Summary of results*

Table I compares this work with high-data rate D-band TXs. The proposed TX achieves a 84.48 Gb/s data-rate, consuming 600 mW from a 1V supply. Compared to similar CMOS-based TXs, the proposed low-cost system-in-package is the first with on-chip mmW multi LO generation and demonstrates 64-QAM transmission over the air at D-band. Moreover, it radiates one of the highest output power reported in the literature for pure CMOS TX ICs. The power consumption of the LO generation, IF to D-band front-end, biasing and digital circuitry are 130

Table 1. Performance comparison of high data-rate transmitters (*P_{out} corresponds to P_{sat} in this case, **EIRP radiated by the on-board antenna at P_{sat}).

Ref.	Freq. [GHz]	Data-rate (Modulation)	EVM (rms)	Symb. rate [GBaud]	P_{out} [dBm]	Technology	P_{DC} & Energy/bit	#Ch.×Ch. Bandwidth [GHz]	On-chip mmW LO/ in-package antenna & ant. gain
[1]	140-144	5.3Gb/s (64-QAM)	-	0.88	-2.3	InP	- -	1×4	No/No
[2]	130-142	12Gb/s (QPSK)	24.5%	6	-	45nm SOI	1255 mW 105 pJ/b	1×12	No/ Yes: Quartz 1.85 dBi
[4]	250-280	80Gb/s (16-QAM)	12.0%	20	-1.6	40nm CMOS	1790 mW 22.37 pJ/b	1×25.92	No/No
[5]	284-291	24Gb/s (16-QAM)	14.0%	6	9.5*	65nm CMOS	270 mW 11.25 pJ/b	1×7.36	No/No
[6]	220-255	95Gb/s (16-QAM)	17.0%	23.75	1.5	130nm BiCMOS	550 mW 5.78 pJ/b	1×28	No/Yes: on-chip ring & Si Lens 27 dBi
[3],[7]	131-140	-	-	-	14.3*	22nm FDSOI+PCB	196 mW -	1×8	No/Yes: 8×1 patch array 13.6 dBi
[8]	137-137	30Gb/s (64-QAM)	8.5%	5.0	27.5**	22nm FDSOI+InP HBT+LTCC	760 mW 25.3 pJ/b	1×**6**	No/Yes: 8×1 patch array 13.6 dBi
This Work	**139-157**	**54.32Gb/s (16-QAM)**	**11.2%**	**8×1.76**	**8.3****	**45nm SOI+PCB**	**600 mW 11.04 pJ/b**	**8×2.16**	**Yes/ Yes: 2×2 patch array 10 dBi**
		84.48Gb/s (64-QAM)	**9.8%**	**8×1.76**			**600 mW 7.10 pJ/b**	**8×2.16**	

mW, 450 mW, and 20 mW, respectively, resulting in 7.10 pJ/b energy consumption. The module radiates 8.3 dBm of EIRP at P_{sat} using a 10 dBi gain antenna in-package. The module including the IC, the diplexer and the antenna fits in a 12×6 mm^2 area. Better than 10% EVM has been demonstrated across the full TX band at 5 cm for 64-QAM modulation and at 7 cm for 16-QAM modulation. Furthermore, the addition of a flat lens antenna, yet not specifically optimized, allows increasing the link distance from 7 to 40 cm for the LB, offering an effective solution for meter-range wideband point-to-point D-band links based on compact and low-cost packaging.

V. Conclusions

An 84.48 Gb/s 64-QAM multi-channel TX module with antenna-in-package has been presented. Such a high-data rate wireless transmission has been achieved over a broad spectrum (17.3 GHz centred at 148 GHz) while maintaining a reasonably low input base-band bandwidth, thanks to an innovative channel bonding architecture. On-chip mmW multi-LO generation has been demonstrated for the first time by using high integer-N frequency multiplication. The two-channel D-band transmitter IC is fabricated in 45-nm CMOS PDSOI technology and flip-chipped on a PCB. The low-cost PCB process used to realize the packaged module represents a viable solution for short-range links beyond 100 GHz. The board comprises an SIW diplexer combining the two D-band channels and a 10-dBi-gain patch array. The 12×6 mm^2 TX provides an EIRP of 8.3 dBm with low DC energy consumption (7.1 pJ/bit) and high spectral efficiency (6 bits/Hz).

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