Serial connected active voltage clamping

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Abstract

The new post project for uranium enrichment SILVA needs specific power converters. The LETC laboratory of the C.E.A. in Pierrelatte has been studying these since 5 years. The aim of this laboratory consists in developing high voltage solid-state converters using a large number of small standard solid-state components (MOSFETs, IGBTs, thyristors and diodes) connected in series. In these associations, voltage balancement system are not used, but the voltage is limited on each stage in its safety area by clamping protection. This paper describes different voltage clamping systems, active clamping technique and their association in series.

Keywords
Device characterization, emerging topologies, modeling, MOS device, Power semiconductor device, reliability, simulation, system integration, test bench.

Introduction

The new post project for uranium enrichment SILVA (joint program CEA-COGEMA) needs specific power converters [1]. These have been studied since 5 years by the *Laboratoire Electrotechnique et Technologie des lasers à vapeur de Cuivre (LETC)* of the C.E.A. in Pierrelatte [2] [3].

The aim of this laboratory consists in developing high voltage solid-state converters. Several small standard solid-state devices (MOSFETs, IGBTs, thyristors and diodes) are connected in series on printed circuit boards [4] in order to replace gas-tubes (thyratrons, ignitrons and tetrodes). In these associations, voltage balancement system are not used, but the voltage range is limited on each stage in its safety area by clamping protection. This paper describes different voltage clamping systems, active clamping technique and their association is series.

These studies are conducted with the EEPS department of ESIM (*Ecole Supérieure des Ingénieurs de Marseille*) [5] and CENTRALP Enertronic which commercializes the industrial products.

Single protected component

Testing facility

The main part of these experimental studies has been made in our laboratory with a homemade component-evaluation facility called Avalanche Machine [6].

This tool applies voltage and current square signals to a component under test. The range and time of theses signals can be adjusted and are available on an oscilloscope. The next figure presents the synopsis of this equipment.

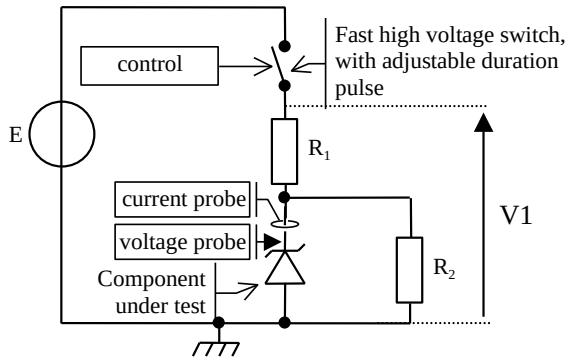

Figure 1 : Avalanche Machine synopsis

Voltage clamping techniques

The main different clamping techniques are intrinsic clamping, passive clamping and active clamping [7] [8] [9].

In intrinsic clamping, the component is self-protected by its own ability to limit its voltage. Not every solid-state device can run in such conditions.

In passive clamping, the protected component is clamped by an external device (transil, diode or varistor) plugged in parallel between the power terminals.

In active clamping, the component is auto-protected by a feedback system. Typically, a transil can be used to switch on MOSFET by charging its gate when the clamping voltage has been reached between the drain and the source of the MOS.

Figure 2 illustrates the typical basic structure of these three kinds of overvoltage protections on a MOSFET. The gray parts show the ways of clamping current :

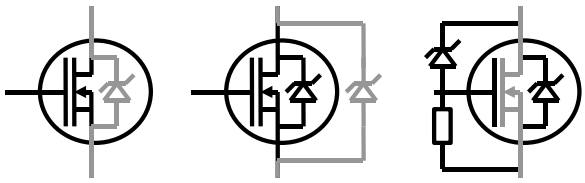

Figure 2 : typical kinds of voltage protection, intrinsic, passive and active clamping

In **intrinsic clamping mode**, the protected component has to support the avalanche mode. Not every solid-state device can run in such conditions. Only some diodes and recent solid-states devices are able to run in intrinsic voltage clamping mode. The main limit concerns the maximum reachable clamping energy for the chip.

In **passive clamping mode**, the protection component is directly connected in parallel on the power device. It's a classic protection mode, in which the main problem comes from the high dynamic resistance (R_{dyn}). When the current increases, the voltage level fixed by the protection component can reach the breakdown voltage of the solid-state device (V^M_{BV}) and destroy it (cf. Figure 3).

However, we can avoid such a problem by using a lower rating transil or by connecting several transils in parallel to reduce the global dynamic resistance. But in both cases, we are penalized by this protection mode either in terms of lower voltage level capability or in terms of the quantity of necessary protection components.

In **active clamping mode**, the voltage control is due to a reverse feedback on the control electrode of the protected component. The power dissipation ability is determined by the main switch component.

In contrast to the passive clamping mode, the high transconductance of the transistor implies a very low dynamic resistance. Thus, the active clamping mode allows a stable voltage level without breakdown risk, as shown on the Figure 3.

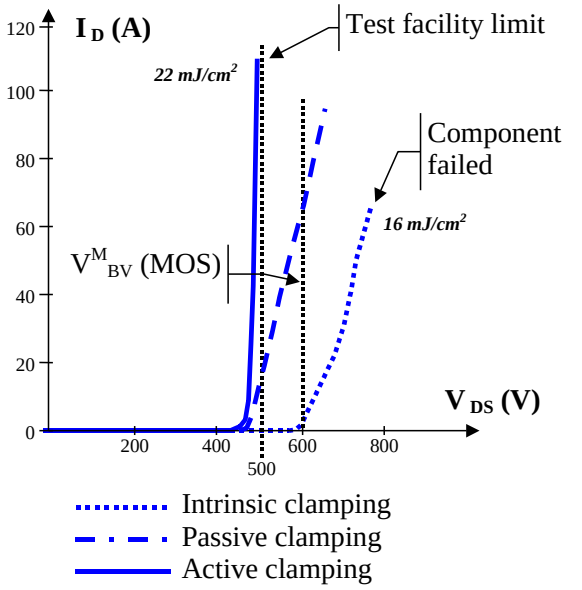

Figure 3 : three voltage clamping modes and the associated characteristics

The experimentation shows that in **high current clamping mode**, the active protection has a constant voltage level and a high energy absorption capability (Figure 3). Figure 4 presents a MOSFET (500 V, 0.85 Ω) protected by a transil (440 V) connected between gate and drain. The waveforms come from the *Avalanche Machine*.

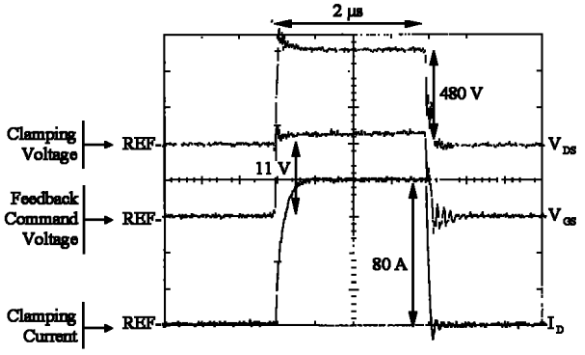

Figure 4 : typical high current clamping mode waveforms

Application of active clamping in serial association

This paragraph has two parts. The first deals with the perfecting by simulation of the active clamping structure on a single component. The second part present a product made in our laboratory using active voltage clamping system in series, and the ways to optimize it.

Perfecting by simulation

Simulation limit

In such a case of simulation (unlike qualitative simulation which can use perfect components) the access of all real phenomena forces us to be careful to the two following points : including parasitic elements (wiring inductors and parasitic capacitances) and using the more real models as possible in each application range.

The first point is generally well known and easy to adjust. However, using valid component models stays a fussy exercise [10]. For example, all power MOSFETs PSPICE models are treated like lateral MOS. As a result, every parasitic capacitance variation laws that are used are false for this type of transistor. As a conclusion, turn on delay time does not reflect the reality.

As far as we are concerned, the studies have been made with 500 V, 0.85 Ω MOSFETs IRF 840. We use a manufacturer model (coming from its web site) as a base of model, with our own modifications. The final MOS model has been validated by experiment for our study field.

Instability mode due to active clamping principle

The studied system is composed of a 500 V, 0.85 Ω MOS, actively clamped by a 440 V transil. It is studied by simulation as an automation system.

The **connection between the drain and the gate of the MOS represents the control loop** of the voltage regulation on the component. The **clamping voltage value of the transil is the voltage reference** value and **the drain-source voltage is the output value**. An external current is imposed to the clamping structure, as shown on the Figure 5.

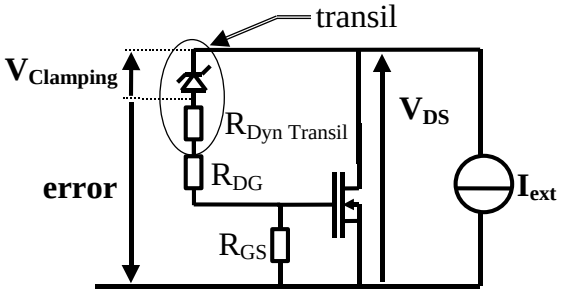

Figure 5 : Active voltage clamping structure studied by simulation as an automation system

We study the frequency response of the output voltage (V_{DS}) to little variations imposed on the voltage reference ($V_{Clamping}$). PSPICE traces the phase and the gain diagrams in order to localize the instability area.

Let remind us that a control loop is considered as unstable regarding the phase between output value and reference value. When it reaches ± 180 deg, the gain of this reverse feedback must not exceed 15 dB.

Figure 6 presents the parametric study of the regulation loop. The parameter is the external current which goes from 0.5 A to 10 A.

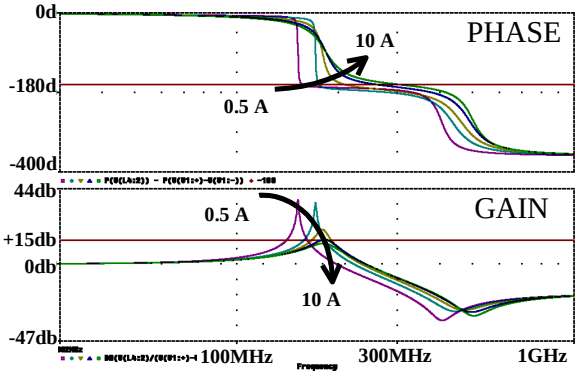

Figure 6 : parametric study on external current, phase and gain diagram

Figure 6 shows instability modes in the domain of low clamping current. For example, for an 1 A external current, the gain reaches 23.7 dB when the phase is –180 deg. This instability mode causes oscillations at about 175 MHz.

Experimentally, while clamping low current we observe these voltage oscillations on the feedback signal. Such oscillations can destroy the component because of gate oxide breakdown. The Figure 7 shows the corresponding waveforms.

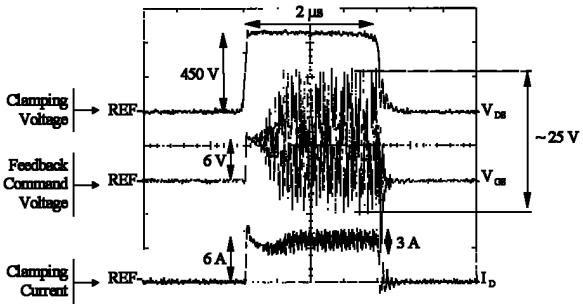

Figure 7 : command oscillations in case of low current clamping with a too high feedback gain

Such a typical problem of feedback system is that a too high gain can imply regulation instability. A solution we propose is to add a small resistor (several ohms) in series with the transil (R_{DG} on Figure 5). Such diminution of the gain stabilizes the feedback. The value of this resistance has been determined by a bi-parametric analysis of the system. The parameters are the R_{DG} value and the clamping current (I_{ext}).

Thanks to several bi-parametric studies (using I_{ext} as one of them), each resistor value has been optimized in order to avoid instability loop conditions. The next 3D curve shows an example of this type of bi-parametric study. It presents the gain loop when the phase is –180° depending of D_{DG} and I_{ext} values.

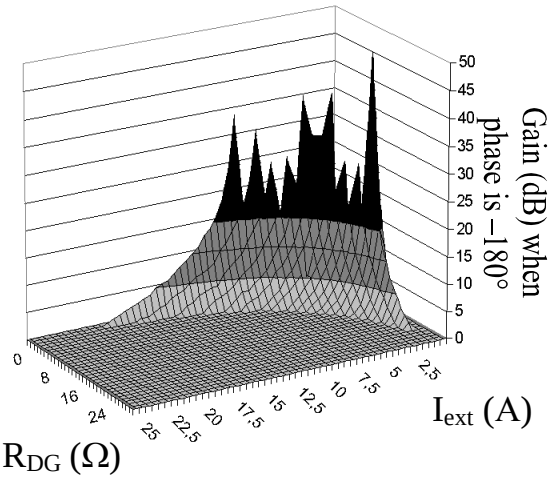

Figure 8 : bi-parametric study on I_{ext} and resistance in series with the transil

Such a diagram shows the instability area in current, depending of the resistance R_{DG} value. Instability area is localized in the low clamping current domain and can be reduce by adding a resistor in the regulation loop.

The Figure 9 presents the same experimental waveforms as in Figure 7 by using adapted sizing to avoid instability and failure.

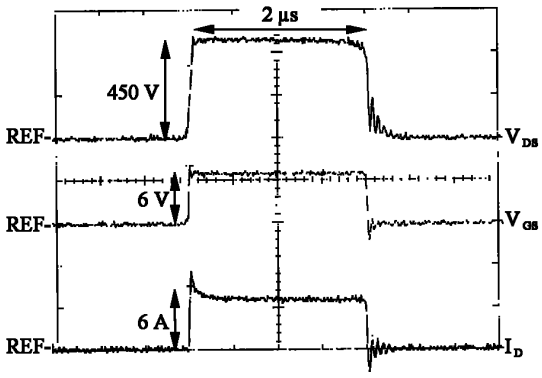

Figure 9 : command oscillations in low current clamping with an adjusted feedback gain

Construction

Existing product

The following photograph presents the prototype of a MOS matrix developed by our laboratory.

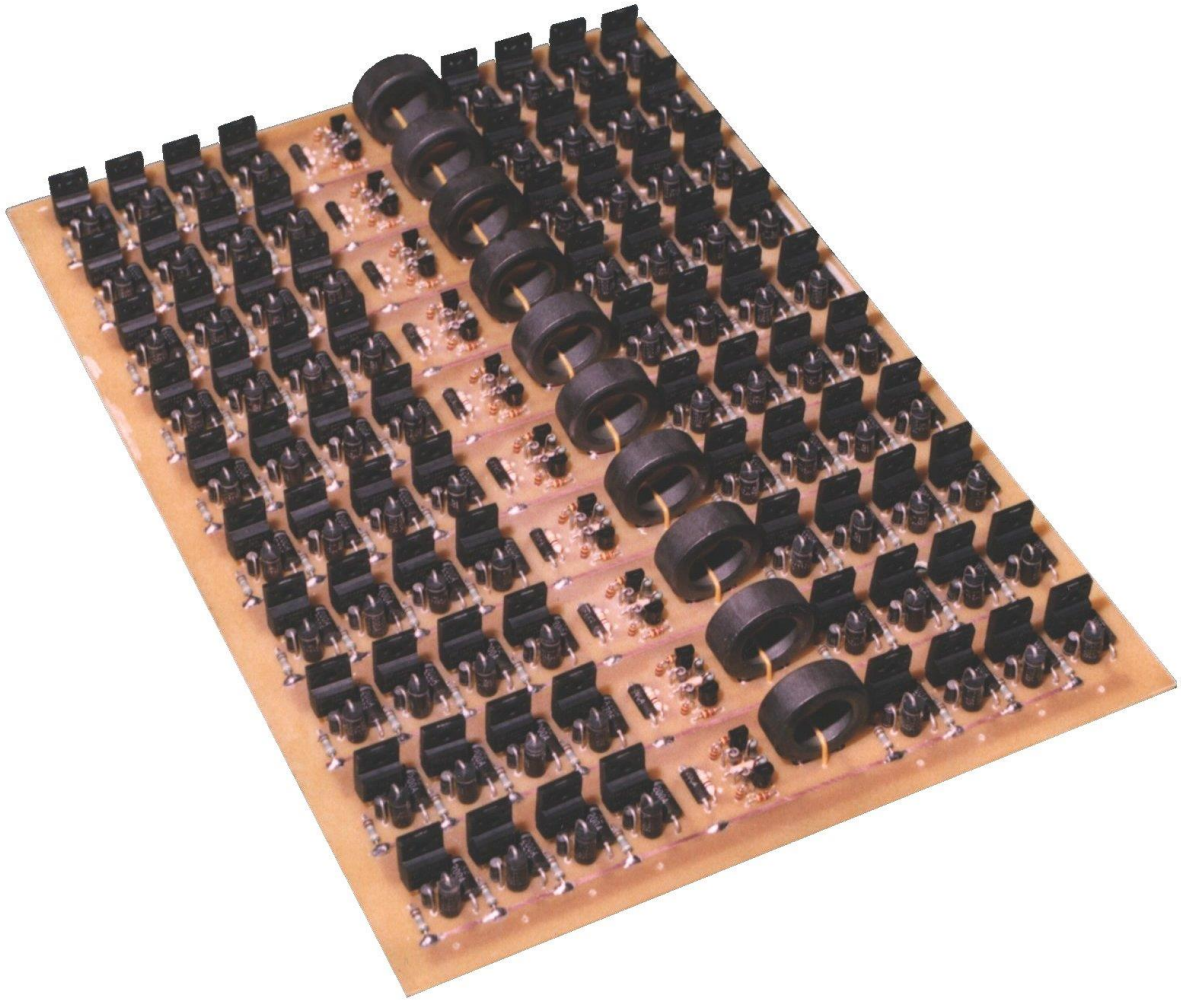

Figure 10 : MOS matrix using active voltage clamping on each stage

This high voltage switch (3 500 V) is designed to run on short-circuit and to open high current (240 A) on inductive charge. The overvoltage met in such a case requires reliable overvoltage protection. So, active voltage clamping has been used on each component of each stage. Moreover, in order to have an optimal overvoltage protection, passive clamping is used on each component too.

Perfecting and optimization

Nowadays, studies are made in collaboration with CENTRALP Enertronic to optimize this high voltage switch. The optimization points are following :

- Using one active clamping structure for several solid-state devices in parallel. Simulation and works are in progress to use a single regulation loop (with a single transil) for eight switching devices in parallel.

- Optimized use of solid-state device capabilities, such as the voltage rating. To have a higher voltage switch without over-costs, the clamping voltage reference of each stage (determined by the transil voltage rating, in the control loop) has to be closer to the power devices voltage rating. Of course, this optimization does

not have to be made to the detriment of reliability.

Thanks to the tools developed to study active voltage clamping system, we are working on a 5 000 V 1 000 A version able to run in short circuit mode : the higher the di/dt is, the more difficult it is to run in this mode. The optimized product has to support di/dt higher than 50 kA/µs.

Conclusion

Active voltage clamping seems to be the best overvoltage protection technique regarding an optimized use of power device voltage rating.

Thanks to the high clamping current and clamping energy that are reachable in the chip (without overvoltage and failure) this technique appears to be one of the most efficient.

The major subtleties of implementation occur while sizing the structure in order to avoid instabilities and voltage oscillations during a transient overvoltage. This is especially true in serial associations. These oscillations can destroy the system by gate oxide breakdown or drain-source destructive avalanche.

To perfect the active voltage clamping structure, several tools have been used :
- PSPICE for frequency studies
- 3D curves for instability areas representations
- Small scale experimental tests for simulation validation

Nowadays, theses tools are used for solid-state devices matrix perfecting.

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