Innovative Low-Power Self-Nanoconfined Phase-Change Memory

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Innovative Low Power Self-Nano-Confined Phase-Change Memory

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***Abstract*— In this paper, we demonstrate at array level and in industrial like devices, the extreme scaling down to nanometric dimensions of the Phase-Change Memory technology thanks to an innovative Self-Nano-Confined PCM device (SNC PCM). We show how such solution based on an optimized GeN/GeSbTe stack enables programming down to 50 µA and endurance up to more than 10^8 cycles in 4 kb arrays, with the huge advantage of having no dependency on the critical lithography dimension used. We further demonstrate that the high thermal confinement achieved in such extremely confined PCM makes the engineering of the SET pulse becoming fundamental in order to assure a reduced SET resistance drift. Moreover, thanks to physico-chemical analyses and 3D TCAD electro-thermal simulations we demonstrate the Self-Nano-Confined phenomenon, revealing an effective scaling of the PCM down to around 12 nm and how it improves the thermal efficiency of the device thanks to a reduced current density and thermal stress in the system.**

***Index Terms*— Low power Phase-Change Memory, Thermal confinement, Electro-thermal simulations.**

I. Introduction

PHASE-CHANGE MEMORY (PCM) is a major candidate among the resistive Non-Volatile Memory (NVM) technologies. Featuring properties of both DRAM and Flash, its advanced state in terms of development and industrialization in Storage Class Memory applications [1] and in embedded PCM-based microcontrollers for automotive applications [2] makes it an undeniable breakthrough in the present storage scenario. Even if phase-change mechanism with current in the microampere range has already been demonstrated for nanometric analytical devices [3], current reduction remains the main requirement for PCM products to address next generation of NVM low power applications. Several solutions have been proposed so far, such as: a) aggressive lithography and architecture solutions [4], b) more or less complex material engineering [5], c) interfaces and thermal efficiency improvement [6]. Despite the promising results, these solutions still raise doubts about the technology cost, its scalability in industrial devices, the material evolution control during Back-End-Of-Lines (BEOL) fabrication steps, and the material degradation along cycling especially in scaled PCM. PCM stacks based on oxide interfaces have been proposed in order to reduce the programming current [7], but without scaling capability demonstration and a possible detrimental oxygen impact on the integrity of the chalcogenide material [8] [9]. In this work, we propose a Self-Nano-Confined PCM (SNC PCM) solution based on an optimized oxide-free GeN/GeSbTe stack integrated in state of the art "Wall" PCM (Fig. 1). The device features high stability and integrity even during BEOL fabrication (one hour at 400 °C) and a reliable low voltage initialization step. We show RESET current (I_R) reduction down to 50 µA, without any dependence on the device size, suggesting the existence of a self-nano-confined (SNC) mechanism responsible for a higher thermal efficiency of the device. This result is very encouraging since previous work performed on PCM arrays presented a minimum RESET current of 100 µA achieved either with not scaled devices (critical dimension

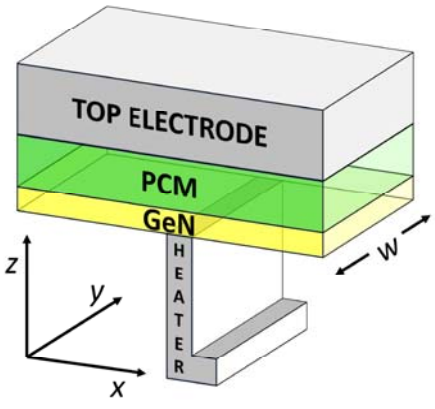

Fig. 1. Simplified schematic of the as fabricated SNC PCM "Wall" device based on a GeN/GeSbTe stack.

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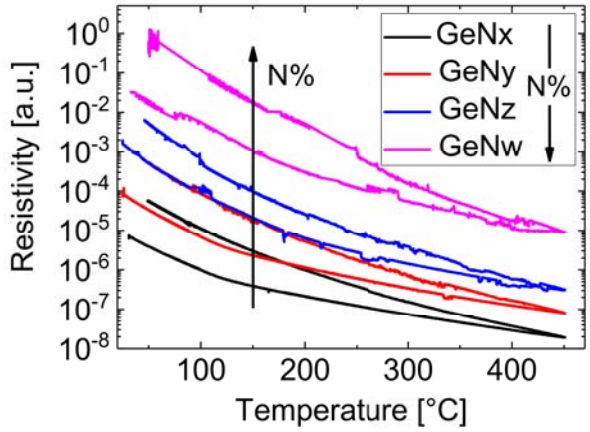

Fig. 2. N concentration tuning in GeN layer. The higher the N concentration from x to w, the higher the resistivity.

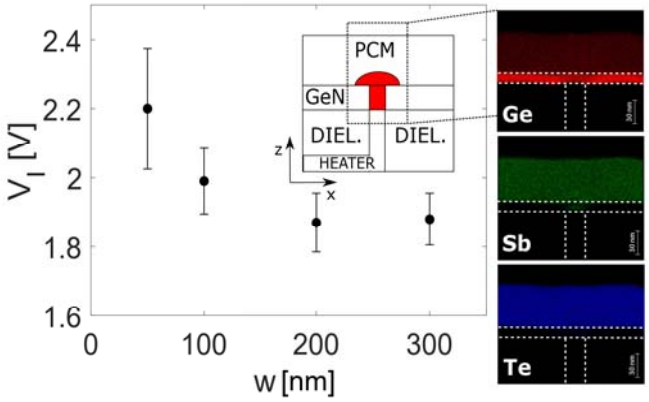

Fig. 3. Mean and $\pm 1\sigma$ values for the initialization voltage (V_I) measured in arrays as a function of w (left). TEM/EDX (xz plane) analysis of a device initialized at 1.2 mA, showing the SNC phenomenon and the absence of elemental segregation (right). The inset schematizes the shape of the active volume of the SNC PCM.

CD equal to 200 nm) [10] or extremely scaled (CD equal to 20 nm) [11] but expensive because of complex fabrication. The results presented in this work are supported by detailed Transmission Electron Microscopy (TEM) images supported by Energy-dispersive X-ray spectroscopy (EDX) analyses and 3D TCAD electro-thermal simulations, revealing an effective scaling of our PCM down to about 12 nm. The reduced current density and thermal stress in SNC PCM enable an endurance up to more than 10^8 cycles. Finally, we demonstrate the need for an optimized SET operation in extremely confined PCM device featuring high thermal confinement.

II. Device Fabrication and Electrical Characterization

A. GeN layer analysis and device integration

The SNC PCM functionality is based on the soft breakdown of the GeN layer performed as a first step (i.e. initialization) on as fabricated devices. The reliability of such electrical initialization depends on the layer uniformity, its resistivity and the tuning of the electric field required. We engineered the GeN layer by exploiting different N contents and thicknesses in order to tune its resistivity, the electric field needed to initialize the layer, and its stability at high temperature targeting the BEOL compatibility and best device performances. The resistivity as a function of temperature measured by the four-point-probe method is reported in Fig. 2 and it shows the increase of the resistivity with N content. Intermediate N content introduced in GeN_y layer was finally chosen for integration in electrical devices, featuring the right compromise in terms of resistivity even after annealing at 450 °C.

The GeN/GeSbTe optimized stack was integrated by magnetron sputtering in 4 kb arrays of state of the art "Wall" based PCM devices fabricated in the BEOL of the fabrication of LETI Memory Advanced Demonstrator (MAD) based on 130 nm CMOS technology, for statistical electrical parameters evaluation. Fig. 1 reports a 3D simplified description of the as fabricated cell. The devices have a nominal width (w) ranging from 50 nm up to 300 nm.

B. Electrical characterization of 4 kb PCM arrays

Preliminary tests are performed on 4 kb arrays to confirm the GeN layer integrity and the device functionality. The initialization voltage (V_I), which is used to supply the bit-line of the arrays, shows a slight evolution and a low variability with respect to w (Fig. 3). The slight decrease of V_I observed increasing w is associated to the known phenomena of materials dielectric strength change with material shape and size [12]. The inset in Fig. 3 describes the initialization mechanism, showing in red the region involved in the programming of the cell after the initialization procedure (i.e. the active volume). The TEM/EDX analysis after initialization reported in the same figure confirms the diffusion of Ge, Sb and Te in the GeN constriction with the formation of a GeSbTe confined region without facing any material segregation. This

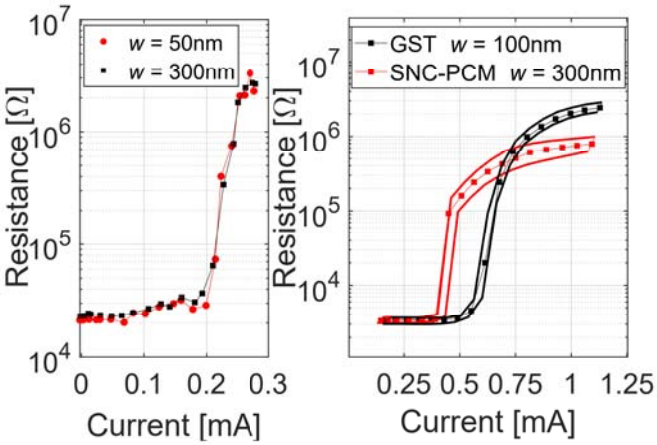

Fig. 4. (Left) 1T1R RI characteristics for 50 nm and 300 nm devices obtained with 10 ns/300 ns/10 ns staircase pulses. Size-independency of SNC mechanism is here verified with I_R of about 250 µA. (Right) Median and $\pm 1\sigma$ values for RI data comparing the behavior of a SNC PCM (with w equal to 300 nm) with respect to standard PCM (w equal to 100 nm) based on $Ge_2Sb_2Te_5$ (GST). The SNC PCM is 3x larger but it assures the same programming current of GST with a steeper transition.

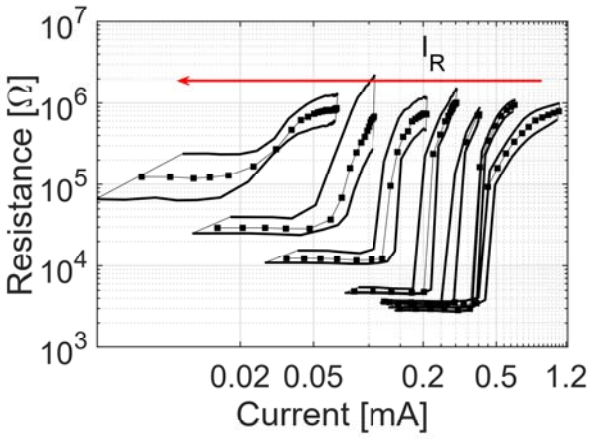

Fig. 5. Median and $\pm 1\sigma$ values for the RI characteristics in log-log scale obtained in 4 kb arrays at different I_Rs. SNC PCM devices demonstrate a programming current reduction down to 50 µA.

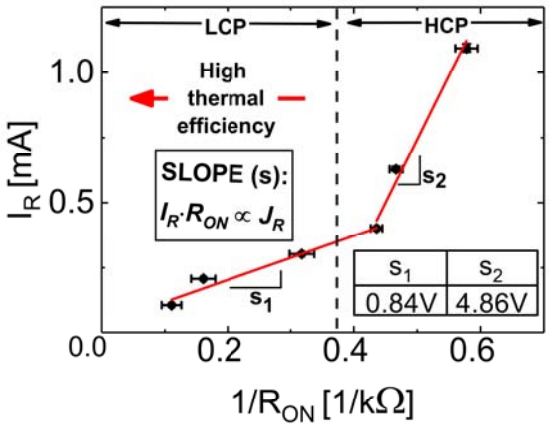

Fig. 6. Median and $\pm 1\sigma$ values for the RESET current (I_R) as a function of the inverse of the dynamic device resistance (R_{ON}) in 4 kb arrays. The different slopes evidence the lower current density (J_R) needed to program devices initialized with low I_R (LCP) with respect to the ones for which a high I_R is used (HCP). A lower slope in LCP population is highlighting a better thermal efficiency of the programming operation in such SNC PCM devices.

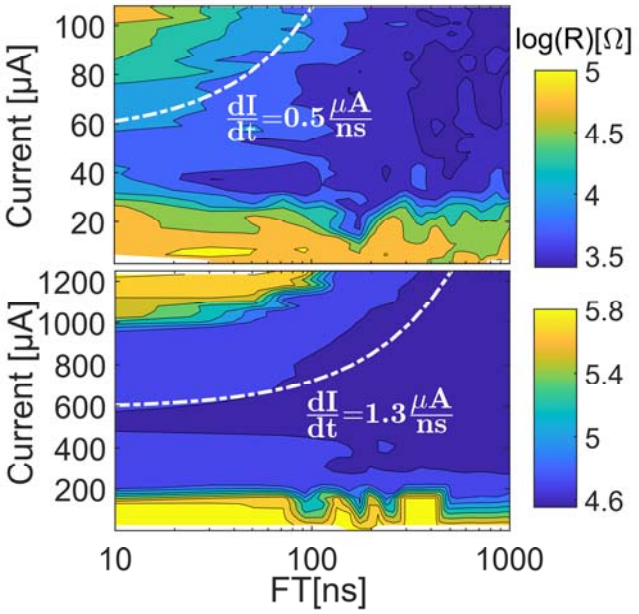

Fig. 7. SET cartographies showing the SET resistance evolution as a function of the pulse fall time (FT) (x-axis) and of the pulse current (y-axis). The results are reported for a 1T1R device initialized at 100 µA (top) and 1.2 mA (bottom). The slope dI/dt needed to reliably SET the cell (i.e. equal to dI/dt_{SET} used to achieve a 3x RESET resistance lowering) is more than two times lower in SNC PCM owning to LCP.

support the idea that the SNC mechanism is taking place in our devices. Resistance vs Current (RI) characteristics of 1T1R (i.e. 1 transistor/1 resistor) devices demonstrate that the SNC PCM mechanism is independent from the device size w (Fig. 4 (left)), showing identical RI for device widths of 50 nm and 300 nm when initialized with the same current. The main advantage is that the mechanism can be tuned by controlling the bit line current that flows in the device during the initialization step, therefore it has the role to define both the CD and the RESET current of the devices. The initialized devices are firstly programmed in the SET state with a squared pulse "SP" (i.e. rise/width/fall time equal to 10 ns/300 ns/10 ns). The gradual resistance increase towards the RESET state is obtained with a staircase up sequence of SPs of increasing amplitude (with steps of 0.1 V). Furthermore, in Fig. 4 (right) we compare the RI characteristics obtained in 4 kb arrays for SNC PCM with respect to the standard GST cell highlighting the same programming current in both the devices (1.2 mA) only if the w in a standard cell is reduced by a scale factor of three. The steeper SET-RESET transition in SNC PCM is a particular evidence of the confined structure achieved thanks to the initialization step. By tuning the current in the initialization, it was possible to obtain seven different RI characteristics (Fig. 5) and show that the SNC mechanism can take place down to RESET current of 50 µA. The SET resistance increase at low I_R is a clear evidence of the smaller diameter achieved during the initialization process.

By taking into account the inverse proportionality between the dynamic resistance of the devices (R_{ON}) and the area of the initialized confined region of the GeN layer, it is possible to consider:

$$I_R \cdot R_{ON} \propto J_R \tag{1}$$

where I_R is the RESET current and J_R is the associated current density. The I_R as a function of the inverse of R_{ON} is reported in Fig. 6 which is useful to follow the evolution of J_R in the different device populations. The data can be divided in two regions each one characterized by a different slope (s_1 and s_2). The lower value of s_1 is correlated to the J_R reduction in devices belonging to the Lower Currents Population (LCP) leading to a better thermal efficiency with respect to the devices in the High Currents Population (HCP).

The analysis on the SET programming speed is reported in the SET cartographies of Fig. 7 performed on 1T1R devices from LCP (I_R equal to 100 µA) and HCP (I_R equal to 1.2 mA). The test is done by acquiring the resistance achieved in the cell after the application of a RESET pulse followed by a SET pulse (with a fixed pulse width of 300 ns, and increasing

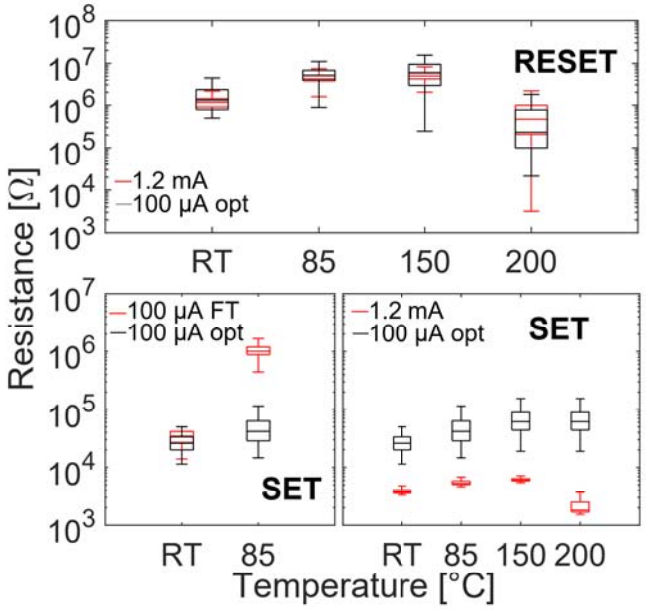

Fig. 8. RESET (top) and SET (bottom) data retention performed by isochronal annealing of one hour at increasing temperatures on 4 kb arrays with I_R of 1.2 mA and 100 µA. The RESET retention performances are comparable for the two SNC PCMs. SET stability is ensured by SET-opt protocol, since a standard FT strategy leads to a high resistance drift already at 85 °C.

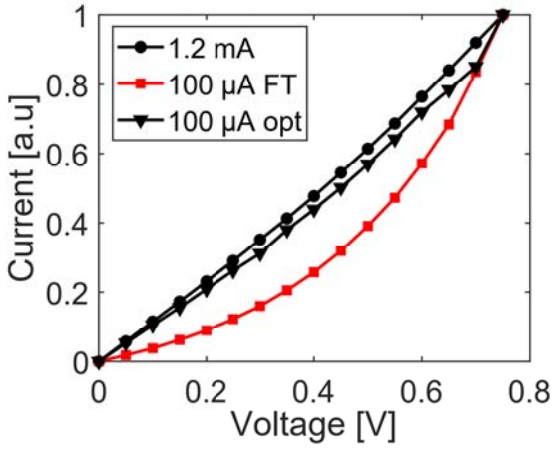

Fig. 9. Normalized subthreshold IV curves for 1T1R devices programmed at 1.2 mA (HCP) and 100 µA (LCP). The ohmic behavior observed in HCP devices is achieved in LCP ones only with optimized SET protocol.

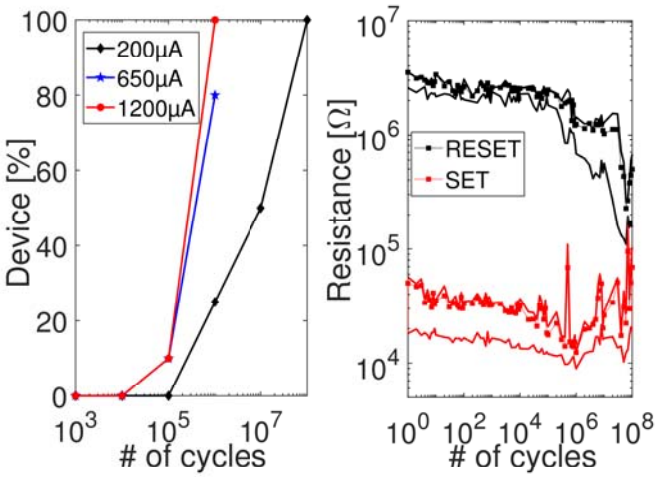

Fig. 10. Device endurance analysis showing the statistics for the starting of the resistance window degradation, detected as a 3x reduction of the starting RESET resistance, for three different values of initialization current I_R. Ten devices has been tested for 650 µA and 1200 µA population and four for the 200 µA due to their best endurance performance up to 10^8 cycles.

fall time and amplitude). The dashed lines in the figure represent a linear fit used to evaluate the current over time ratio (dI/dt) needed during the pulse fall time to reliably SET the cell (i.e. to decrease the resistance value threefold with respect to the RESET state). The optimal dI/dt (i.e. dI/dt_{SET}) ratio is more than two times lower in devices belonging from LCP, revealing the need of an optimized SET pulse to fulfill the specific requirement. Data retention tests on RESET and SET states were performed for the two populations LCP and HCP under investigation. Both the standard SET and the optimized SET were compared in terms of retention. The RESET state (Fig. 8) shows a comparable behavior for both the high and low initialization currents, with a resistance drift at 85 °C and a beginning of recrystallization at 200 °C, confirming the preservation of the material properties even in nm-scale SNC PCM. The comparison between the standard (SET-FT) and optimized SET (SET-opt) shows that the optimized SET protocol helps reducing the resistance drift faced as soon as the temperature is increased, certifying the higher crystalline homogeneity obtained in the confined region of the SNC PCM device with respect to the standard pulse. The result achieved with the optimized pulse is also evidenced in the subthreshold conduction analysis (Fig. 9). In particular, the LCP device programmed with a SET-opt procedure reveals a reliable ohmic behavior, comparable with the device initialized at higher current and programmed with a standard pulse. On the contrary, the 100 µA device programmed in SET state with a standard pulse shows an exponential conduction, that we can correlate with a non-uniform crystalline or partially amorphous structure having trap-dominated conduction [13].

The endurance is performed to study the material evolution along cycling for three populations ranging from LCP to HCP (i.e. initialized at 200 µA, 650 µA and 1200 µA). The comparison is made detecting when the resistance window starts to be reduced in particular because of the RESET resistance decreasing. The percentage of devices facing such starting of degradation is reported as a function of cycling in Fig. 10. It shows that the degradation starts at 10^6 cycles for devices with I_R equal to 650 µA and 1200 µA (HCP), while in SNC PCM featuring the lower I_R (LCP) the same order of degradation is observed only at 10^8 cycles. To be noted that in all the tests performed, all the devices kept at least a resistance window of one order of magnitude after 10^6 cycles. Furthermore, the measured degradation results to be accelerated by the use of the same pulses (RESET: 10 ns/300 ns/10 ns and SET: 10 ns/300 ns/10 µs) for the three populations at

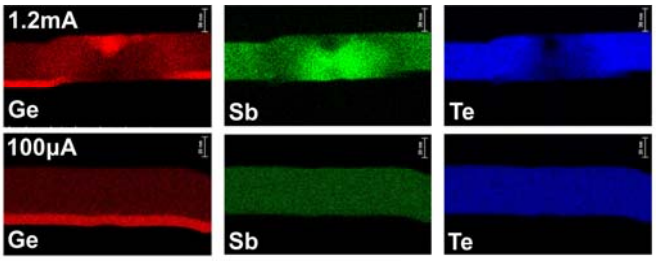

Fig. 11. TEM/EDX Ge, Sb and Te cartographies for SNC PCM cycled 10^6 times, respectively at 1.2 mA (top) and 100 µA (bottom). At 1.2 mA the GeN layer degrades along cycling with strong elemental segregation. On the contrary, 100 µA device does not show signs of degradation (programmed region not visible because of its nm-dimension).

the maximum I_R. Therefore, this result is even more representative of the high reliability of SNC PCM devices, that could feature higher endurance if benefiting of optimized or intelligent cycling algorithms [14]. The resistance evolution along cycling for a RESET current of 200 µA is reported in Fig. 10, where it is possible to evidence the type of RESET lowering we observed independently from the initialization current applied (i.e. the RESET lowering mechanism is the same but it happens at a different number of cycles). The device degradation under cycling is studied by the TEM/EDX cartographies (Fig. 11), performed on devices cycled up to 10^8 cycles for both I_R of 1.2 mA (top) and of 100 µA (bottom). The analysis confirms the higher level of segregation triggered after 10^6 cycles in HCP devices, while no sign of degradation appears in LCP where the GeN layer results to be still uniform after cycling. To be noted that the signal reduction due to the presence of the filament is quite small in the device programmed at 100 µA because of the signal integration along the width of the lamella used for the analysis. The SNC PCM stability was verified after a BEOL like thermal budget of one hour at 400 °C. By increasing the annealing time, the GeN layer faces a structural reorganization [15], which results in the V_I lowering (Fig. 12). Nevertheless, the TEM/EDX image (inset) and the SET/RESET distribution for 200 µA cells show that the GeN layer integrity is kept even after an annealing of one hour at 400 °C and the devices can be programmed with a similar resistance window.

III. Electro-thermal simulations

3D electro-thermal simulation were performed in COMSOL Multiphysics [16] and run on SNC PCM with different critical dimensions. Fig. 13 represents the temperature profile reached in the PCM at the same current density J for devices having a CD of 12.5 nm (representative of the LCP) and of 37.5 nm (representative of the HCP). It is possible to observe a higher maximum temperature in devices with the smaller CD, highlighting the higher thermal efficiency of SNC PCM featuring lower I_R. In Fig. 14 the results of the simulations for the current density at the melting of the PCM material, shows its increasing moving towards a higher CD, in accordance with experimental results previously reported in Fig. 6. Furthermore, it is shown that a higher J leads to

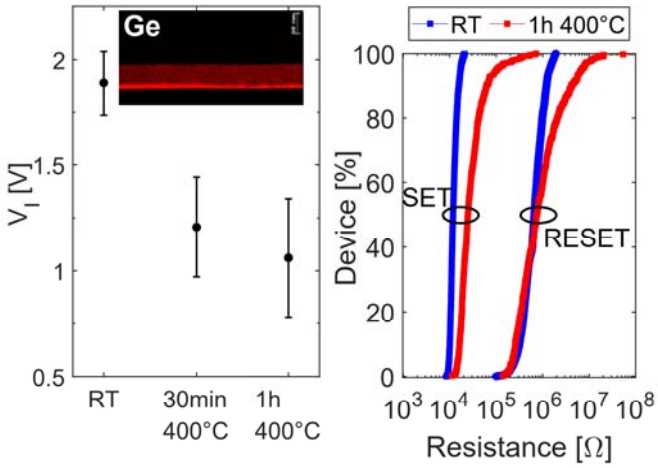

Fig. 12. Results of BEOL like thermal stress at 400 °C. GeN_y layer integrity is confirmed by TEM/EDX analysis (inset). V_I is lowered at around 1 V after annealing. SNC mechanism is preserved after BEOL, as demonstrated in SET/RESET distributions for I_R equal to 200 µA, compared before and after annealing.

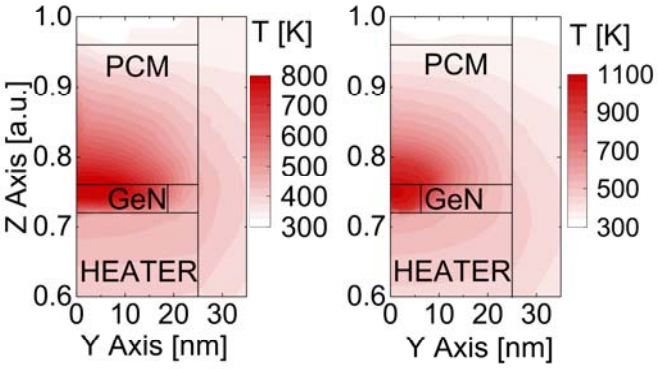

Fig. 13. Temperature profile simulated for SNC PCM with CD of 12.5 nm (right) and 37.5 nm (left) using the same current density J. Higher temperature is achieved in smaller SNC PCM thanks to its higher thermal efficiency.

a higher maximum temperature, which is likely responsible for a faster degradation of the material as observed in the endurance tests and TEM/EDX image (Fig. 10 and Fig. 11) in the devices initialized with high I_R. Moreover, the analysis performed on the temperature uniformity inside the constriction generated in the GeN layer, shows a lower temperature gradient dT/dz (i.e. higher uniformity) in devices with small CD (Fig. 15). In general,

$$\Delta T = R_{th} R_{ON} I^2 \tag{2}$$

where ΔT is the temperature increase in a device having a specific thermal resistance R_{th} at a given programming current I. Hence:

$$\frac{dT}{dt} \propto \frac{dI}{dt} \tag{3}$$

It means that during the SET operation, in order to reliably program the device, the current over time rate reduction during the fall time of the SET pulse (i.e. dI/dt_{SET} measured in Fig. 7) depends on the following relation:

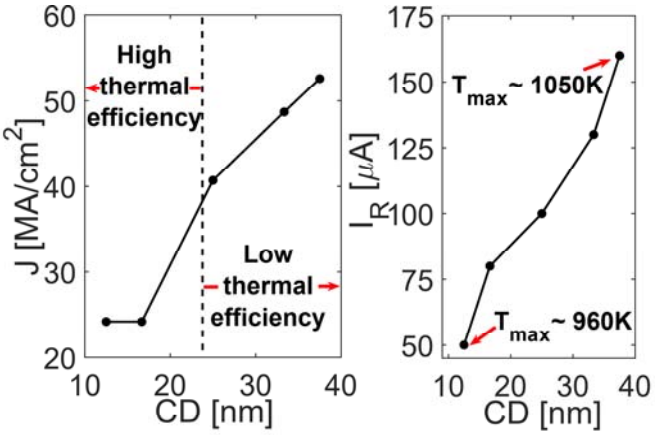

Fig. 14. Simulated J needed to achieve the melting of the material as a function of CD (left). J is lower in small CD (i.e. higher thermal efficiency) in accordance with Fig. 6. I_R extracted from simulations as a function of CD (right), shows that the maximum temperature (T_{max}) achieved during RESET operation is lower for smaller CD. The CD extracted at a I_R of 50 µA is of around 12 nm, that is the expected CD in the devices initialized at such low current in Fig. 5.

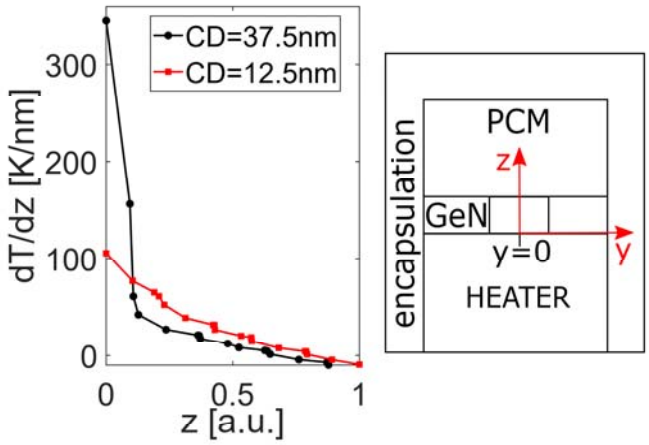

Fig. 15. Simulated temperature gradient along z-axis ($\boldsymbol{dT/dz}$) in the confined region of SNC PCM (at y = 0) for two devices featuring different CD size. A higher temperature homogeneity (i.e. lower $\boldsymbol{dT/dz}$) is achieved in highly scaled confined SNC PCM featuring small CD.

$$\frac{dI}{dt}_{SET} \propto v_g \frac{dT}{dz} \tag{4}$$

where v_g is the material crystalline growth speed. Therefore, the improved temperature uniformity in smaller CD observed in our simulations (Fig. 15) explains the lower dI/dt_{SET} measured in devices initialized at low current and featuring small CDs. This result supports the need for an optimized SET protocol in extremely confined devices, like in our SNC PCM.

IV. Conclusion

This work demonstrates for the first time at array level and in industrial like devices, the extreme scalability down to nm scale of PCM technology thanks to an innovative and lithography-free SNC PCM device. We show the possibility to customize the programming condition of our device independently from the size and down to a programming current of 50 µA. We demonstrated the need for a lower current density to program the cells initialized at currents lower than 400 µA. Thanks to 3D TCAD electrothermal simulations we highlighted that such lower current density is related to a better thermal confinement of the cell: the maximum temperature was shown to decrease with the device CD in III. Endurance up to more than 10^8 cycles is presented for nm scaled SNC PCM devices. This result is supported by TEM/EDX anlyses showing that 10^6 cycles do not impact the GeN interfacial layer for low CD devices. Furthermore, the SET programming cartographies show the need for a SET pulse protocol optimization for highly scaled SNC PCM, which assures a reduced SET resistance drift and a data retention comparable with the devices initialized at higher current. The SNC PCM solution presented shows also a perfect integrity after BEOL thermal budget, definitely combining BEOL process compatibility, performance reliability, low power programming and scalability demonstrated at array level.

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