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Impact of Bottom Electrode Integration on OxRAM Arrays Variability

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ABSTRACT

HfO_2-based OxRAMs with various metal stacks in the inferior VIA of bottom electrode were fabricated. We demonstrated for the first time that the metal stack of TiN PVD (physical vapour deposition), followed by an annealing step decreases the standard error of the forming voltage by 10% compared to the other variants. The related die-to-die and cell-to-cell variability is greatly reduced along the wafer diameter and the LRS shows better control of the tail bits at 3σ of the distribution. The number of failed operations over 1e4 cycles for 1k cells is reduced by a factor 3, reaching a BER of 8e-5. Finally, correlation of the cell reliability with the bottom via roughness is discussed.

INTRODUCTION

Resistive Random-Access Memories (RRAMs) are extensively studied as a competitive candidate for future nonvolatile memory application due to their simple structure, fast switching speed and compatibility with silicon Complementary Metal-Oxide-Semiconductor CMOS technology [1-2]. However, the key obstacle for the use of metal oxide RRAM (OxRAM) is the relatively poor uniformity of the switching voltages and resistance states. Some studies investigate RRAM variability on single cell structures for a large number of cycles [3], thus considering the cycling variability but not the device-to-device one. Others works in literature dealt with array structures, although lacking information on the fundamental variability limits [4-6]. Moreover no correlation with process parameters was addressed. In this work, we focus on the impact of various metal stacks as inferior VIA of the bottom electrode (BE). The process-induced variability is studied as well as impact of die location on cycling variability. The results allowed us to benchmark the various bottom electrode integration processes and to relate the process variations to the electrical performances.

OXRAM TECHNOLOGY AND STRUCTURE

OxRAM technology was integrated on 130 nm CMOS logic. On top of Cu Metal 4, a BE is defined by three various metal stacks (Tab. 1) as inferior VIA and completed with the deposition of a 150nm TiN layer, acting as the bottom electrode of the memory. The remainders of the fabrication steps are exactly the same for the three investigated BE integrations. They consist in BE CMP, deposition of the HfO_2 10nm/Ti 10nm/TiN memory stack and the completion of the back end of the device. A summary of the process steps, together with a cross section of a fully integrated 400nm device, are reported in Fig. 1.

The tests presented in this work have been performed on 4kb 1T-1R arrays developed within this platform. The word line (WL) is connected to the NMOS gate, setting the current compliance Icc. Forming and Set operations are performed by applying a positive voltage pulse on the bit line (BL) that is also the OxRAM top electrode, whereas Reset is performed by applying a voltage pulse on the source line (SL), contacted to the NMOS source.

FORMING VOLTAGE VARIABILITY

The first indicator used to evaluate the various BE integration processes is the forming voltage distribution. This parameter has the advantage of being (a) very sensitive to physical characteristics such as the electrode surface roughness, the insulator thickness and eventual oxide interface residues, and (b) one critical parameter for OxRAMs integrated in scaled technology nodes, as the maximum BL voltage is frequently limited by the gate oxide thickness.

The forming voltage has been measured with a 1µs pulse sequence of increasing BL voltages from 2V to 5V, with a step of 0.1V. The 4kb arrays (8 matrices) along the wafer diameter chosen for this measurement are presented in Fig. 2. The heat maps reported in Fig. 3 and the forming voltage distributions in Fig. 4 show the differences between BE integrations and between matrices along the wafer diameter for each variant. The W variant is the least uniform: it has a larger process induced drift (top wafer = lower voltage). For W, which has a higher mechanical strength than TiN, a higher RMS roughness of its post CMP surface (Fig. 7b) is observed in comparison with the TiN one (Fig. 5b). Consequently, it can induce oxide residues on the BE surface (Fig. 6), corresponding to higher forming voltages. Both TiN splits have slight radial fluctuations, where annealed PVD TiN (PVD+A) has the tightest distribution. The anneal step improves the metal stack characteristics in terms of defectiveness and surface contact. Because the forming voltage is approximately normally distributed, we calculated the mean values and the standard deviation of the forming voltage to estimate the expected forming voltage needed to fully form 4kb, 16kb and 1Mb matrices (Fig. 8). The predicted values change considerably depending on the selected process, underlining the importance of reducing the forming voltages and the related variabilities, especially for large arrays.

ENDURANCE VARIABILITY

Cycle-to-cycle variability for the various BE integrations was addressed by cycling three 4kb matrices per wafer for 1e4 operations. The test protocol was the following: first, a forming operation with a write and verify algorithm (target R<1MOhm) is performed with 1µs pulses of increasing BL voltages from 2V to 5V and Icc of 25µA. Next, forming operation is followed by 1µs pulses ranging from 2.0 to 3.5V with a compliance of 260µA. Then, one matrix per variant (same position) was cycled 50 times with Vset 2.0, Icc 260µA, Vreset 1.8V. The results show that PVD+A has a better low resistance state distribution and less defectiveness with respect to the CVD and W variants (Fig. 9).

Finally, a 1e4 cycles test has been performed on three 4kb matrices with 3 conditions (Tab. 2). The results with the best condition are showed in Fig. 10, where a separation of high and low resistance states can be obtained at 3σ up to 1e4 cycles for PVD+A variant. We calculated the BER (Bit Error Ratio) for each matrix as the number of error bits over the total number of read operations. A summary of the mean BER differences for the various integration methods is reported in Fig. 11, where the PVD+A is significantly better than the other variants with a number of errors generally three times lower.

CONCLUSION

We fabricated OxRAM 1T1R arrays with various metal stack deposition as bottom electrode to improve memory reliability and reduce variability. A TiN PVD, followed by an anneal process, showed lower and more controlled forming voltages with lower dispersion, and a better BER over 1e4 cycles, attributed to a more uniform bottom electrode surface along the wafer and within the die.

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CVD	PVD+A	W
TiN 350°C / TiN 100°C / TiN CVD	TiN 350°C / TiN 100°C	TiN 350°C / W 440°C / TiN 100°C
- CVD TiN at 200°C - PVD Ti+TiN at 100°C	- PVD Ti+TiN at 100°C - Anneal at 400°C (Ar)	- PVD Ti+TiN at 100°C - CVD W at 440°C

Tab. 1: *Variants of metal stack in inferior VIA of OxRAM bottom electrode studied in this work*

- Standard Foundry Wafer CMOS 130nm + 4 Cu Metal
- Bottom Electrode Definition
  - CVD
  - PVD+A
  - W
- Memory Stack Deposition (HfO2 10nm/Ti 10nm/TiN)
- Ø 300nm Mesa Patterning
- Encapsulation and CMP
- Via
- M5

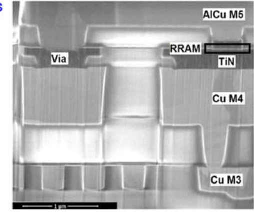


Fig. 1: *Description of the process flow and SEM cross section of the integrated OxRAM*

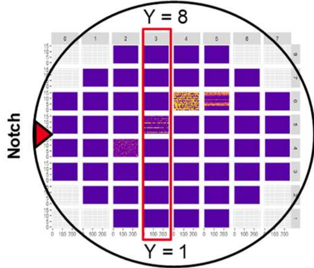


Fig. 2: *Wafer map of 8 tested matrices along the wafer diameter*

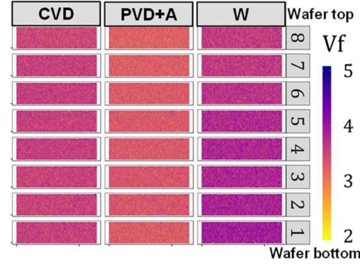


Fig. 3: *Forming voltage heat-map per variant along wafer diameter*

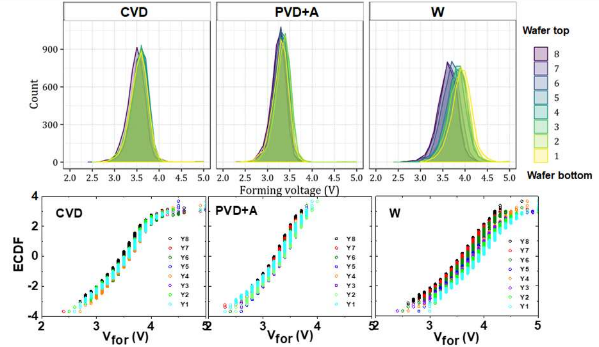


Fig. 4: *Forming voltage distribution of 4kb arrays along wafer diameter for each variant. V_{BL} from 2V to 5V with a 0.1V step*

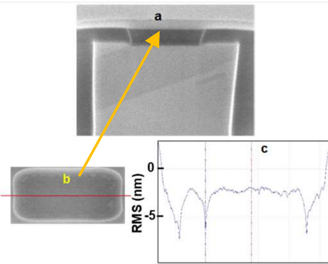


Fig. 5: *(a) SEM cross-section of inferior VIA with TiN, (b) TiN surface post CMP, (c) TiN RMS surface scan*

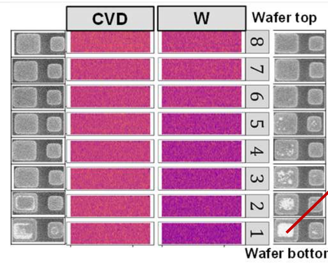


Fig. 6: *SEM observation of bottom electrode surface. For OxW, more oxide residues on the post oxide CMP surface along wafer diameter*

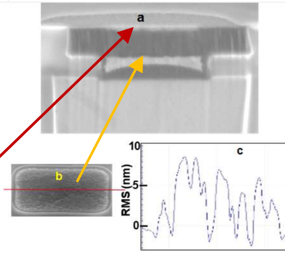


Fig. 7: *(a) SEM cross-section of OxRAM BE with W in the inferior VIA, (b) W surface post CMP, (c) W RMS surface scan*

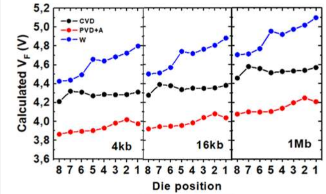


Fig. 8: *Predicted forming voltages to fully form 4kb, 16kb, 1Mb*

Conditions		
Cdt number	V_{set}	V_{reset}
1	2.1	1.8
2	2	1.8
3	2	1.7
Common: pulse width 1µs, Icc 260µA		

Tab. 2: *Summary of programming conditions applied on the tested arrays*

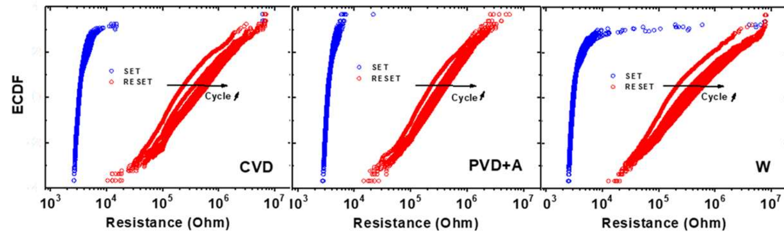
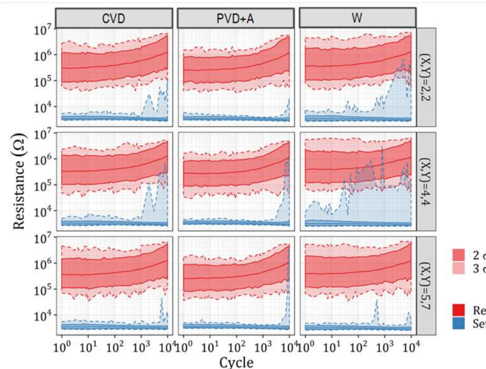


Fig. 9: *Measurement of LRS and HRS resistance distributions after 1, 10, 20, 30, 40 and 50 cycles on one matrix per wafer performed with the programming conditions of Tab. 2*

Fig. 10 (in right): *LRS and HRS resistances (median and deviations) measured during 1e4 cycles performed with the programming conditions of Tab. 2*



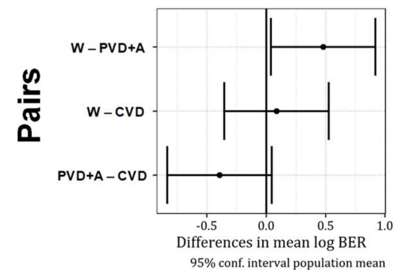


Fig. 11: *Mean BER differences between various integration methods*