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Abstract

This paper reviews a new, real-time measurement instrument dedicated for online neutron monitoring in nuclear reactors. The instrument implements the higher order Campbelling methods and self-monitoring fission chamber capabilities on an open source development board. The board includes an CPU/FPGA System On a Chip.

The feasibility of the measurement instrument was tested both in laboratory with a signal generator and in the Minerve reactor. It is shown that the instrument provides reliable and robust count rate estimation over a wide reactor power range.

The fission chamber failure detection ability is also verified, the system is able to identify whether the measured count rate change is due to the malfunction of the detector or due to the change of neutron flux. The applied method is based on the change of the frequency dependence of the fission chamber signal power spectral density, due to the malfunction. During the experimental verification, the considered malfunction was the change of the polarization voltage.

Keywords: High order Campbelling, FPGA, Measurement system, Count rate estimation
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1. Introduction

The recent development of French Sodium-cooled Fast Reactor (SFR) induces the need for new neutron flux monitoring systems in order to enhance the safety features. Given the configuration of the pool type SFR, the neutron instrumentation is planned to be set up in the reactor vessel in order to monitor the neutron flux over a few orders of magnitude [1]. The high temperature fission chambers are the best candidates for this purpose since the typical temperature in the vicinity of the core is around 500 ^{o}C [2]. This detector type was extensively studied in the CEA during the nineties and is still under active development. In addition, a research effort is currently done in order to exploit the wide flux range monitoring capability of fission chambers: it was previously shown that the use of high order Campbelling mode (HOC) provides a linear estimation of the neutron flux over a wide range of count rate by suppressing the impact of parasitic noises.

In this framework, a HOC measurement system prototype was developed at the Instrumentation, Sensors and Dosimetry Laboratory (LDCI) of CEA Cadarache. The main goal of the work is to assess the feasibility and the industrial use of such measurement system. To complete the measurement device, a fission chamber malfunction detection module (referred later as "smart-detector" capability) was included.

In this paper, the implementation of HOC method on an open source hardware development board is detailed. First, the general theory of HOC is discussed briefly and the most important advantages of its application are highlighted. The theoretical basis of the fission chamber malfunction detection is also reviewed. Second, the design of the Campbell measurement system is presented: the preference of using a open source hardware with a CPU/FPGA chip at the prototype phase are summarized; The HOC computation algorithm is explained through diagrams and clocking figures; The software dedicated to control the FPGA module is introduced. The last part of the paper is dedicated to the validation of the measurement system through laboratory measurements and in-core experimental campaigns performed at the Minerve reactor.

2. Theoretical background

2.1. High order Campbelling theoretical background

Campbell derived a theorem [3] that links the intensity of a shot noise process consisting of general pulses $f(t)$ with an amplitude distribution to

the variance of the process. The generalisation of this theorem was proposed and its complete derivation has been performed in [4, 5]:

$$s_0 = \frac{\kappa_n}{\langle x^n \rangle \int f^n(t)dt} = \frac{k_n}{C_n}. \tag{1}$$

where κ_n is the nth order cumulant of the signal, s_0 is the count rate and $\langle x^n \rangle$ stands for the nth order raw moment of the amplitude distribution. Commonly, the methods in which $n \geq 3$ are called higher order methods. Eq. (1) shows that if the pulse shape and the amplitude distribution are known (therefore the calibration coefficient C_n is determined), and the cumulant (of any order) of the signal is measured, then the mean count rate s_0 of the signal can be estimated.

In the current work, the estimation of the cumulants is performed by applying unbiased cumulant estimators, called k-statistics [6]. If the measured signal consists of N discretely sampled values Y_i, then the third order cumulant estimator is given as:

$$k_3 = \frac{2S_1^3 - 3NS_1S_2 + N^2S_3}{N(N-1)(N-2)}, \tag{2}$$

where S_1, S_2, S_3 are the first, second and third order sums of the data points defined as:

$$S_n = \sum_{i=1}^{N} Y_i^n \tag{3}$$

The performance of high order Campbelling methods have been intensively studied in [7]; it was shown that the application of higher order methods sufficiently suppresses the impact of various noises. The linearity of the count rate estimation over a wide count rate range (from 10^4 to 10^9 cps) have been verified both numerically and experimentally. It was highlighted that the application of higher than third order methods do not bring any practical advantage and accurate count rate estimation can be achieved with the third order Campbelling based on signal samples of a few ms.

2.2. Smart detector theoretical background

Eq. (1) shows that any cumulant of the signal may change not only due to the change in the count rate, but also due to the change in the mean pulse shape or in the amplitude distribution. The higher order methods are particularly sensitive to these changes because of the higher exponents in Eq. (1). The change of the pulse shape and its amplitude may occur due to a malfunction, such as the reduction of detector pressure or voltage since

these result a change in the electron drift velocity. During the measurement only the change of the cumulant (therefore the change of the estimated count rate) will be detected, thus we have to be able to decide whether this change occurred due to the change of the neutron flux around the detector or due to the malfunction of the detector.

Therefore we have to define a measurable quantity of the fission chamber signal which is sensitive to the pulse shape change but not to the count rate change. As a previous study shows [**?**], the width of the power spectral density (PSD) of the detector signal satisfies this requirement. In this work the PSD of a signal $y(t)$ is defined as:

$$PSD(f) = \frac{FT(y)FT^*(y)}{T_m} \tag{4}$$

where FT stands for the Fourier transform, and T_m is the measurement time

It was shown that by measuring the width of the PSD, one can detect the change of the pulse shape due to the leakage of the filling gas. The spectral width was defined as the width at the half maximum of the PSD, it is usually contained in the 0-20 MHz band, which is an easily accessible frequency band with the modern instrumentation.

3. Design of high order Campbelling measurement system

The development of an on-line neutron monitoring system, which makes use of fission chamber signals and works in higher order Campbell mode, requires:

- Capability to convert and process the signal at the output of the available pre-amplifier (between -10 and 10 V for the typical nuclear instrumentation).
- Real-time computation of the first, second and third order sum of the signal (see Eq. (3)).
- High sampling frequency in order to resolve the signal consisting of pulses with a width of a few tens of nanoseconds.
- Ability to process a large amount of data in real-time (given that a time window of a few ms has to be applied for accurate estimations).

Since this work aims to develop a prototype system and provide proof of concept, two additional requirements have to be considered:

- Versatility in order to modify the prototype easily and test new implementations.
- Large user community and preferably open source philosophy in order to facilitate the learning and to get fast technical support.

3.1. Hardware selection

Recently several single board computers and system on a chip (SoC) boards revolutionized and facilitated the development of digital measurement instruments. Based on the above defined criteria, the Red-Pitaya board was chosen; it was created to provide a customizable measurement system with a generous amount of examples according to the open source philosophy. Due to its low footprint, low price and relatively large user community, it fulfills all the requirements which were expected at the prototype stage.

The Red-Pitaya board is built around a Xilinx Zync 7010 SoC which embeds an FPGA and a dual core Arm CPU clocked at 668 MHz. The Red-Pitaya board hosts two Analog-to-Digital Converters (ADC) and two Digital-to-Analog Converters (DAC) which are directly connected to the FPGA. The ADCs have a sampling frequency of 125 MHz and a resolution of 14 bits. The board provides two measurement ranges through jumper positions: $\pm 0.6\,\mathrm{V}$ and $\pm 16\,\mathrm{V}$. The great strength of the FPGA is letting to design a circuit, which allows to process the data in line, therefore reducing the time, and the memory storage for heavy computations. This makes FPGAs ideal to perform simple computing patterns on a vast amount of data in real time. These characteristics fulfill all the above stated requirements to develop an online neutron monitoring system: the board is able to process the signal at output of the most common pre-amplifier(0,10 V for the CEA PADF and -10,0 V for the Canberra ADS pre-amplifiers applied in this work), to resolve the fission chamber pulses (with a length of few tens of ns), and to perform the real-time processing of large amount of data.

It has to be mentioned, that although it may seem that the CPU could handle all the data processing needed to calculate the high order sums of the signal, the real time computation with the CPU couldn't be realized due to the huge amount of data transfer and operations ($\approx$ 750[Mop/s]) it implies. Therefore, in the neutron monitoring instrument, the FPGA was dedicated to the low level, time critical, redundant operations (namely computing the power sums of the signal values), whereas more complicated operations were performed on the CPU.

The FPGA of the board is configured using Verilog, a low level Hardware Description Language (HDL), and the softwares running on the CPU are developed in C language. It has to be recognized that development with a

hardware description language is more cumbersome than with a normal procedural language (the main constraints are detailed in the following section). Thus, during the design of the instrument the use of the low level computing was kept to a reasonable minimum, in order to facilitate the development and the maintainability of the device while keeping CPU computing power for prospective data processing. The following sections are devoted to explain the inner design of the new measurement system.

3.2. Third order cumulant measurement system

The most time consuming operations, while computing the third order cumulant estimator k_3 (Eq. 2), are the computations of the sums S_1, S_2 and S_3 (Eq. 3), since the higher order power of each signal sample is required in real-time. On the other hand, the further operations to compute the estimator k_3 based on the sums, has to be done only once at the end of the measurement time and don't exhibit any simple computational patterns. Consequently, the real-time computation of the sum terms were realized on the FPGA, and, after the transfer of the sums to the CPU, the final operations to compute the cumulant estimator were performed by a control software running on the CPU.

The developed FPGA module of the measurement system is composed of five algorithmic blocks. Two blocks are dedicated to read and write data for the Processing System (PS, i.e. the computer part of the SOC). One block is in control of the measurement soft reset. Two blocks are directly related to computation of the third order cumulant estimator terms. The function and the realisation of the last two blocks are detailed below.

3.2.1. Unbiased cumulant estimation FPGA module

The algorithm design starts with the definition of registers (variables used to store data): `S1`, `S2` and `S3` contain respectively the sum of single, square and cubic power of the samples for `N` number of samples. It is favorable to limit the number of samples to a power of 2 to simplify division by `N` into bit shifting operation. It was shown previously that the proper measurement time for the cumulant was between a hundred of micro-seconds and a few tens of millisecond [7], in terms of number of samples, this corresponds to N between 2^{22} (33.5 ms) and 2^{14} (131 μs) if the sampling frequency is 125 MHz; Register `N` size was set to 23 bits.

The sizes of `S1`, `S2` and `S3` have to be carefully defined as well, since their sizes have to be adequately large in order to avoid overflows. The development board provides two's complement signed 14 bits samples, an addition of two samples has to be stored on 15 bits, where as their multiplication is

stored on 28 bits. This implies that `S1`, which contains up to `N` summed data has to be 36 bits wide because of the maximum value of `N`, which is 2^{22}. `S2` and `S3` must be 50 and 64 bits wide in order to contain respectively the sum of square and cubic power of samples.

Once each used register has the proper size, the algorithm can be designed. Two important constraints have to be taken into account at the low level computing. First, every operation in an algorithmic block is performed in parallel during a clock tick; the results of the operations will be available at the end of the clock tick which prohibits the use of regular procedural programming. However, branching (i.e. conditional tests) does not consume any computation time. Second, only one operand can be used in an operation; it implies to pipeline the computation of square and cubic power over several clock ticks.

Fig. 1 summarizes the implemented algorithm: the main algorithmic block contains a loop dedicated to the computation of the sums. To provide a better understanding of the time operation of the algorithm, Fig. 2 illustrates is clocking diagram for $N = 4$.

At each clock tick, the data stream coming from the ADC (`adc_a`) is stored into two temporary registers (`single` contains the ADC value and `double`↩ contains the square of the ADC value), which are used to pipeline the power computation. In the same time, `adc_a` is added to `S1`, `double` to `S2` and `triple` to `S3` (`triple` is also a temporary register dedicated to store the cubic power of samples, it is fed with the result of the multiplication `single*double`).

A sample counter (`sample`) is incremented at each cycle to keep track of the amount of samples processed since the start of the current measurement. When `sample` is equal to `N`, the completion process and the transfer of `S1`, `S2`, `S3` to registers accessible by the PS (namely `S1mem`, `S2mem`, `S3mem`) begins. To transfer the sums to the area from which the data transfer towards the CPU takes place, intermediate registers (namely `S1inter`, `S2inter`, `S3inter`) have to be used to store the sums due to the pipelining. The reason is that the final values of `S2` and `S3` will be available respectively one and two clock ticks after `S1`, however, the data transfer has to be done in one clock cycle in order not to mix old and new data in registers where the CPU has access.

To achieve the transfer, first the flag `data_transfer` responsible for data transfer from intermediate registers to the memory area accessible by CPUs is set to false. In the same clock tick when the `sample` is equal to N, the flag specifying the availability of `S1` (`S1ready`) is set to true, while the flags indicating the availability of `S2` and `S3` (`S2ready` and `S3ready`) are set to `false`.

In the next clock tick, a test `S1ready==true` allows `S1` to be transferred to the intermediate register `S1inter`, while the computation of `S1` restarts.

At the same time, `S2ready` is set to true since `S2` will be ready for the next tick. During the following tick, a test `S2ready==true` allows `S2` to be copied to `S2inter` and its computation restarts, while `S3ready` is also set to `true`. In the next clock tick, the test `S3ready==true` is verified and the copy of `S3` to `S3interm` is performed; a register which keeps track of measurement time (`time_stamp`) is also incremented and the flag `data_transfer` is reset to `true`. All the sums can now be copied from intermediate registers to the ones accessible by the PS (the algorithmic block responsible for this transfer is summarized in Fig.3)), while the registers containing the sums, `S1`, `S2`, `S3` are already filled with the data of the new measurement.

3.2.2. Control software of the High Order Campbelling module

A software was written in a high level programming language to control the FPGA module. Its main task is to read the data provided by the FPGA at the designated memory addresses, to construct the estimator $k3$ and to make it available for further processing. At this phase, two constraints have to be considered to fulfill the requirements of real-time monitoring: first, the software must be capable to construct the estimator in a time window shorter than the duration of the measurement without being slowed down by the post-processing of data. Second, it should not miss any measurement and should store each result produced in the memory for further processing.

In order to fulfill these requirements, the software design uses two threads, which allow to take advantage of the dual core architecture. One transfers the available measurement into the memory of the PS: it reads the time stamp computed by the FPGA, and if this time is larger than the one stored in computer memory, $S1$, $S2$ and $S3$ are transferred and $k3$ estimation is constructed. The second thread is responsible for heavy and slow processes such as printing and saving the cumulant estimator. It has only access to the data provided by the measurement thread. In order not to lose data, a FIFO (First In First Out) pile can be used by the measurement thread to store the terms of the cumulant. Both threads are detailed through diagrams available in Fig. 4 and Fig. 5.

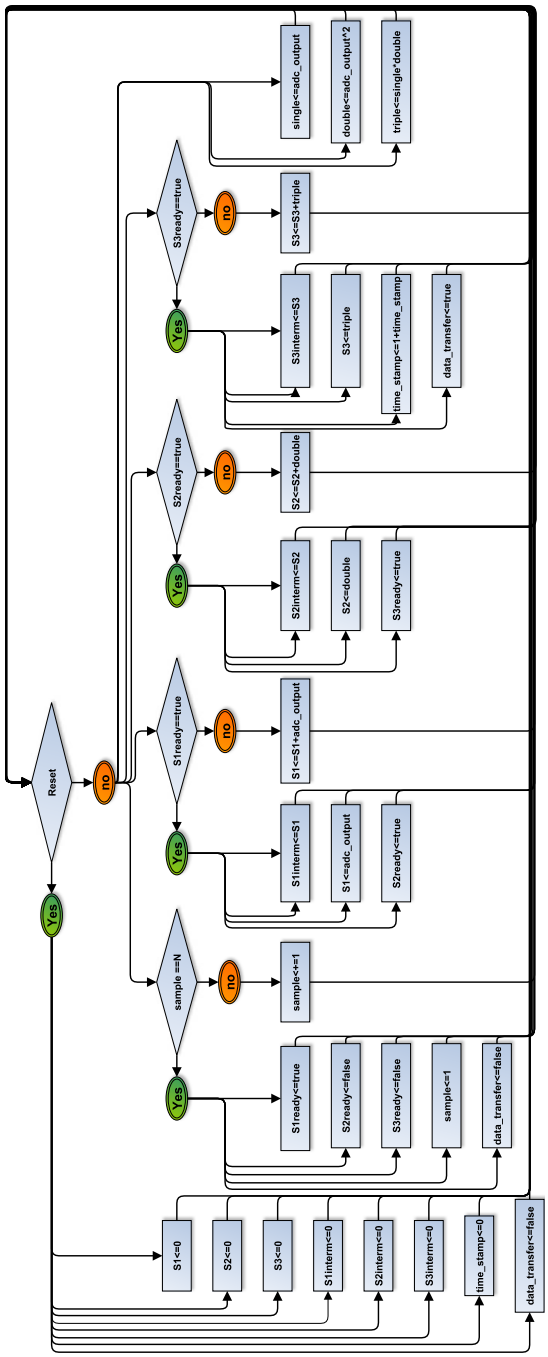

Figure 1: The algorithm for the computation of the terms of the estimator $k3$: $S1$, $S2$ and $S3$.

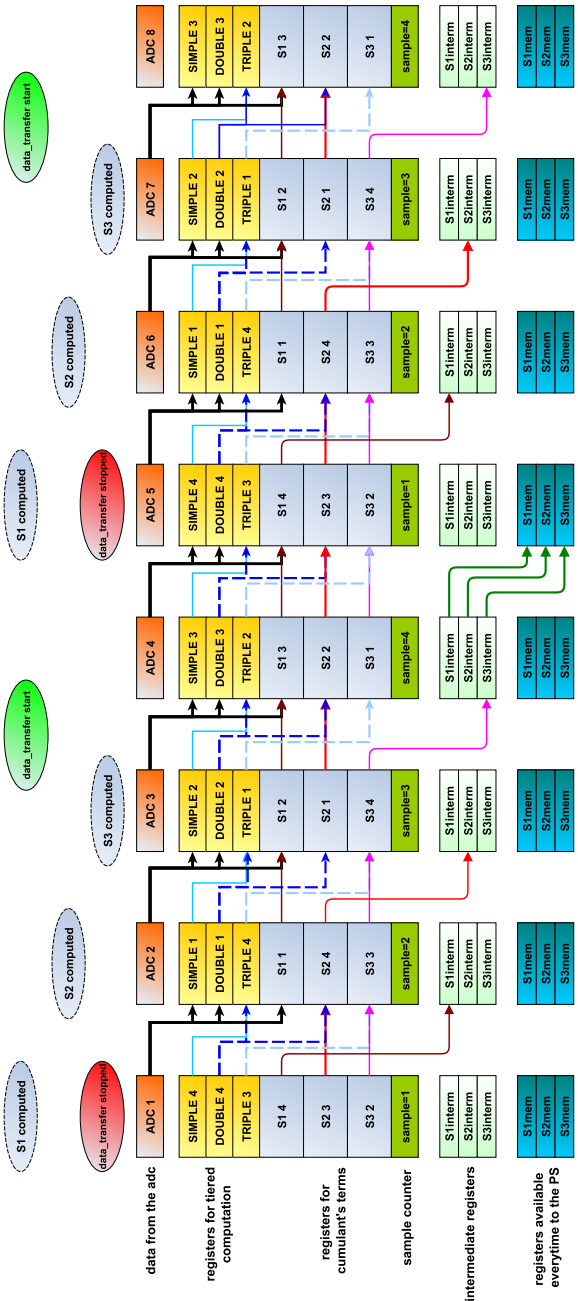

Figure 2: Clocking diagram of the algorithm for computation of the cumulant terms. For the sake of simplicity, the number of samples per measurement is set to $N = 4$. The squares represent the state of registers at each tick while the arrows summarize the operation performed during the tick. Bubbles at the top of the diagram are related to flags for finishing the computation and initiating memory transfer.

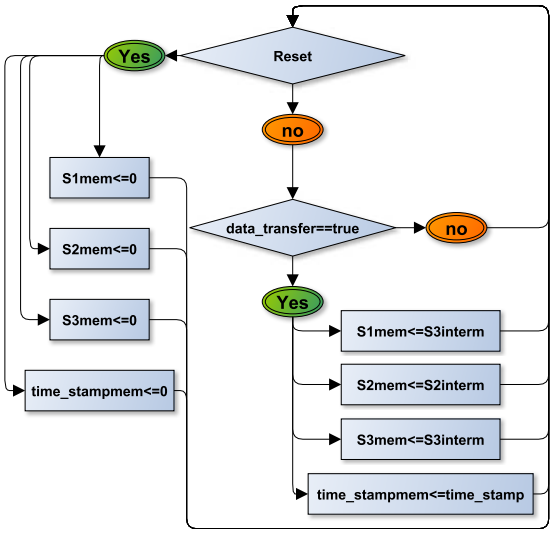

Figure 3: Diagram of the algorithmic block dedicated to transfer data from the computing block to the block in charge of communication between the FPGA and the PS.

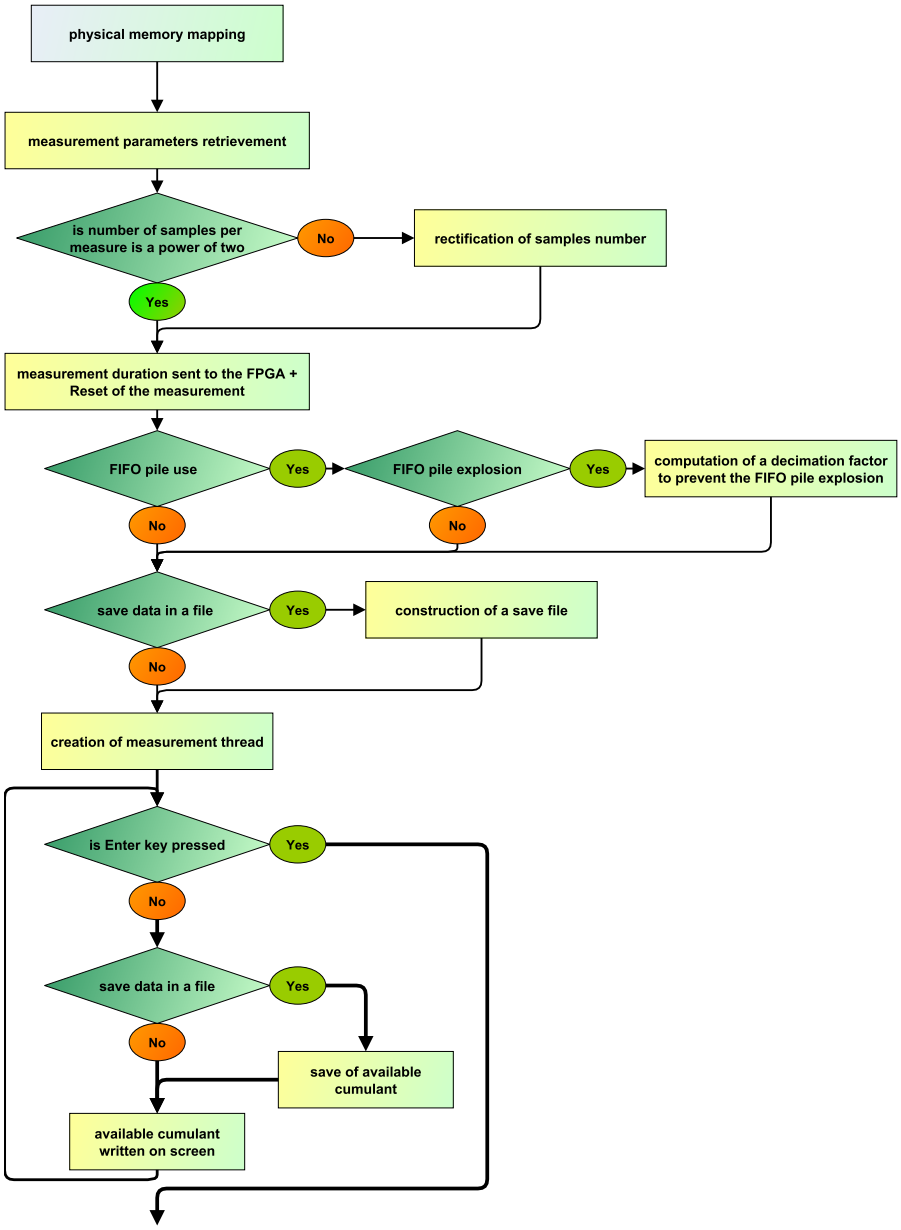

Figure 4: Diagram of the HOC measurement system control software.

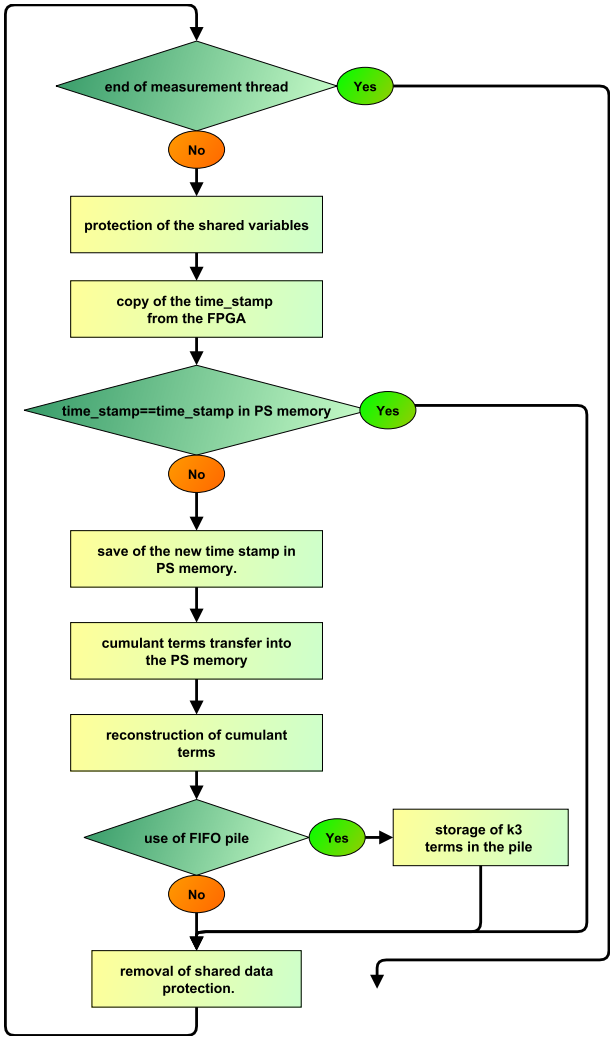

Figure 5: The measurement loop schematized here is called by the measurement thread independently from the main software.

3.3. Smart detector system

The measurement prototype was completed with smart detector capabilities in order to detect the change in the width of the power spectral density, which indicates a possible malfunction during operation.

As it was shown previously [8], it is satisfactory to monitor the power spectral density on the s time scale. In order to minimize the necessary change in the FPGA modules developed for the higher order cumulant computations, in the smart detector module, the FPGA (controlled by the PS) is responsible only for recording the raw data. The complex data processing, such as computing the PSD and determining its width, is done on the CPU with specific C routines from the GSL (GNU Scientific Library) [9].

3.3.1. Smart detector FPGA module

The hardware part of the smart detector module consist of a punctual raw data recorder which makes use of the block RAM available on the FPGA; the Artix-7 have 60 blocks of 36 kB RAM which can have a limited set of configuration [10]: Since the data coming from the ADC are 14 bits wide, only 2^{16} data points (0.524 ms) can be stored in the memory.

The FPGA module is constructed from three algorithmic blocks available in Fig. 6: the first one stores ADC data into a memory buffer, while the second and third one deal respectively with data transfer to the PS and with message dispatching through the smart detector module.

For the sake of simplicity, it was decided to use the memory transfer algorithm included in the Red-Pitaya project and a serialised architecture to move data buffer from the FPGA to the PS: The PS sends the memory address to be read and the memory transfer code block makes ready the related data (`buff[yraw_read_addr]`) for an eventual read command.

Even with a limited signal length and slow memory transfer ($\approx$ 12.5 Mdata/s), this architecture is suitable for the fission chamber failure detection. Nevertheless, in the future, it is possible to improve this module: since the granularity of memory transfer is 32 bits, transferring more than one 14 bits of useful data in a clock tick could speed up the transfer to the PS by a factor 2.

3.3.2. Control software of the smart detector module

The control software of the campbell measurement system was extended in order to include the smart detector capabilities. The general architecture remains the same: two threads are running on the two cores of the CPU. One is dedicated to the measurement and only does lightweight processing while the other is related to heavy data processing (as shown in Fig.7). A

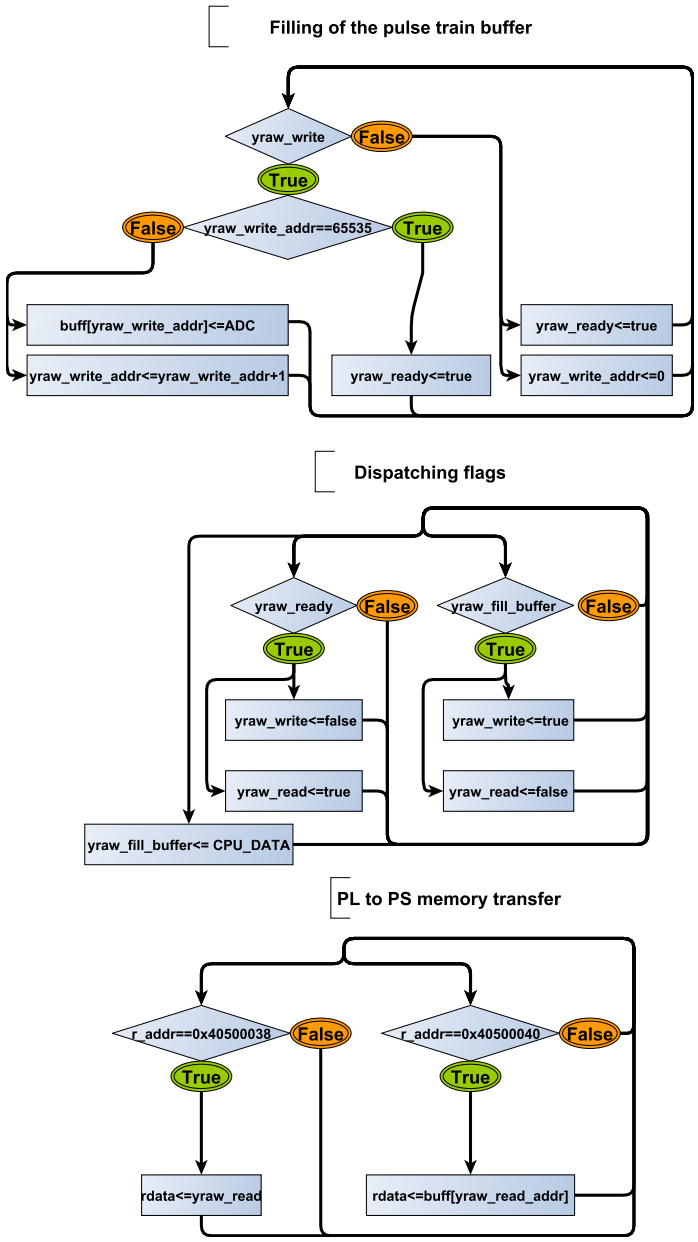

Figure 6: Smart detector algorithm implemented on the FPGA. The register `ADC` represents a raw sample.

flag set by the user at the program start-up (`compute_psd`) allows to enable the smart detector module.

The measurement thread was adapted to transfer signal segments: one flag is shared with the data processing thread, `psd_compute_flag` is used to notify the FPGA that the signal buffer has to be filled. Then, the measurement thread checks periodically if the data buffer is ready. Once it is ready, the data is transferred. When a complete signal segment has been transferred, the measurement thread indicates it with `psd_compute_flag`.

The data processing thread is in charge of PSD computation. When the buffer data is ready to be processed, the thread proceeds to the PSD computation after requesting a new signal segment. The spectrum is computed using the Bartlett's method. When the the amount of computed spectra reaches `MAX_PSD`, the average spectrum is computed, and the width of the spectrum is estimated. Finally, the mean spectrum is saved on the disk.

4. Experimental validation

The measurement system prototype was tested through several experiments. During the development phase, experiments in laboratory were performed to check whether the FPGA modules are well implemented. Finally, the measurement system was connected to fission chambers and tested in the Minerve reactor under real working conditions. The measurements and the obtained results are detailed in the following sections.

4.1. Laboratory validation

4.1.1. Validation of the HOC measurement system

The validation of the HOC measurement system was done in two steps. In the first step, the proper computation and transfer of $S1$, $S2$ and $S3$ was checked by replacing the ADC input data by a constant value of 2. It was verified that for N samples, the computed sums S_1, S_2 and S_3 are equal to $2N$, $4N$ and $8N$ respectively.

In the second step, the accuracy of the third order cumulant estimation was tested with Poisson pulse trains simulated by a pulse train generator. The pulse trains consisted of exponential damped pulses with a width of around 100 ns and a random normally distributed amplitude. The count rates were varying between $4 \cdot 10^5$ to $4 \cdot 10^7$ c/s. The pulse trains were loaded (in the proper format) and played by a Tektronix AWG 5012 signal generator. The datasets were 0.128 second long, with a sampling time of 8 ns and the pulse amplitude selected to be consistent with the output of a typical fission chamber measurement chain (3% of the $\pm$16 V range were used). For

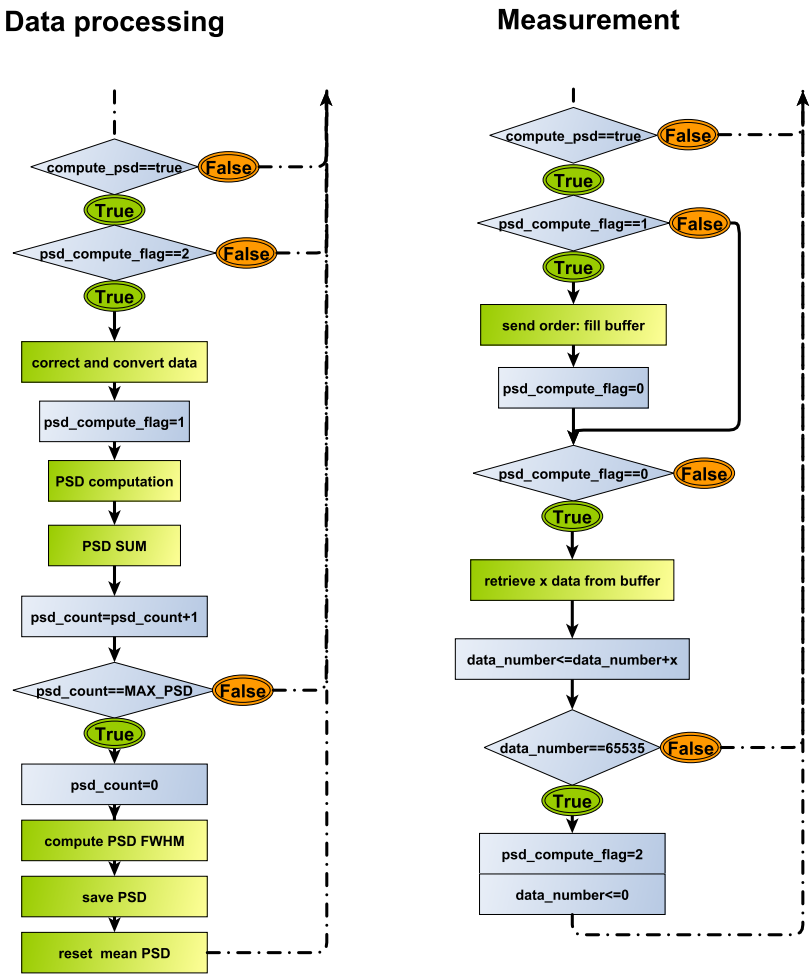

Figure 7: The control software dedicated to the smart detector module. (Only the measurement thread communicates with the FPGA smart detector module, even if the request for a new measurment is sent through the shared variable `psd_compute_flag` by the data processing thread.)

each pulse train, the third order cumulant estimator was computed before uploading to the signal generator and compared with the estimation of the measurement system. The results are summarized in the Table 1.

The measured third order cumulants are close to the computed ones. A maximum of 3.5 % of relative overestimation was found during these tests. The discrepancy is most probably due to the electronics transfer function and the truncation made by the ADC. Investigations has shown that the transfer function results a slight reshaping, therefore the measured estimation is slightly higher then the computed cumulant. Nevertheless, in practical situations the calibration methodology will inherently take into account the reshaping, hence the count rate will not be overestimated.

c. rate (c/s)	$k3$ (computed)	$k3_a$ (measurement)	$k3_b$ (measurement) μs
$4 \cdot 10^6$	$2.84 \cdot 10^{-5}$	$(2.90 \pm 0.01) \cdot 10^{-5}$	$(2.91 \pm 0.19) \cdot 10^{-5}$
$4 \cdot 10^7$	$5.70 \cdot 10^{-5}$	$(5.85 \pm 0.02) \cdot 10^{-5}$	$(5.86 \pm 0.36) \cdot 10^{-5}$
$4 \cdot 10^6$	$3.22 \cdot 10^{-5}$	$(3.33 \pm 0.02) \cdot 10^{-5}$	$(3.37 \pm 0.27) \cdot 10^{-5}$
$4 \cdot 10^5$	$1.15 \cdot 10^{-5}$	$(1.19 \pm 0.02) \cdot 10^{-5}$	$(1.27 \pm 0.27) \cdot 10^{-5}$

Table 1: Computed and measured third order estimators for pulse trains at various count rates. $k3_a$ refers to the estimation based on 34 ms samples and $k3_b$ refers to the estimation based on 262 μs samples.

4.1.2. Smart detector module validation

In order to test the smart detector module, and the PSD measurement capabilities of the system, several pulse trains with a length of 0.128 s were simulated, and played with the signal generator. The trains contained Gaussian shaped pulses with a mean count rate of 10^6 c/s. The width (i.e. the standard deviation of the Gaussian) of the pulses were changed (5 ns, 10 ns and 15 ns were considered).

The obtained power spectral densities are available in Fig.8. As it can be seen, the spectrum shape is characteristic of the pulse shape. The line centered around 1 MHz and its harmonics are artifacts due to the fact the same 0.128 s signal was played periodically. The functioning of the smart detector module was appropriate.

4.2. In reactor validation

Finally, the measurement device was tested during an experimental campaign at the Minerve facility of CEA [11].

Several setups were realized in order to assess the compatibility of the device with the standard nuclear instrumentation. During the campaign,

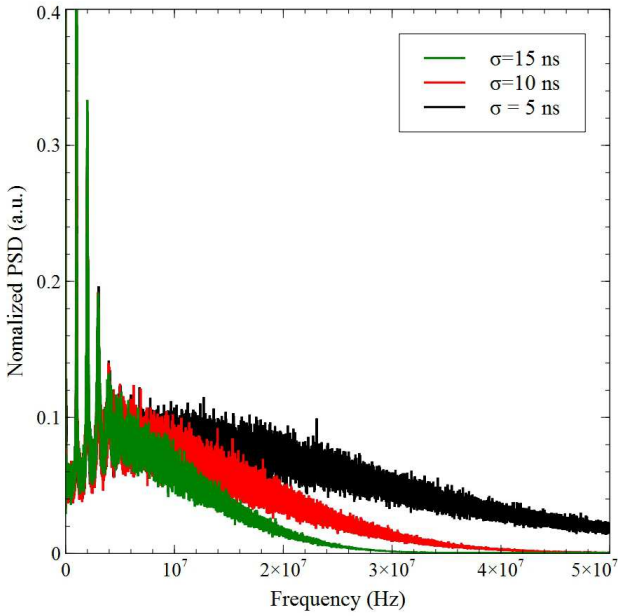

Figure 8: PSD obtained with simulated pulse trains.

two pre-amplifiers were used: the ADS, manufactured by Canberra and the PADF designed by the CEA instrumentation and electronics laboratory. These pre-amplifiers are different in their output voltage and transfer function.

In order to cover a wide count rate range, two type of fission chambers were tested during the experiments: the CFUL01 (a relatively large chamber, which contains 1g of U235; its pulse shape is around 80 ns wide) and the CFUR (a rather small chamber, which contains $10\mu g$ of U235; its pulse shape is around 20 ns wide). At the same neutron flux, the CFUR chamber results 5 orders of magnitude lower count rate than the CFUL01.

The CFUL01 chamber was located in the surrounding of the driver zone, whereas the CFUR was installed in the center of the reactor.

During the campaign, the following experiments were performed in order to assess various aspects of the measurement device:

- Cumulant estimation with the CFUL01 and the PADF at various power levels: to assess the linearity of the measurement system.
- Cumulant estimation with the CFUR and the PADF at various power

levels: to assess the limits of the system at low count rates.

- Pulse train recording with the CFUR and the PADF at various power levels: to calibrate the HOC system (in order to retrieve the count rate with the higher order method), and to estimate the count rate with pulse counting algorithms.

- PSD measurement with the CFUL01 and the ADS pre-amplifier with various bias voltages: to simulate a detector failure and to measure the change of the spectral width.

4.2.1. Third order cumulant measurements, CFUL01/PADF

The third order cumulant has been estimated at reactor powers between 10 W and 80 W with the CFUL01, based on 33 ms time windows. Both the ± 0.6 V and the ± 16 V input ranges have been used, in order to assess the linearity with both ranges.

The signal saturates at 30 W reactor power, when measured with low voltage range. Therefore, only two measurements were done with this range (at 10 W and 20 W). The cumulant over power ratios are $(4.04 \pm 0.36)\ 10^6$ (a.u.).W^{-1} and $(4.11 \pm 0.28)\ 10^6$ (a.u.).W^{-1} for the 10 W and 20 W power, respectively. Although, in the future a better resolution of the power is needed to draw deeper conclusion, the good agreement of the ratios implies that the behavior is linear.

With the ± 16 V range the whole power range was covered. The obtained cumulant estimations are presented in Fig.9. The measured third order cumulant shows linearity with the reactor power. The departure from linearity is lower than 1.6 %, which is the result of the random error of the estimation. In order to estimate the count rate, the measurement chain has to be calibrated. The calibration, through applying the methodology described in [12] (namely, to evaluate the coefficient C_n in Eq. (1) by measuring the mean pulse and the pulse amplitude distribution at low power), was planned to be done during the post-processing of recorded signal samples. Unfortunately, for this purpose the signal was recorded with the high voltage range, which was not appropriate to discriminate properly the single pulses from the noise. In the future, when further reactor time can be obtained for similar measurement purpose, the calibration is going to be repeated with the low voltage range as well. In order to avoid similar problems, also a new calibration procedure is under development, which can be performed during the real-time operation, and does not require post-processing. Nevertheless, the measurement with the CFUL01 was still valuable to assess the linear cumulant estimation of the measurement device.

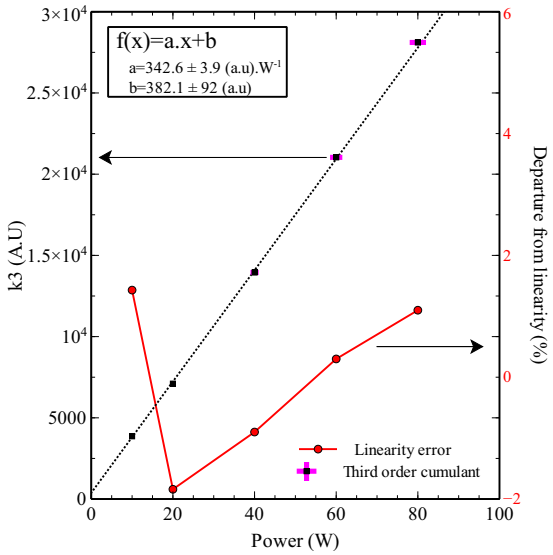

Figure 9: Third order cumulant recorded with the ±16V range as a function of the reactor power.

4.2.2. Third order cumulant measurements, CFUR/PADF

Measurements with the CFUR chamber were performed only with the low voltage range, since the count rate of the signal was expected to be rather low on the power range of Minerve.

The measurements were done at 40 W and 80 W power level. The results are summarized in Table 2. The cumulant estimation based on one 33 ms long sample results a high standard deviation, which is expected since at these count rates only few pulses appear during one sample, and the number of observed pulses is uncertain. Nevertheless, the expected value of the cumulant estimator was based on 1900, 33 ms long signal samples, therefore the overall deviation of the estimated mean cumulant is less than 2.3%. (In comparison, when the reactor was all control rods down and estimation was based only on the noise in the system, the estimated third order cumulant appeared to be 350 ± 50, which is less than the deviation of the cumulant estimation for the fission chamber signal). The mean cumulant over the power ratios show good agreement, which implies linear behaviour. For the estimated count rates (discussed later), the deviation refers to the $400 \cdot 0.52$ ms sample, not only to one sample.

To calibrate the fission chamber through the methodology presented

Table 2: Cumulant and count rate estimations with the HOC module and with pulse counting.

Power (W)	k_3 (a.u.)	$\langle k_3 \rangle / P$ (a.u.).W^{-1}	HOC count rate c/s	Ref. count rate c.s
40	(1.18± 0.39)10^4	295±12	3430± 354	(2861±118)
80	(2.38±0.56) 10^4	297±10	6918± 686	(6103± 171)

in Ref. [12], the raw signal recorder module dedicated to smart detector was used, with a minimalist control software. Several signal segments were recorded at 80 W and the pulses were isolated during post-processing in order to determine the calibration coefficient in (1). From the measurements nearly 2700 pulses were isolated, which allows to have acceptable statistics. The mean pulse shape and the amplitude distribution of the pulses is illustrated in Fig. 10. As one can see, the dynamic of the measurement system allows to discriminate the pulses from the noise and the resolution is fine enough to observe even the current bouncing back from the cable (a small bump following the main pulse). The prototype is capable of working as a raw signal recorder as well. The estimated calibration coefficient for the third order is:

$$C_{clas} = 3.44 \pm 0.3 \ (a.u.).s/c \tag{5}$$

The calibration has large uncertainty, which shows the disadvantage of this methodology. As it was highlighted in Ref. [12] as well, for the high order methods an empirical calibration may be favorable. Such calibration is not plausible for the traditional Campbelling method, due to the linearity gap between pulse counting methods and the second order Campbelling.

In order to obtain a reference count rate, 400 signal segments recorded at a reactor power of 80W and 400 recorded at a power of 40 W were analyzed with pulse counting method as well. The estimated count rates obtained by pulse counting, and the ones computed from the calibrated higher order Campbelling are included in Table 2. It has to be highlighted again that the standard deviation refers to the $400 \cdot 0.52$ms long signal sample for the counting algorithm result while it is related to the $1900 \cdot 33$ ms long signal for the calibrated HOC. The standard deviation of an estimation based on one 0.52 ms sample is much higher for the pulse count, but the goal was to define the reference (i.e. the real) count rate of the chamber at these powers. The good agreement of the estimated count rates show that the results measured

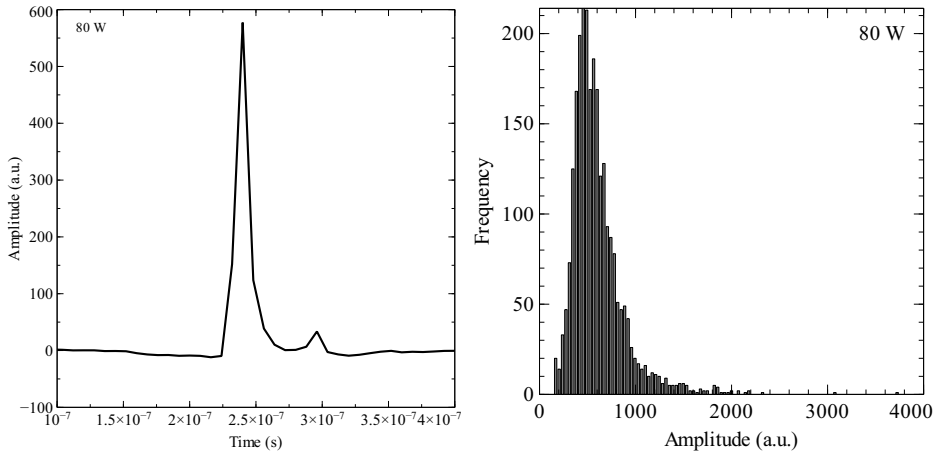

Figure 10: Left: mean pulse shape computed with single pulses coming from the 80 W measurement data. Right: amplitude distribution of pulses computed on datasets recorded at 80 W.

by the system are physically correct. The results also imply that monitoring at really low count rates (in the order of 10^3 cps) is possible with higher order Campbelling, but longer measurements are necessary (nevertheless, the same holds for pulse mode measurements as well).

4.2.3. PSD measurements, CFUL01/ADS

When the tests of the smart detector module were performed, only the ADS preamplifier were available, which allowed to verify that the device is capable to work with other instruments as well.

The ADS pre-amplifier and a CFUL01 chamber were used to test the smart detector module. Using the CFUL01 was advantageous for this purpose, since it has a higher count rate, therefore its power spectral density can measured more accurately during real time operation.

In the current experimental work, the change of the pulse shape was achieved by changing the fission chamber voltage in the saturation regime. The increase of the voltage has similar effects on the pulse width as the decrease of the gas pressure, but it is simpler to achieve during the measurement.

Measurements were taken at a constant reactor power of 20 W with the voltage changed between 600 V and 850 V. For each applied voltage, the PSD was constructed by using 4000 datasets of 0.52 ms long signals. The low vari-

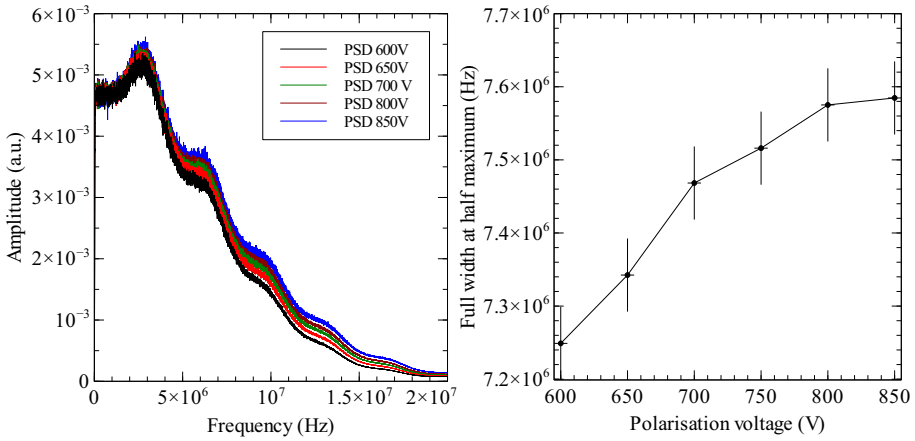

Figure 11: Left: PSD as a function of the applied voltage. Right: Spectral width as a function of the polarisation voltage.

ance of the spectra estimated from this amount of data, allows to distinguish change in the spectral as small as 50 kHz. The measured PSD and the estimated spectral width are presented in Fig.11. The slight oscillation of the PSD is an artifact due to the applied cable. As expected, the spectral width increases with the increase of the applied voltage, and it saturates at high voltages. The reason of the saturation of the spectral width is the saturation of electron drift velocity in argon-nitrogen mixtures at high reduced electric fields [13].

Therefore, the proof of concept of the smart detector is validated: it is possible to detect a change of mean pulse shape from investigating the power spectral density, whereas the measurement noise and the low frequency filtering of the system have negligible influence on the determination of the spectral width.

Although, in the current experiment, the time needed to record and process the 4000 datasets is approximately 300 s due to the slow data transfer, this already allows to test in every 5 minutes whether the chamber malfunctions. However, the processing time of the smart detector prototype could be reduced by a factor of 3 by using optimised FFT routines, and in the future even faster tests can be achieved for the industrial application by implementing the same method on board with higher performance.

5. Conclusion

An innovative measurement system prototype for real time neutron monitoring was presented and validated through this paper. The prototype was built using an open source CPU/FPGA device with ADC on board. Such architecture has a several advantages: time critical, simple operations can be performed on the FPGA, immediately after recording the data, whereas complex and heavy data processing can be performed on the CPU. The simplicity of the chosen board (Red-Pitaya) allowed fast and straightforward development.

The main purpose was to prove the feasibility of a real time neutron flux monitoring system using the third order Campbell mode. This method suppresses the impact of noise and provides wide range of operation. In this work it was shown that the method is even capable to work at count rates as low as 10^3 cps.

In the work, the concept of fission chamber failure detection was also included. The self monitoring capability of the system is based on detected the change in the width of the power spectral density of the signal.

The paper provides detailed description of the implemented FPGA algorithms and the control software running on the CPU. All the challenges and solutions were highlighted in order to serve as a tutorial for similar developments.

The reliability of the concepts and the robustness of the device was tested through an experimental campaign at the Minerve reactor. The linear response and the real time operation of the device was verified over a wide power range. Through the calibration of the system the physical validity of the measured results was assessed. The self monitoring capability was also tested, the system is capable to detect the change in the voltage set between the electrodes of the chamber.

Since the calibration of the system is rather elaborate, a simpler, automatic and real time calibration procedure is under development.

For industrial usage, the next step is going to be the implementation of the same concepts on a board which has higher performance in order to achieve faster self monitoring capability.

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