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# Doping profile extraction in thin SOI films: application to A2RAM

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**Abstract**—We propose for the first time a method based on C-V measurement to extract the bridge doping profile which governs the A2RAM performances. Assessed with TCAD simulation and simple extraction model adapted from bulk devices, this technique is validated with experimental data.

**Keywords**— A2RAM; C-V characteristic; SOI; electrical characterization, doping profile.

## I. INTRODUCTION

The A2RAM (Fig.1) is a 1T-DRAM [1] with an N-doped layer (nMOS case) called ‘the bridge’ located at the bottom of the low-doped p-type body. The bridge allows short-circuiting the source and drain. The concept of A2RAM has been presented in [2] and its experimental performance in [3]. Recently, the scalability issues of the A2RAM have been studied by TCAD simulations [4]. We noticed some inconsistencies with measurements, presumably related to the mismatch of the bridge doping profile between TCAD simulations and experiments. As the A2RAM behavior is strongly related to these parameters, we need an accurate solution to evaluate them. The use of physical characterization such as Secondary-Ion Mass Spectroscopy (SIMS) is not reliable here because (i) the silicon film is too thin and (ii) the target doping is too low (around  $10^{18}\text{cm}^{-3}$ ). Thus we need a method based on electrical measurement. For this purpose, the C-V electrical characterization is emulated through TCAD simulations and validated with experiments.

## II. A2RAM: TCAD SIMULATION METHODOLOGY AND C-V CHARACTERISTIC

We simulate the A2RAM structure (Fig. 1) as fabricated in [3] with Synopsys TCAD tools [5] using the same models as in [4].

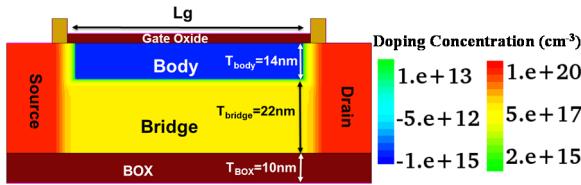


Figure 1. Simulated A2RAM cell with parameters defined by the process flow in [3].

The main technological parameters are: abrupt Gaussian doping profiles, body thickness  $T_{\text{body}} = 14$  nm, bridge thickness

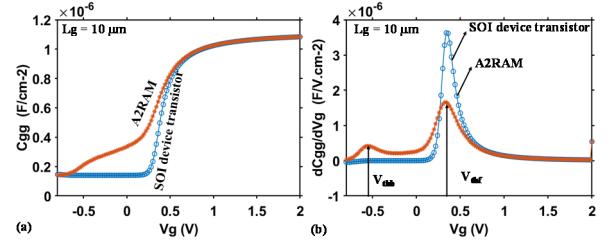


Figure 2. (a) C(V<sub>g</sub>) characteristic of the A2RAM and standard SOI transistor with same silicon thickness but no doped bridge. (b) First derivative of the C-V curves.

$T_{\text{bridge}} = 22$  nm, bridge doping  $N_{\text{bridge}} = 10^{18} \text{ cm}^{-3}$ , Equivalent Oxide Thickness EOT = 3.1 nm and Buried Oxide thickness (BOX)  $T_{\text{BOX}} = 10$  nm. We performed small signal simulation and report on Fig.2-(a) the gate capacitance  $C_{\text{gg}}$  versus the gate voltage  $V_g$  for both the A2RAM and a standard SOI device transistor. Similarly to a back-biased FD SOI devices with an inverted back channel, the A2RAM C-V characteristic shows a double hump related to the presence of the inversion charge at back and front interfaces. It is possible to define the threshold voltage for the formation of these channels. Fig.2-(b) shows the first derivative of the C-V curves. When the front-gate bias increases, the first hump is related to the ‘conduction of the bridge’ at  $V_{\text{thb}}$  and the second one to the onset of the front channel at  $V_{\text{thf}}$  (Fig.2-(b)).

## III. BRIDGE DOPING PROFILE EXTRACTION METHODOLOGY WITH TCAD

To extract the bridge doping profile, we revisit the method described in [6-11]. The depletion depth depends on the gate voltage: a small signal variation on the metal modifies the depletion depth and the charge density at bottom of the film.

### A. Extraction of the ‘doping profile of the bridge’

Having  $C_{\text{gg}}$ , and considering the depletion regime in the body and all dopants ionized, we need to compute the so-called ‘doping function’  $N_{\text{net}}$  (1) defined as an apparent density of charge in the silicon film [6]:

$$N_{\text{net}} = 2 \left( qA^2 \epsilon_{\text{Si}} \frac{dC_{\text{gg}}^{-2}}{dV_g} \right)^{-1} \quad (1)$$

with  $q$  the elementary charge,  $\epsilon_{\text{Si}}$  the silicon permittivity and  $A$  the gate area. Fig.3-(a) shows  $|N_{\text{net}}|$  versus  $V_g$  derived from the C-V characteristic of the A2RAM (Fig.2-(a)). In the gate bias range between  $V_{\text{thb}}$  and  $V_{\text{thf}}$ , the ‘doping function’ presents a broad peak with the maximum value  $9.10^{17} \text{ cm}^{-3}$  close to the doping value set in TCAD (Fig.1).

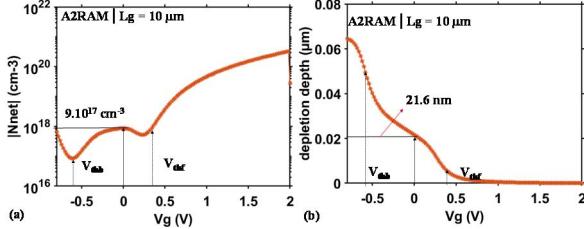


Figure 3. (a) Doping function and (b)-depletion depth in A2RAM by TCAD simulations.

In Fig.4-(a), similar simulations are performed for various bridge doping value  $N_{\text{bridge}}$  ( $3.10^{18}$ ,  $10^{18}$ ,  $3.10^{17}$ , and  $10^{17} \text{ cm}^{-3}$ ) keeping constant the bridge thickness  $T_{\text{bridge}}$  ( $22 \text{ nm}$ ). With higher values of  $N_{\text{bridge}}$  ( $\geq 3.10^{18} \text{ cm}^{-3}$ ), the extracted bridge doping can be accurately evaluated (Fig.4-a) because less and less portion of the bridge is depleted by the field effect. If the  $N_{\text{bridge}}$  is low ( $< 3.10^{17} \text{ cm}^{-3}$ ), the extracted value has no sense because the bridge is fully depleted. This observation is confirmed in Fig.6-a where we compare the C-V of A2RAM as described in Fig.1 but with  $N_{\text{bridge}} = 10^{17} \text{ cm}^{-3}$ , and  $3.10^{17} \text{ cm}^{-3}$ , with the C-V of a SOI device transistor with the same silicon thickness. For a bridge doping higher than  $3.10^{17} \text{ cm}^{-3}$ , the change in slope starts to become significant, but as the device is still fully depleted (including the bridge), that is why the extraction remains “inaccurate”. Indeed, for  $N_{\text{bridge}} < 3.10^{17} \text{ cm}^{-3}$  the shape of the C-V curve shows the same slope even if we have an  $N_{\text{bridge}}$ .

On the other hand, Fig.5-(a) shows the impact of the bridge thickness  $T_{\text{bridge}}$  ( $28$ ,  $22$ ,  $14$ ,  $10$ , and  $8 \text{ nm}$ ) while keeping constant the bridge doping ( $N_{\text{bridge}} = 10^{18} \text{ cm}^{-3}$ ). As for the bridge doping, good resolution of the  $N_{\text{bridge}}$  extracted is guaranteed for thicker bridge ( $T_{\text{bridge}} \geq 22 \text{ nm}$ ). But, the extracted  $N_{\text{bridge}}$  is less accurate for films thinner than  $14 \text{ nm}$  because the bridge is more and more depleted. For ultrathin  $T_{\text{bridge}}$  ( $< 8 \text{ nm}$ ), the bridge is totally depleted. In Fig.6-b, we compare the C-V curves of an ARAM as described in Fig.1 but with  $T_{\text{bridge}} = 8 \text{ nm}$  and a SOI device transistor with same silicon thickness. They are similar with a smooth slope in the case of the A2RAM.

### B. Extraction of the ‘Body’ thickness

We aim to extract the bridge doping  $N_{\text{bridge}}$  and the body thickness  $T_{\text{body}}$ . At a gate voltage between  $V_{\text{thb}}$  and  $V_{\text{thf}}$ , the bridge is still formed, and the body is depleted: this means that the gate capacitance  $C_{\text{gg}}$  corresponds to  $C_{\text{ox}}$  and  $C_{\text{si}}$  in series, with  $C_{\text{ox}}$  and  $C_{\text{si}}$  the gate oxide and the depletion layer capacitance respectively. In this particular case, the depletion layer corresponds to the p-doped body layer, so we have:

$$\text{depletion depth} = T_{\text{body}} = \epsilon_{\text{Si}} (C_{\text{gg}}^{-1} - C_{\text{ox}}^{-1}) \quad (2)$$

As we precisely know the value of the total silicon thickness  $T_{\text{Si}}$ , we can easily deduce  $T_{\text{bridge}}$  ( $T_{\text{bridge}} = T_{\text{Si}} - T_{\text{body}}$ ).

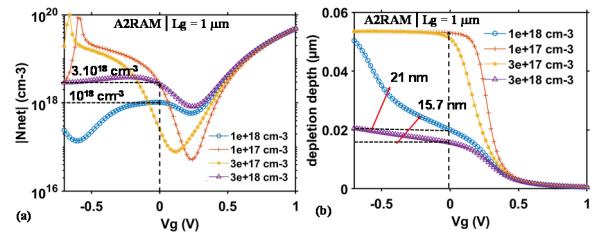


Figure 4. (a) Doping function and (b) depletion depth for different  $N_{\text{bridge}}$  ( $3.10^{18}$ ,  $10^{18}$ ,  $3.10^{17}$ , and  $10^{17} \text{ cm}^{-3}$ ) obtained by A2RAM TCAD simulations.

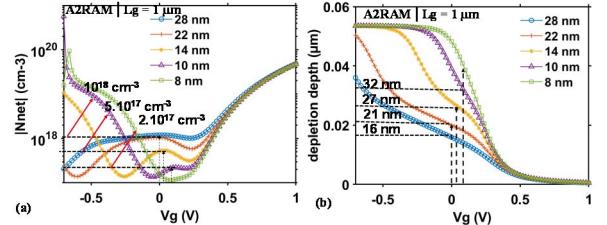


Figure 5. (a) Doping function and (b) depletion depth for different  $T_{\text{bridge}}$  ( $28$ ,  $22$ ,  $14$ ,  $10$  and  $8 \text{ nm}$ ) obtained by A2RAM TCAD simulations.

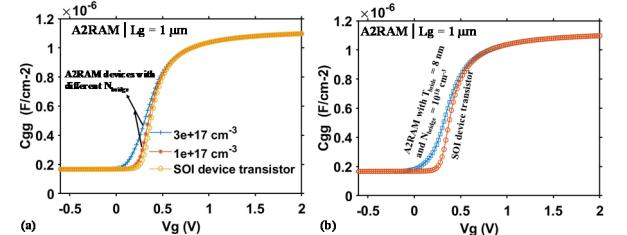


Figure 6. Comparison of the C-V of a SOI device transistor with (a) A2RAM as defined in Fig.1 but with  $N_{\text{bridge}} = 3.10^{17} \text{ cm}^{-3}$  and  $N_{\text{bridge}} = 10^{17} \text{ cm}^{-3}$ , (b) A2RAM as defined in Fig.1 but with  $T_{\text{bridge}} = 8 \text{ nm}$ , obtained by TCAD simulations.

Fig.3-(b) shows the depletion depth versus gate bias  $V_g$ . The depletion depth corresponding to the electrical thickness of the ‘body’ must be determined at same gate voltage as the one used for the bridge doping extraction (in this case  $V_g=0$ ). The value extracted,  $T_{\text{body}} = 21.6 \text{ nm}$ , is  $8 \text{ nm}$  higher than the  $14 \text{ nm}$  of  $T_{\text{body}}$  defined in TCAD (Fig.1). This difference is related to the relatively low value of the bridge doping. To confirm this hypothesis, we have extracted  $T_{\text{body}}$  for different  $N_{\text{bridge}}$ , and the results are shown in Fig.4-(b). As in  $N_{\text{bridge}}$  extraction,  $T_{\text{body}}$  extraction is more accurate for higher doping: for  $N_{\text{bridge}} = 3.10^{18} \text{ cm}^{-3}$ , we obtain  $T_{\text{body}} = 15.7 \text{ nm}$ , just  $2 \text{ nm}$  thicker than the expected  $14 \text{ nm}$ . If  $N_{\text{bridge}}$  is too low ( $< 3.10^{17} \text{ cm}^{-3}$ ), the silicon film is fully depleted (Fig.6-a), including the bridge. This implies that  $C_{\text{gg}}$  capacitance depends on BOX capacitance and equation (2) cannot be used (this explains why  $T_{\text{body}} > T_{\text{Si}}$  for low  $N_{\text{bridge}}$ ).

In Fig.5-(b), the results achieved for different bridge thickness  $T_{\text{bridge}}$  values (28, 22, 14, 10, and 8 nm) at the same bridge doping  $N_{\text{bridge}}$  ( $10^{18} \text{ cm}^{-3}$ ) are shown. For  $T_{\text{bridge}} > 8 \text{ nm}$ , the  $T_{\text{body}}$  extracted are 16, 21, 27, and 32 nm instead of 8, 14, 22, and 26 nm thus inaccurate because the initial bridge doping is relative low as we have noticed in Fig.3 and Fig.4. For low  $T_{\text{bridge}}$  ( $< 8 \text{ nm}$ ) like for low values of  $N_{\text{bridge}}$  the value of  $T_{\text{body}}$  extracted is meaningless because the bridge is depleted (Fig.6-(b)).

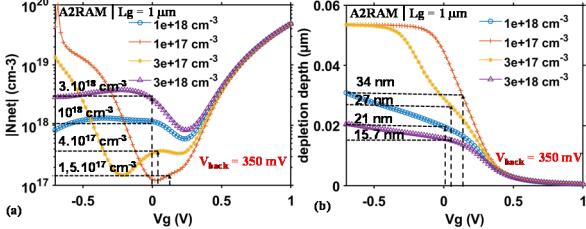


Figure 7. (a) Doping function and (b) depletion depth with back-gate bias ( $V_{\text{back}} = 350 \text{ mV}$ ) for different  $N_{\text{bridge}}$  ( $3.10^{18}, 10^{18}, 3.10^{17}, \text{ and } 10^{17} \text{ cm}^{-3}$ ) obtained by simulations.

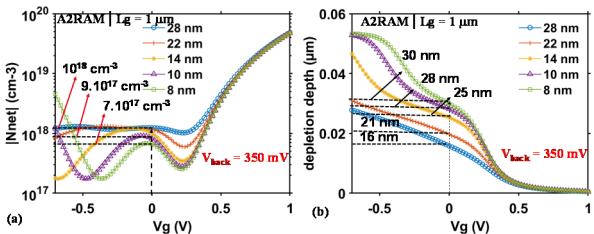


Figure 8. (a) Doping function and (b) depletion depth with the back gate ( $V_{\text{back}}$ ) at 350 mV for different  $T_{\text{bridge}}$  (28, 22, 14, 10 and 8 nm) obtained by A2RAM TCAD simulations.

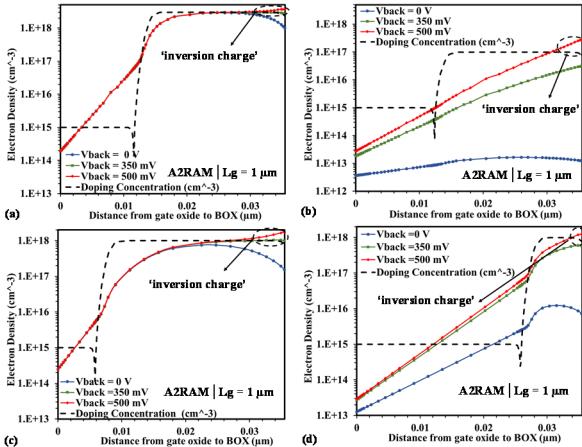


Figure 9. comparison of the doping concentration with the electron density extracted at  $V_g = 0 \text{ V}$  for different  $V_{\text{back}}$  for an: (a) A2RAM as defined in Fig.1 with  $N_{\text{bridge}} = 3.10^{18} \text{ cm}^{-3}$ , (b) A2RAM as defined in Fig.1 with  $N_{\text{bridge}} = 10^{17} \text{ cm}^{-3}$ , (c) A2RAM as defined in Fig.1 with  $T_{\text{bridge}} = 28 \text{ nm}$ , and (d) A2RAM as defined in Fig.1 with  $T_{\text{bridge}} = 8 \text{ nm}$ ; obtained TCAD simulations.

### C. Comments about the resolution of the technique

The observations derived from Fig.4 could infer that the minimum value of the bridge doping that can be extracted is  $3.10^{17} \text{ cm}^{-3}$ . However, Fig.7 shows if the back gate is properly biased ( $V_{\text{back}}$ ), it is possible to extract a doping value even for

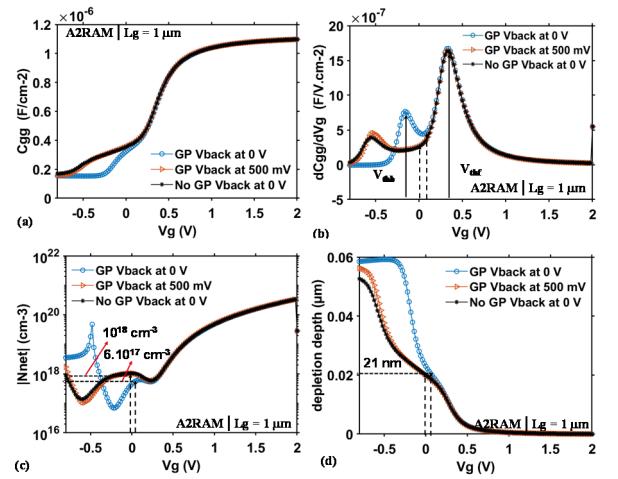


Figure 10. (a) C-V characteristic, (b) first derivative of the C-V, (c) doping function, and (d) depletion depth of the A2RAM with mid-gap back metal and with a p-type GP (TCAD simulations).

low doping ( $< 3.10^{17} \text{ cm}^{-3}$ ). Reducing the bridge doping value while keeping the same mid gap metal at the back interface changes the flat band condition, thus we need to apply a back bias  $V_{\text{back}}$ . Even in flat band condition at the back interface, if the value of  $N_{\text{bridge}}$  is low ( $< 3.10^{17} \text{ cm}^{-3}$ ), the value of  $T_{\text{body}}$  extracted is less accurate. In fact, the depletion of the bridge due to the pn junction (body-bridge) is no longer negligible. Considering the standard expression of the depletion depth at thermal equilibrium [12], we can estimate the depletion depth in the n-type ( $3.10^{17} \text{ cm}^{-3}$ ) bridge equals 3.3 nm. Since the ‘bridge thickness’ is 22 nm, neglecting the depletion of the bridge due to the body junction is not realistic.

In the same way, from Fig.5 one can deduce that below  $T_{\text{body}} = 8 \text{ nm}$  it is not possible to extract a bridge doping  $N_{\text{bridge}}$  and a body thickness  $T_{\text{body}}$ . But in Fig.8-(a) and 8-(b) biasing the back interface enhances the resolution of the extraction. As observed in Fig.7 the shift of the flat band condition can be managed by biasing the back gate. However, there is a limit of the bias which can be applied on the back interface  $V_{\text{back}}$ . In Fig.9, we compare the electron density extracted at gate voltage  $V_g = 0 \text{ V}$  with the original ‘doping concentration’ for different structures at variable  $V_{\text{back}}$ . For  $V_{\text{back}} > 500 \text{ mV}$ , the electron density at the back interface is higher than the concentration in the volume of the bridge. Its variation is just few nanometer above the BOX, due to “weak inversion”. That is why for this work, we have limited  $V_{\text{back}}$  at 350 mV.

Previous simulations consider a metal electrode directly below the BOX with a mid-gap work-function. However, in real A2RAM device [3] a silicon ground plane GP acts as the back gate. To determine if the presence of GP could have an impact on our extraction methodology, we performed simulation of A2RAM including a p-type GP (doping  $10^{18} \text{ cm}^{-3}$ ). Because of the back gate work-function shift, C-V curves are not aligned (Fig.10-a): we need to apply 500 mV on the GP to superpose the C-V plots for metal and silicon back gate (Fig.10-(a,b)). In this condition, the bridge doping extracted is the same as the one without the GP (Fig.10-c). Note also that  $T_{\text{body}}$  extraction is not impacted by the GP (Fig.10-d).

#### IV. EXPERIMENTAL RESULTS AND DISCUSSION

We extract the doping profile of the bridge on the samples fabricated at LETI with process flow described in [3]. The experimental C-V characteristics with two  $V_{back}$  shown in Fig.11-(a) are comparable to C-V from TCAD simulations.

The shift of the  $V_{thb}$  that can be evidenced on Fig.11-(b) (at  $V_{back} = 0$  V) like on Fig.10-(b) is mainly due to the presence of the GP. In consequence, the bridge doping value of  $4 \cdot 10^{17} \text{ cm}^{-3}$  read on Fig.11-(c) at  $V_{back} = 0$  V is lower than the real value but the accuracy can be improved by biasing the back gate at  $V_{back} = 500$  mV as evidenced by simulation. In this condition, the extracted doping value equals nearly  $10^{18} \text{ cm}^{-3}$ . The  $T_{body}$  extracted (Fig.11-d) at  $V_{back} = 0$  V (27 nm) or at  $V_{back} = 500$  mV (24 nm) is overestimated because the value of  $N_{bridge}$  is low (as we have noticed and concluded in Fig.3-b, Fig.4-b).

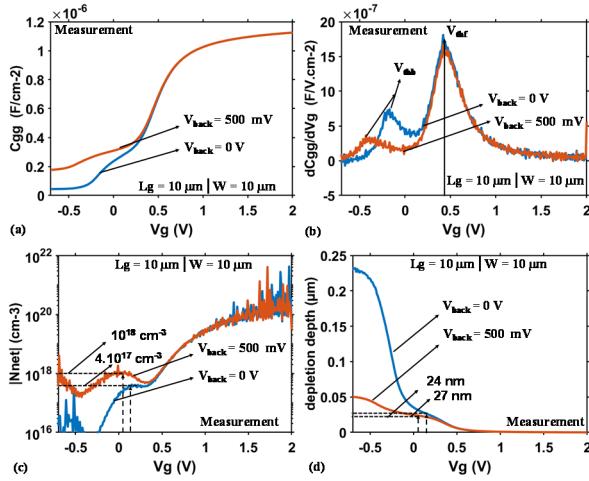


Figure 11. (a) C-V characteristic, (b) first derivative of the C-V, (c) doping function, and (d) depletion depth of the A2RAM sample [3] with mid-gap back metal and with a p-type GP.

#### V. CONCLUSION

In this paper, we have developed an electrical characterization method to extract the doping profile in thin SOI films with an application to the A2RAM. We have noticed that for low values of  $N_{bridge}$  and  $T_{bridge}$ , the accuracy can be enhanced by biasing the back gate. The extraction technique has been then implemented on the samples fabricated in LETI [3] and the results are in agreement with the ones shown in simulation.

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#### REFERENCES

- [1] S. Okhonin, P. Fazan, and M.-E. Jones, "Zero Capacitor Embedded Memory Technology for System on Chip," 2005 IEEE International Workshop on Memory Technology, Design, and Testing (MTDT'05).
- [2] N. Rodriguez, S. Cristoloveanu, and F. Gámiz, "New concepts for 1T-DRAMs: covercoming the scaling limits," 978-1-61284-172-4/11/\$26.00 © 2011 IEEE.
- [3] N. Rodriguez, C. Navarro, F. Gámiz, F. Andrieu, O. Faynot, and S. Cristoloveanu, "Experimental demonstration of capacitorless A2RAM cells on silicon-on-insulator," IEEE Electron Device Letters, Vol. 33, No. 12, December 2012.
- [4] F. Tcheme Wakam, J. Lacord, M. Bawedin, S. Martinie, S. Cristoloveanu, and J.-Ch. Barbe, "Optimization guidelines of A2RAM cell performance through TCAD simulations," in SISPAD2017.
- [5] TCAD Sentaurus software – Synopsys vM-2016.12-SP1.
- [6] D. K. Schroeder, "Semiconductor material and device characterization," Third Edition, pp. 61-125, John Wiley & Sons, Hoboken, New Jersey, 2006.
- [7] G. Ghibaudo, S. Bruykre, T. Devouire, B. DeSalvo, and E. Vincent, "Improved method for the oxide thickness extraction in MOS structures with ultra-thin gate dielectrics," Proc. IEEE Int. Cod. on Microelectronic Test Structures, Vol i2, March 1999.
- [8] A. Sareen, Y. Wang, U. Sodervall, P. Lundgren, and S. Bengtsson, "Effect of Si cap layer on parasitic channel operation in Si/SiGe metal–oxide–semiconductor structures," J. Appl. Phys., Vol. 93, No. 6, 15 March 2003.
- [9] S. Chattopadhyay, K. S. K. Kwa, S. H. Olsen, L. S. Driscoll, and A. G. O'Neill, "C–V characterization of strained Si/SiGe multipleheterojunction capacitors as a tool for heterojunction MOSFET channel design," Semicond. Sci. Technol. 18 (2003) 738–744.
- [10] J-H Lee, S. Cristoloveanu, and A. Chovet, "Non-homogeneous electrical transport through silicon-on-saphire thin films: evidence of the internal stress influence," Solid-State Electronics Vol. 2S, No. 9, pp. 947-953, 1982.
- [11] S. Cristoloveanu, J-H Lee, and J. Pumfrey, "Profiling of inhomogeneous carrier transport properties with the influence of temperature in silicon-on-insulator films formed by oxygen implantation," J. Appl. Phys. 60, 3199 (1986).
- [12] H. Mathieu, "Physique des semiconducteurs et des composants électroniques," Fifth Edition, pp. 109-177, Dunod, Paris, 2001.