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Silicon photonics has allowed cost reduction and performance improvement for optical interconnects for the past few years, and short-reach wavelength-division-multiplexed (WDM) links have recently emerged thanks to the introduction of microring modulators and filters [1-5]. Nevertheless, the promise of optical networks-on-chip foreseen in [1] has to face the integration challenges of scalable low-footprint elementary drivers and robust operation under heavy thermal stress due to self-heating of the cores with varying loads. This work presents a 3D-stacked CMOS-on-Si-photonic transceiver chip, which includes base building-blocks targeting die-to-die WDM optical communication for multicore processors: 10Gbps 2.5V_{pp} OOK modulator driver, associated receiver, and digitally-supervised analog wavelength stabilization using microring heaters and remapping for 0-90°C operating range, for a total footprint of 0.01mm^2 per microring.

Fig. 1 presents five different experiments integrated in the chip to validate our approach, starting from a single modulator to a complete 4-wavelength WDM link in the 1310nm band. As the microrings have a sharp temperature-dependent resonance with Q-factors up to 30000, they can be mapped to different wavelengths on the same waveguide, but require fine-tuning of the microrings [2-5] to the laser wavelength using temperature tuning within 0.1°C accuracy by Joule effect in a resistive heater inside the ring. Each wavelength is modulated on the Tx side using carrier-depletion PN-rings and filtered using thermally-tuned passive rings to a germanium photodiode whose photocurrent is demodulated on the Rx side. Vertical-fiber grating couplers inject one or more laser sources into the Si-photonic chip and collect the residual or modulated optical output for monitoring. Fig. 2 presents such an output showing eye diagrams of the optical signal after 2.5Vpp OOK Tx modulation up to 10Gbps.

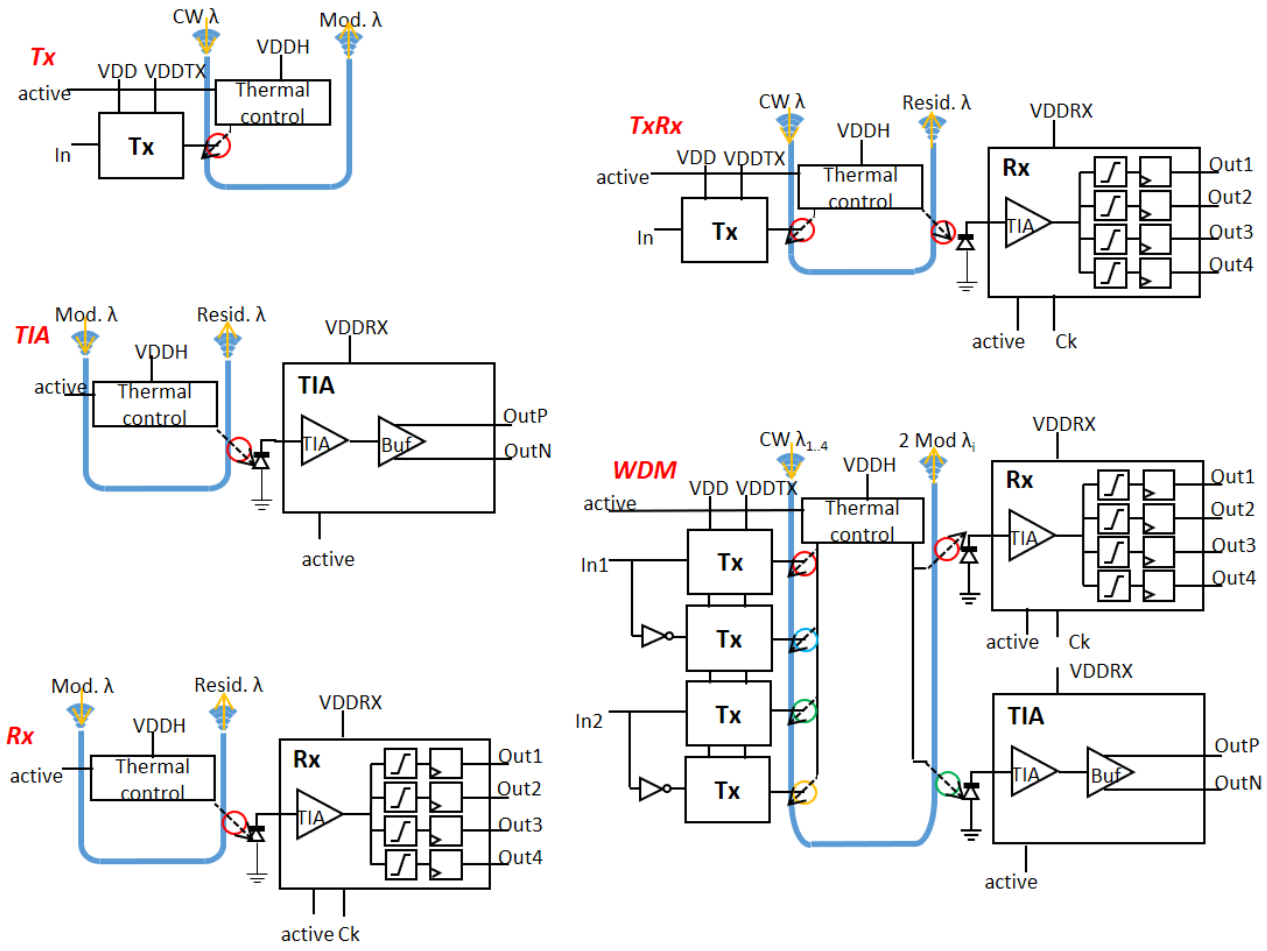

Figure 1: CMOS+Si-photonic chip architecture showing the five implemented sub-experiments

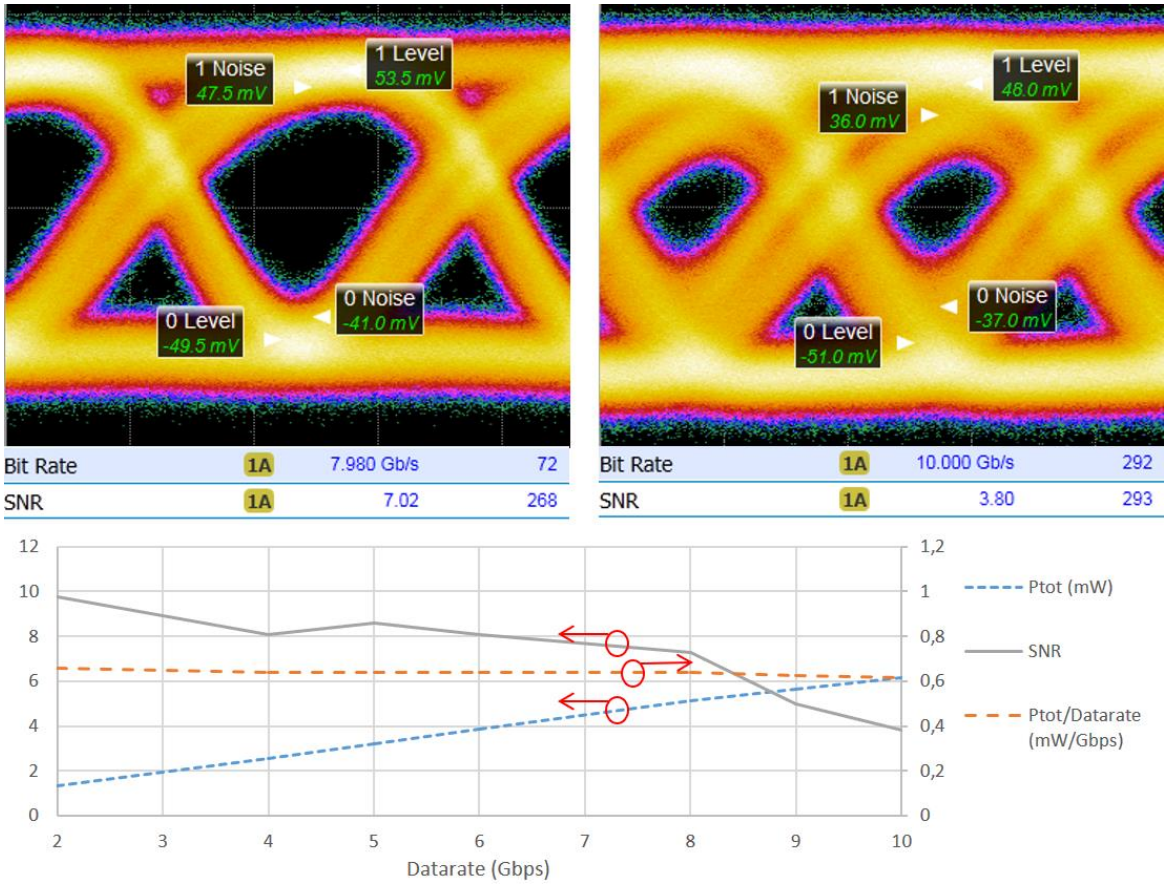

Figure 2: Tx electro-optical modulation eye diagrams and signal to noise ratio at 8Gbps and 10Gbps, for a power consumption of 640 fJ/bit

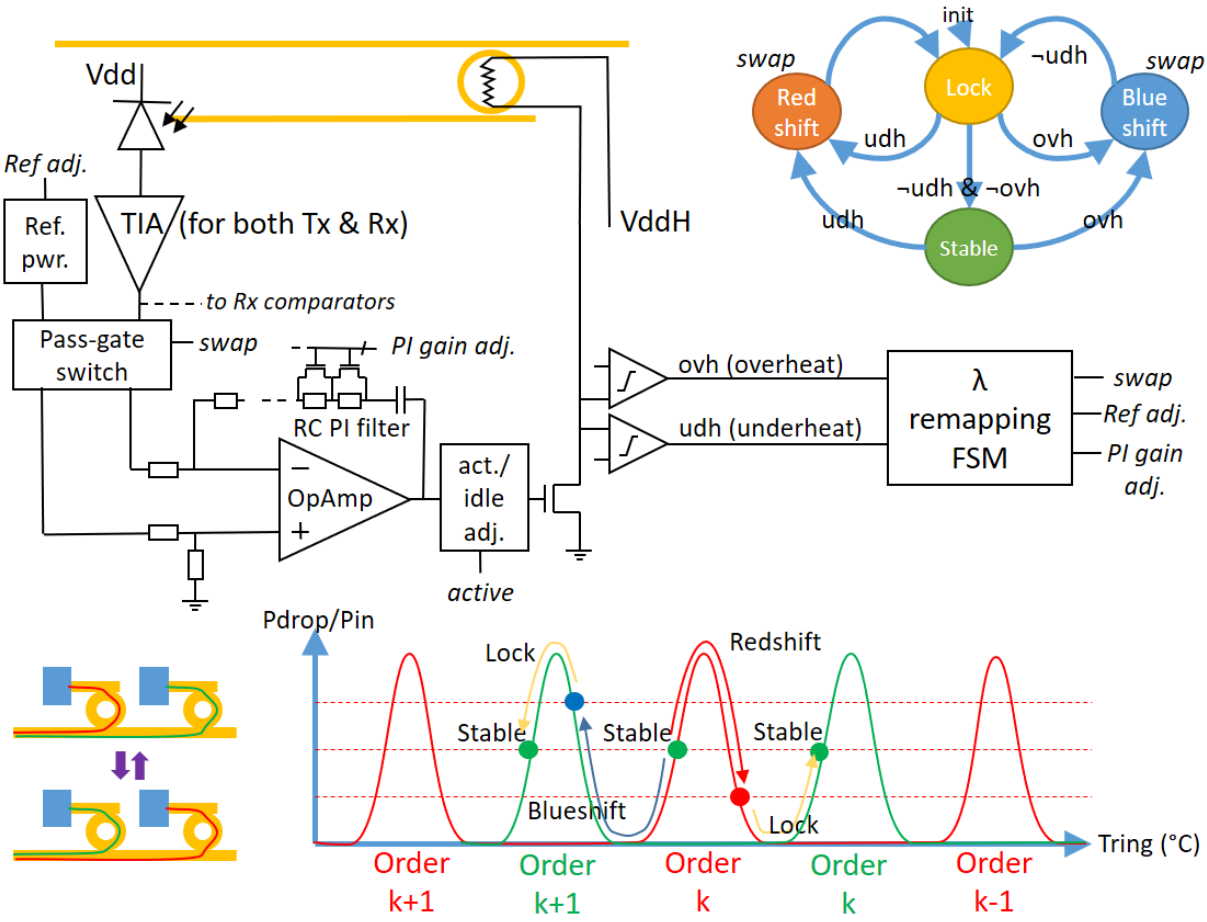

Figure 3: Microring thermal control micro-architecture, with closed-loop analog PI feedback and digital supervision fixing reference set point and loop feedback sign for controlled wavelength remapping

The major innovation in this paper is the new thermal tuning microarchitecture presented in Fig. 3. It uses a digitally-supervised analog feedback loop monitoring the resonance from the drop port of a microring to apply proportional-integral (PI) robust control on the voltage of the resistive heater via a power NMOS transistor. Analog control provides smooth sub-pm tuning to a reference optical power level with no DC offset nor quantization noise. An operational amplifier with configurable RC feedback fixes the control loop gain: proportional and integral parts are set respectively by a controlled segmented 180kΩ polysilicon resistor and a 5pF on-chip capacitor, which take half the area of the 40x40µm^2 tuning controller. A small digital finite-state machine controlling the feedback loop handles initialization and remapping. Normal operation uses negative feedback, where the NMOS gate voltage increases when the optical power decreases, resulting in more heat injected into the ring and a redshift of the resonant wavelength. This stabilizes the wavelength on the sharper edge of the resonant peak induced by non-linear ring dynamics [5], where the modulation efficiency will be maximum as long as the optical power is below the ring bistability point. However, when threshold comparators detect that the ring is either overheated (thermal budget will not allow keeping up with the environmental temperature drop) or under heated (as the ring cannot be cooled-down to hide the temperature increase), the feedback loop sign is inverted using a pass-gate switch to swap the optical power reference and the TIA output. This leads to a controlled stabilization on the other edge of the resonant peak, after what the loop sign is restored to map the ring on the sharp edge of the next wavelength. A slight reference adjustment enforces the shift direction: positive for blueshift, negative for redshift. A loop gain adjustment via the segmented resistor is needed because of the non-linear gain of the ring along the edge. Finally, the control is also adjusted depending on the transmission of data on the wavelength.

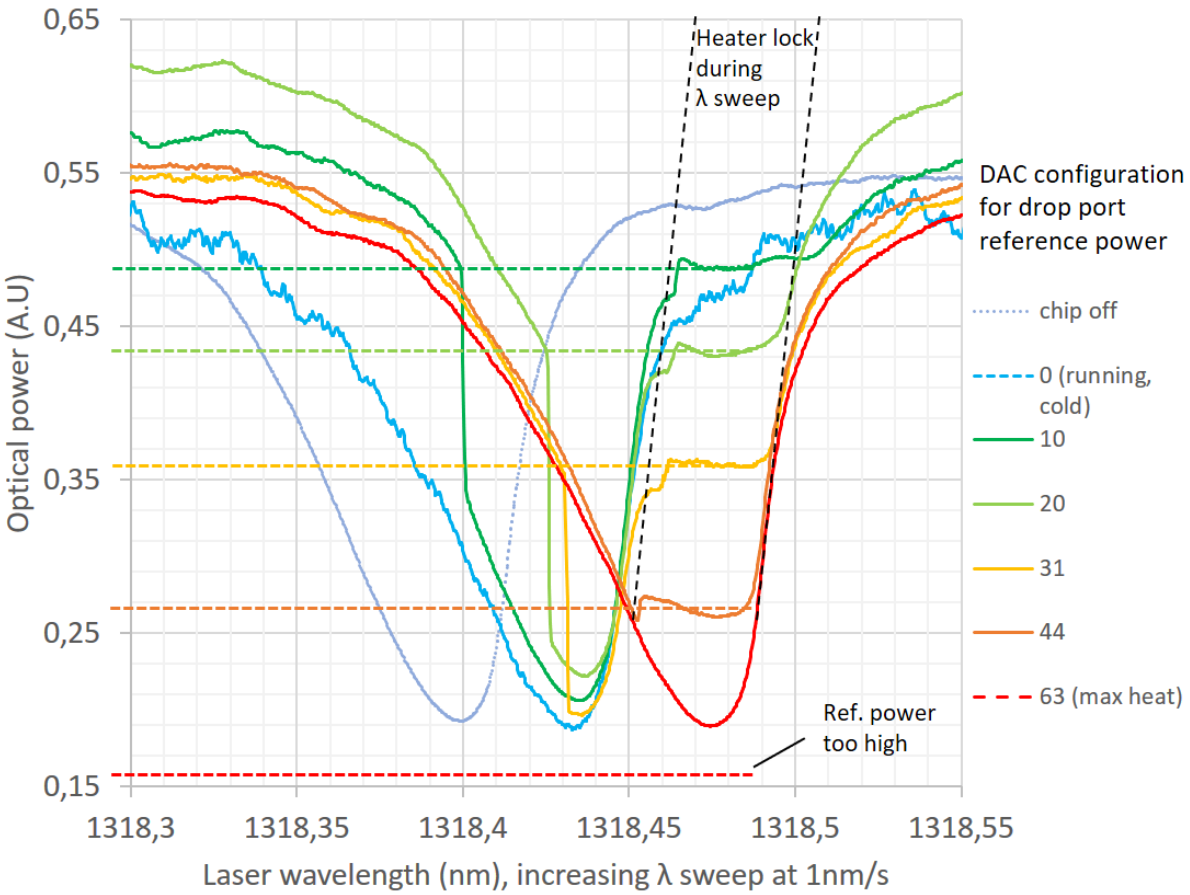

Figure 4: Thru-port transmission spectrum of a microring with different thermal tuning configurations, showing the heater locked (on Drop port) to a reference level during wavelength sweep

Optical transfer function measurements with a laser wavelength sweep are shown on Fig. 4 for a ring controlled at different reference optical powers. The first and last curves show the ring transmission spectrum for a completely cool, resp. hot, microring, with the expected distorted peak. The second dashed curve shows the impact of CMOS heat dissipation on an uncontrolled ring, resulting in a resonance shift of 30pm. The other curves show the ring first heated to the maximum as the optical drop power is below the reference, then suddenly cooled down to the minimum as the peak is crossed to stabilize as expected on its sharper edge, with increasing thermal budget until the maximum is reached. These curves show a 0.5pm flat plateau for about 40pm sweep, showing the tuning accuracy. Tuning range, nevertheless, is not as large as expected because no substrate removal was performed on the microrings [5], letting heat flow off the ring. Fig. 5 presents the dynamic behavior of the thermal tuning. Lock-time is measured after activating the controller, and shows a smooth convergence to a reference level corresponding to -2dB on the through port of a Tx ring, where the extinction ratio will be maximal. Time-domain response to a periodic $30pm_{pp}$ environmental fluctuation of the wavelength shows perfect stabilization of the ring up to 900Hz.

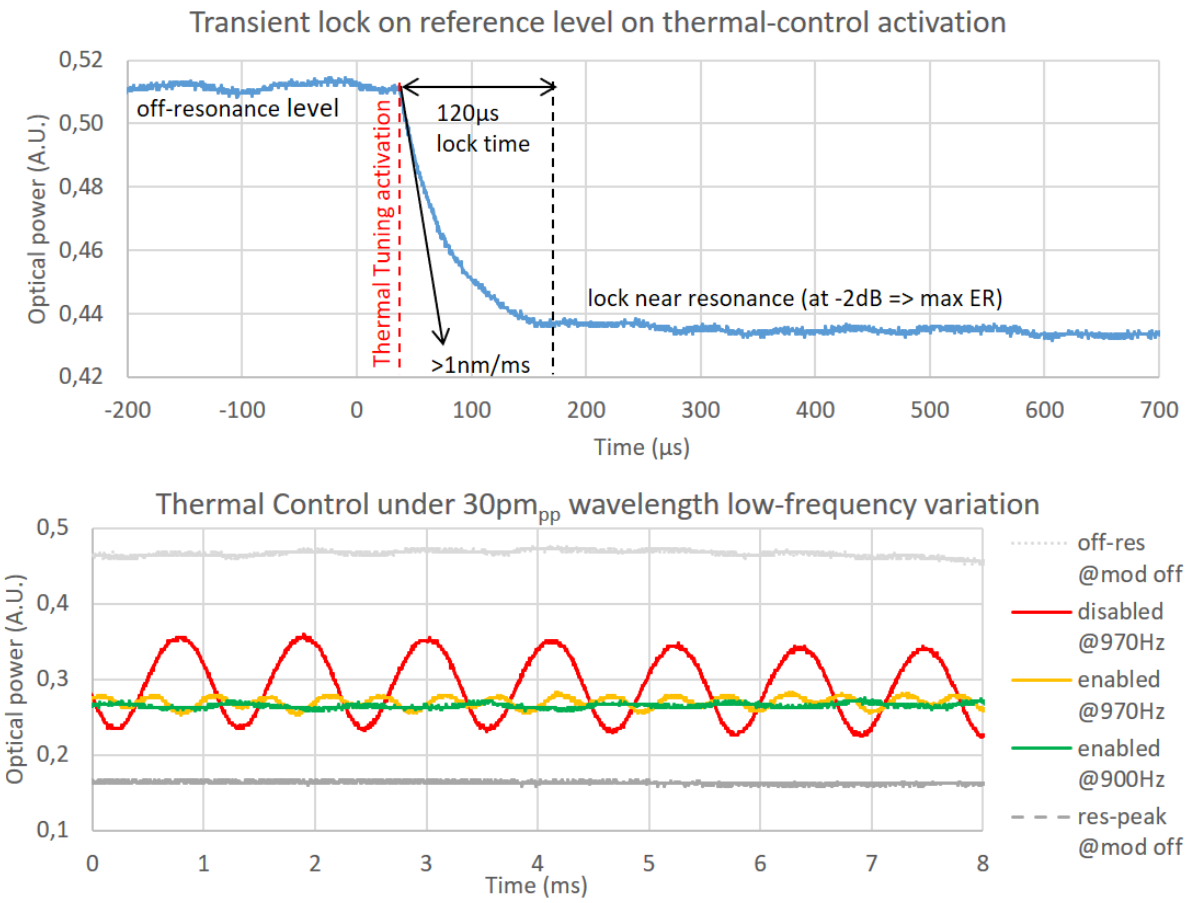

Figure 5: Transient thermal control behavior showing heater lock on target power level after activation and steady state tracking under environmental variation, here laser wavelength

Fig. 6 presents the transceiver performance summary and a comparison table. Authors of [2] follow the same 3D face-to-face integration approach for their WDM transceiver, but still rely on manual external thermal tuning of the microring resonant wavelengths. In [3-4], the electrical and photonic ICs are die-to-die wire-bonded, focusing on 100Gbps Ethernet transceiver modules rather than die-to-die optical communication. Authors of [5] present a complete monolithic CMOS-Si-photonic platform based on standard 40nm process, well suited to on-chip/die-to-die communication, although they do not describe WDM demultiplexing with ring filters. In [3-5], thermal tuning is performed using digital closed-loop control with ΣΔ DAC or SAR ADC, at 100MHz for [3-4], and 76kHz for [5], leading either to high activity or long latency, with a minimum quantization noise of 5pm. The proposed digitally-supervised analog control loop allows for a 50x faster lock-time of 120µs and a demonstrated stability under 900Hz environmental fluctuation, for only 150µW tuning controller power. Digital supervision at 100kHz allows full closed-loop remapping from a wavelength to another in case of large temperature changes in less than 1ms, where previous designs would require to open the loop and scan for a new wavelength. This new remapping capability makes it possible to consider real-time operation with low interruption time under a 0-90°C temperature range commonly found in server chips with varying loads.

	[2] Rakowski ISSCC2015	[3,4] Li, Yu ISSCC2015	[5] Sun JSSC2016	This work
Integration scheme	3D face-to-face	2D proximity wirebonding	Monolithic	3D face-to-face
Technology	130nm SOI SiPh 40nm CMOS	130nm SOI SiPh 65nm CMOS	45nm CMOS SOI	100nm SOI SiPh 65nm CMOS
Datarate	20 Gbps	24 Gbps	10 Gbps	10 Gbps
Ring Q factor	~5500	~5000 Tx, ~18000 Rx	~11600	~30000
Wavelength	1550nm	1550nm	1180nm	1310nm
WDM channels	4	5	11	4
Thermal tuning	Open-loop	Digital closed-loop avg/peak det.	Digital closed-loop bit-statist. (Tx only)	**Analog closed-loop w. digital reconfig.**
Wavelength remapping	No / External	No / External	No / External	**Integrated <1ms remap time***
Heater efficiency	0.16nm/mW	0.16nm/mW	1.25nm/mW	0.04nm/mW
Tuning ctrl. power	N.A. – External	170µW	720µW	**150µW**
Tuning precision	N.A. – External	Not reported	5pm	**0.5pm**
Tuning lock-time	N.A. – External	700ms	6.7ms	**120µs**
Tuning bandwidth	N.A. – External	~1Hz (from tr. meas.)	~1Hz (from tr. meas.)	**900Hz**
Tuning area / ring	0.04mm^2 (pad area)	0.03mm^2	0.0024mm^2	**0.0016mm^2**
Tot. driver area / λ	0.14mm^2 (Tx or Rx)	0.1 / 0.06 mm^2(Tx / Rx)	0.0205mm^2 (Tx)	**0.0096mm^2 (Tx or Rx)**
Bandwidth density	142 Gbps/mm^2	300 Gbps/mm^2	391 Gbps/mm^2	**1 Tbps/mm^2**

* Remapping simulated for heater efficiency of 1.25nm/mW (not attained due to lack of selective substrate removal as in [5])

Figure 6: 10Gbps Si-photonic thermally-tuned transceiver performance summary and comparison table

A photograph of the CMOS chip is shown in Fig. 7, with the different sub-blocks highlighted, and the flip-chip integrated 10Gbps transceiver wire-bonded on a PCB with a fiber array positioned on the optical grating couplers. Inductors are part of the 50Ω output buffers and not in the functional drivers. The footprint for a complete per-wavelength Tx or Rx driver is 9600µm^2, identical on the CMOS and Si-photonic die, and determined by the copper-pillar pitch of 40µm for 6 terminals (ring modulation, ring tuning, photodiode on drop port). This results in a bandwidth-density figure of merit of 1Tbps/mm^2 for a wavelength-locked electro-optical die-to-die communication, paving the way for die-to-die optical networks on photonic interposers for future high-performance computation applications.

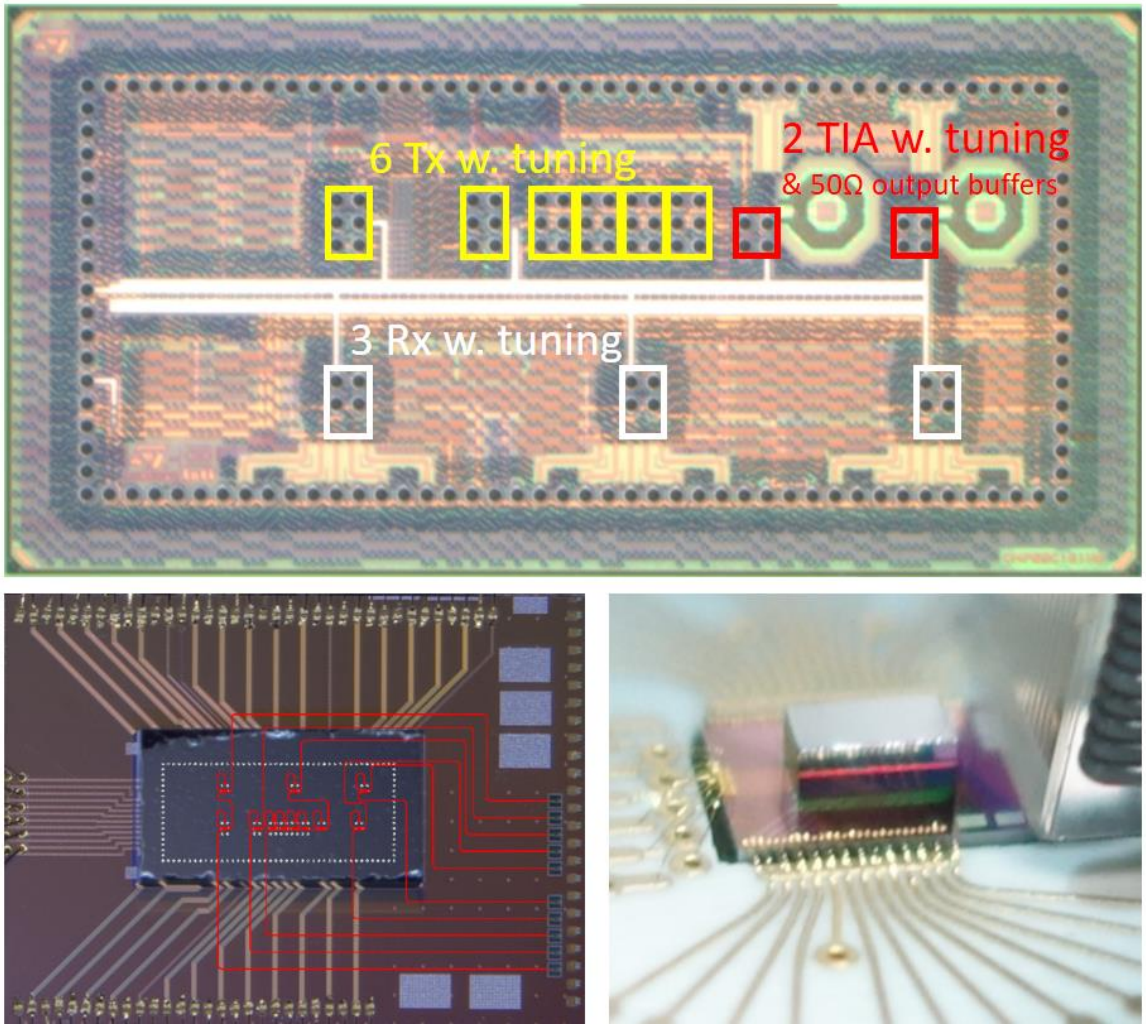

Figure 7: Die photographs of CMOS Transceiver chip with 6 Tx'es and 5 Rx'es including ring tuning, associated flip-chip face-to-face assembly on Si-photonic chip, and board & fiber integration

References:

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[2] Rakowski, *et al.*, "A 4×20Gb/s WDM Ring-Based Hybrid CMOS Silicon Photonics Transceiver," *ISSCC Dig. Tech. Papers*, pp. 408-409, February 2015.

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