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Growth kinetics of Si on fullsheet, patterned and silicon-on-insulator substrates

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Abstract

Using a reduced pressure-chemical vapor deposition cluster tool, we have studied the epitaxial growth of Si using either a silane or a dichlorosilane + hydrochloric acid chemistry on fullsheet, patterned and silicon-on-insulator (SOI) substrates. We have first of all developed a ("HF-last" advanced wet cleaning + low thermal budget (775°C, 2 min) in situ H_2 bake) combination that yields atomically smooth, contamination free Si starting surfaces for both fullsheet and patterned wafers. We have then modeled the low temperature Si growth rate (silane or dichlorosilane + hydrochloric acid chemistry) on fullsheet wafers. A similar growth rate activation energy is found for both chemistries, i.e. $E_{GR} \sim 50\,kcal\,mol^{-1}$. The growth rate dependency on the Si precursor flow is vastly different, however. Fitting this dependency with a simple power law, a value of 0.36 is indeed associated to dichlorosilane, versus 0.92 for silane. The HCl etching rate is characterized by an activation energy $E_{ER} \sim 34\,kcal\,mol^{-1}$, with a 0.52 power law dependency on the HCl flow. On patterned wafers, we have demonstrated that a deposited Si thickness limit (20 nm) exists at 775°C for high $F(HCl)/F(SiH_2Cl_2)$ mass flow ratios. This limit disappears when (i) $F(HCl)/F(SiH_2Cl_2)$ is reduced (ii) the growth temperature is increased to 800°C. Finally, we have highlighted the specifics of the growth on SOI wafers. A significant growth rate reduction (compared to bulk Si) has been evidenced on ultra-thin Si over-layer SOI wafers. It gets less and less pronounced as the buried oxide layer gets thinner and/or the Si over-layer thickness increases.

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1. Introduction

In the last few years, there has been significant interest in SiGe epitaxial growth on silicon substrates, because Si/SiGe heterostructures allow band gap engineering to be used in conjunction with silicon technology [1] in field effect transistors [2,3], photodetectors [4], etc.

We propose in this paper a study of the growth kinetics of Si in reduced pressure-chemical vapor deposition (RP-CVD) on fullsheet, patterned and

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silicon-on-insulator (SOI) substrates. Two precursor chemistries were used: either silane [5] or dichlorosilane + hydrochloric acid [6]. It is possible using the latest chemistry (i.e. the chlorinated one) to selectively grow high quality Si [7–10] layers inside the Si windows of SiO_2 or Si_3N_4-masked Si wafers, making it useful for the formation of Si raised sources and drains [11,12]. The knowledge of the specifics of the growth of Si on SOI wafers will be put to good use for the deposition of tensile-strained Si layers on top of nearly fully relaxed SiGe-on-insulator (SGOI) substrates [13–15].

As far as the experimental results are concerned, the article is organized as follows. We will first focus on the surface preparation (ex situ wet cleaning followed by an in situ low temperature H_2 bake) of fullsheet and patterned wafers prior to epitaxy. We will then present a semi-empirical modeling of the low temperature Si growth rate on fullsheet wafers for the hydrogenated and the chlorinated chemistries. We will highlight the specifics of the selective epitaxial growth of Si with the dichlorosilane + hydrochloric acid chemistry on patterned wafers. We will notably focus on the role of the growth temperature and of the $F(HCl)/F(SiH_2Cl_2)$ mass flow ratio on the Si thickness that can be deposited inside the Si windows. Finally, we will quantify on SOI wafers the impact of both the buried oxide and Si overlayer thickness on the Si growth kinetics.

2. Experimental details

We have grown the Si layers with an Epi Centura RP-CVD industrial cluster tool (manufactured by Applied Materials). The Si(0 0 1) substrates used are nominal ($\pm 0.25^\circ$) and slightly p-type doped (resistance in the 7–10 Ω cm range). During the growth, the wafer lies horizontally on top of a circular SiC-coated susceptor plate that rotates to improve thickness uniformity. The substrate is heated by two banks of 20 tungsten–halogen lamps (maximum power: 2 kW each) located above and below the susceptor assembly. It is therefore heated by thermal radiation coming from the upper lamps bank, as well as by thermal conduction from the susceptor underneath. Temperature monitoring and control is ensured through the lower pyrometer, i.e. the one which is looking at the backside of the susceptor plate on which the wafer lies. The reading is therefore independent of the nature of the substrate (fullsheet, patterned or SOI). It is only the heat transfer by radiation from the upper lamp-bank that can be affected by changes in wafer surface emissivity during Si deposition [16]. In our study, the growth pressure was *always* 20 Torr. The flow of H_2 carrier gas was set at a *fixed value* of a few tens of standard liters per minute (slms), which was *not* altered throughout all the experiments. Pure dichlorosilane (SiH_2Cl_2 or DCS) and pure silane (SiH_4) were used as the sources of Si.

A Akrion Gama One automated wet bench was used for the ex situ cleaning of our substrates. The secondary ion mass spectrometry (SIMS) measurements were carried out on a Cameca IMS 5f spectrometer. Cs^+ primary ions were used for carbon, oxygen, fluorine and germanium depth profiling, with an impact energy of 2 keV. The atomic masses monitored were those of Cs_2C^+ ($133 \times 2 + 12 = 278$ amu), Cs_2O^+ ($133 \times 2 + 16 = 282$ amu), Cs_2F^+ ($133 \times 2 + 19 = 285$ amu) and Cs_2Si^+ ($133 \times 2 + 28 = 294$ amu) [17]. Cross-sectional transmission electron microscopy imaging was performed on an Akashi EM-002B (fitted with an ultra-high resolution pole piece) that was operated at 200 kV. A Digital Instrument 3100 SPM platform fitted with a camera was used for the tapping-mode atomic force microscopy (AFM) imaging of the surface morphology. Scanning tunneling microscopy (STM) was carried out in ultra-high vacuum using an Omicron apparatus. Finally, spectroscopic ellipsometry (SE) measurements were carried on a SE 1280 Ellipsometer from KLA-Tencor.

The Si thickness deposited was determined in three different ways depending on the nature of the substrate:

- On bulk, fullsheet wafers, the 200 mm wafer was scaled on a micro-balance prior and just after the epitaxy step. The average thickness deposited on a 200 mm wafer is then given by: $t(\text{cm}) = \Delta m/(\pi R^2 \rho)$ (Δm is the weight difference

(g), R ($=10$ cm) is the radius of the wafer and $\rho = 2.328$ g/cm^3 is the Si density).

- On bulk, patterned wafers, the Si thickness deposited was determined through a step height difference measurement in AFM at the boundary between a Si window and the dielectric masking material [18].
- On SOI wafers, the Si thickness deposited is determined through a differential measurement in SE of the Si over-layer thickness before and after the epitaxy step.

3. Surface preparation

It is of the utmost importance when growing layers epitaxially on fullsheet, patterned or SOI wafers to start from a mono-crystalline Si surface free of any particles or contaminants.

We have used a variant, which we have named "EpiClean" [18], of the so-called "Low Consumption Front End of Line" (LC-FEOL) wet cleaning [19] to prepare the surface of our samples. This cleaning, whose last three steps are a 2.5 min dip into a HF:HCl:De-ionised water (DIW) bath (0.2/1/100 at 23°C) followed by a DIW rinse and an Iso-Propylic Alcohol vapor drying [18], generate "HF-last", Si(0 0 1) passivated surfaces [20], i.e. surfaces with dangling bonds being mostly occupied by H or F atoms that are stable for a few tens of minutes in ambient conditions, enabling sample transfer and loading. An H_2-bake, typically between 800°C and 900°C for a few tens of seconds up to a few minutes [11,21–26], will lead to the removal of any C, O or F residual atoms and to the formation of smooth [24,27] (2×1):H reconstructed surfaces that are much more stable in the air [28] (up to 40 h [29]).

Several groups have tried to minimize the thermal budget necessary for the H_2 bake [21,25,26,30]. What has been found on fullsheet wafers is that an optimized wet clean [last step: 1:1000 HF(49%):deionized water] followed by an H_2 bake at 800°C for 2 min is sufficient at 10 Torrs to produce oxygen and carbon-free Si surfaces [26]. We have tried to extend those findings for patterned wafers.

We have therefore cleaned fullsheet and patterned wafers with the above-mentioned "EpiClean" wet cleaning, loaded those samples inside the load-locks of our cluster tool, then purged those load-locks with N_2. The samples have then been transferred over to the RP-CVD chamber, where they have been submitted at 20 Torrs to an 2 min H_2 bake at either 775°C or 750°C, followed by the deposition of 60 nm of Si at 750°C using SiH_2Cl_2. We have profiled in SIMS (see Figs. 1 and 2) the C, O and F atoms in those samples. No peak has been observed for those elements at the Si epilayer/substrate interface at 775°C, this whatever the nature of the substrates (fullsheet or patterned). Meanwhile, 750°C seems to be too small a temperature (at least for 2 min H_2 bakes) to get rid of those impurities, as attested by the peaks in SIMS at the interface between the Si epilayer and the substrate on a fullsheet wafer (see Fig. 1). For the sake of completeness, it should nevertheless be mentioned that no such peaks were observed for this bake temperature of 750°C on the corresponding patterned wafer. The temperature boundary between cleaned and contaminated wafers must therefore be slightly above 750°C.

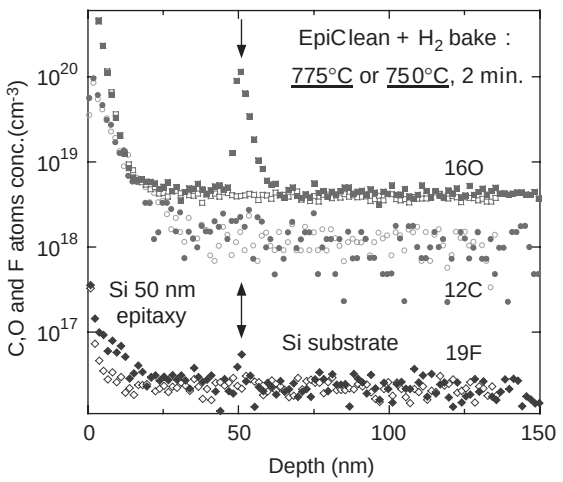

Fig. 1. SIMS depth profile of the O, C and F atoms in the Si epilayers grown on fullsheet wafers after a ex situ "EpiClean" wet cleaning followed by an in situ H_2 bake either at either 775°C (open symbols) or at 750°C (full symbols) for 2 min ($P = 20$ Torrs).

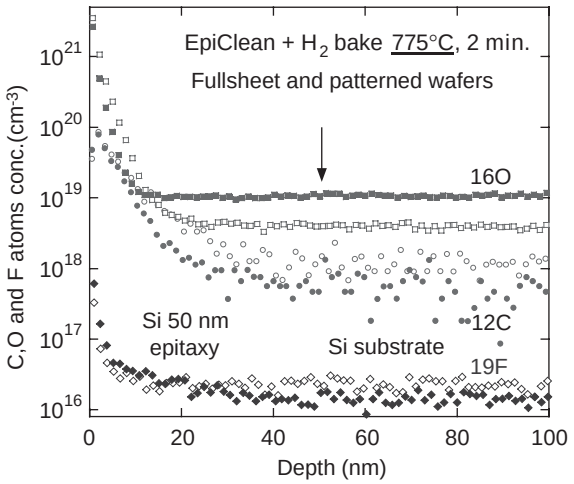

Fig. 2. SIMS depth profile of the O, C and F atoms in the Si epilayers grown on either a fullsheet wafer (open symbols) or a patterned wafer (full symbols) after a {ex situ "EpiClean" wet cleaning + H_2 bake at 775°C, 20 Torrs for 2 min} surface preparation. SIMS profiling was carried out inside a large Si window for the patterned wafer.

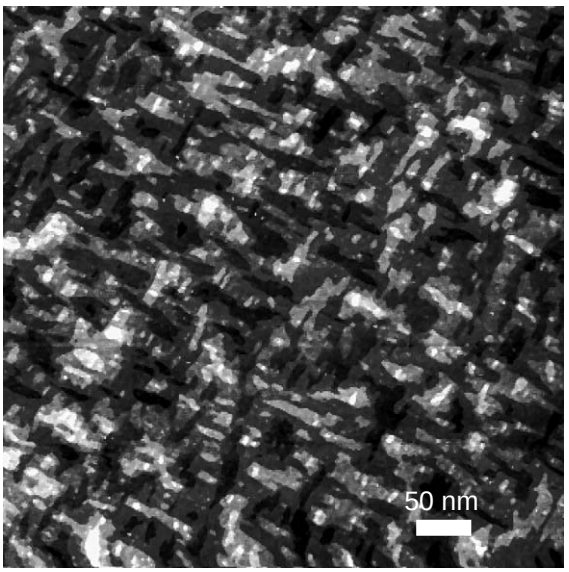

Fig. 3. STM image (500 nm × 500 nm) of the surface of a blanket Si(0 0 1) substrate that has been cleaned ex situ with an "EpiClean" recipe followed by an in situ H_2 bake at 775°C for 2 min. Sample bias voltage: +2.8 V, tunneling current: 80 pA.

This conclusion is supported by the finding of Brabant et al. [30], who have found that neither a 10 min nor a 20 min bake under H_2 at 750°C does enable to completely get rid of the interfacial oxyde. They have indeed obtained in SIMS a small O peak at the interface (maximum: $\sim 10^{19}$ ($\sim 10^{18}$) cm^{-3}, integrated dose: 2.5×10^{12} (2.34×10^{11}) cm^{-2} for a 10 min (20 min) H_2 bake at 750°C). No C peak was obtained in both cases, however.

A STM image of the surface of a fullsheet wafer that has been cleaned ex situ using the "EpiClean" process followed by an in situ H_2 bake at 775°C for 2 min is plotted in Fig. 3. The surface is atomically smooth, with mono-atomic steps either straight (S_A-type) or meandering (S_B-type) [31,32] delimiting either (1 × 2) or (2 × 1)-reconstructed, a few tens of nm wide, terraces. The root mean square roughness of that surface is equal to 0.9 Å.

We can therefore conclude that an "EpiClean" ex situ wet clean followed by an in situ H_2 bake at 775°C, 20 Torrs for 2 min is an efficient, low-thermal budget combination to obtain atomically smooth surfaces free of any residual contamination.

4. Si growth kinetics on fullsheet wafers

4.1. The dichlorosilane+hydrochloric acid chemistry

Simply speaking, the growth of Si using a $SiH_2Cl_2 + HCl$ chemistry is expected to take place according to the following three equations [9,33]:

- SiH_2Cl_2 thermally dissociates in the gas phase into $SiCl_2$ and H_2:

$$SiH_2Cl_2(g) \rightleftharpoons SiCl_2(g) + H_2(g) \quad (1)$$

- Deposition of Si occurs through the reduction of the adsorbed $SiCl_2$ on a free surface site by hydrogen:

$$SiCl_2^* + H_2(g) \rightarrow Si(s) + 2HCl(g) \quad (2)$$

- If enough additional external HCl is added to the system at a given pressure and temperature, silicon etching occurs through:

$$Si^* + 2HCl(g) \rightarrow SiCl_2^* + H_2(g) \quad (3)$$

If the quantity of HCl added to the system is optimized, silicon atoms are removed on a patterned wafer from the dielectric mask before they form stable polysilicon nuclei. The SEG of Si can therefore be visualized as a sum of the growth effect, which is dependent of the abundance of adsorbed $SiCl_2$, and the etching effect, which is dependent upon the partial pressure of HCl.

The low-temperature ($750°C \leqslant T \leqslant 850°C$) Si growth rate modelling we have adopted here is based on the work of Kongetira et al. [33]. They have fitted their Si growth rate dependence on the SiH_2Cl_2 and HCl partial pressures, on the growth temperature and pressure with the following semi-empirical expression:

$$\mathrm{GR}\ (\mu\mathrm{m/min}) = \frac{k_{\mathrm{GR}}(\mathrm{DCS})e^{-E_{\mathrm{GR}}(\mathrm{DCS})/k_B T}(P_{\mathrm{DCS}})^z(P_{H_2})^x}{\Delta} - \frac{k_{\mathrm{ET}}e^{-E_{\mathrm{ET}}/k_B T}(P_{\mathrm{HCl}})^y}{\Delta}$$

where E_{GR} (DCS) and E_{ET} are activation energies for the growth and for the etching of Si, respectively. k_{GR} (DCS) and k_{ET} are rate constants for the growth and for the etching of Si, respectively. Δ is a pressure-related factor. Having been fixed arbitrarily by Kongetira et al. to 1 for a growth pressure of 40 Torrs, it has been found to vary linearly with the growth pressure (in Torrs) in the following manner: $\Delta = 0.06P - 1.4$. P_{DCS}, P_{H_2} and P_{HCl} are the incoming flows' partial pressures (in Torrs). k_B and T are the Boltzmann constant and the absolute growth temperatures, respectively. x has been fixed to 1.0 in Kongetira et al.'s work.

We have consequently made the following assumptions for the modeling of our experimental data: Δ is arbitrarily fixed to 1.0 at 20 Torrs (instead of 40 Torrs), x is equal to 1.0. Let us now focus on the determination of E_{GR}, k_{GR} and z. Without any incoming flow of HCl, the Si growth rate is given by:

$$\mathrm{GR}_{\text{without added HCl}}(\mathrm{nm/min}) = k_{\mathrm{GR}}(\mathrm{DCS})e^{-E_{\mathrm{GR}}(\mathrm{DCS})/k_B T}(P_{\mathrm{DCS}})^z(P_{H_2}).$$

Using an Arrhenius plot of the Si growth rate without HCl as a function of the reverse absolute temperature (see Fig. 4), it is quite easy to determine E_{GR} (DCS). E_{GR} (DCS) has been found

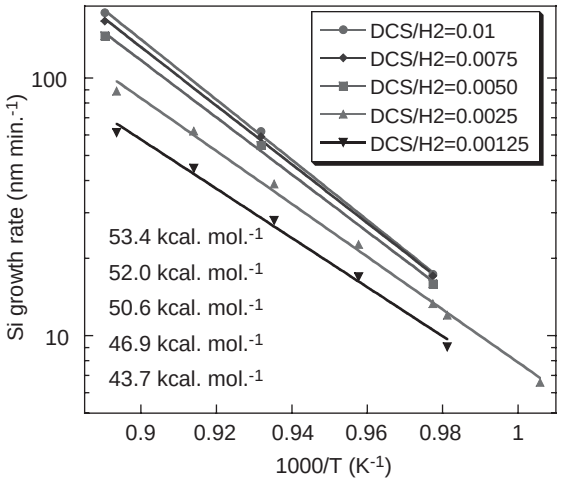

Fig. 4. Arrhenius plot of the Si growth rate as a function of the reverse absolute temperature for several $F(SiH_2Cl_2)/F(H_2)$ mass flow ratios. The associated activation energies E_{GR} (DCS) are reported in the figure.

to increase monotonously from 43.7 up to 53.4 kcal mol^{-1} with the SiH_2Cl_2 partial pressure, which is to the best of our knowledge the first time that such a behavior is reported. A mean value of 49.3 kcal mol^{-1} is associated to E_{GR} (DCS), to be compared to the 52.2 kcal mol^{-1} value of Kongetira et al. [33]. This exponential dependence of the Si growth rate on the reverse absolute temperature is in fact related to the desorption of hydrogen from the silicon surface in order for silicon atoms to be incorporated. An activation energy of 47 kcal mol^{-1} has indeed been found for hydrogen desorption from a Si(1 0 0) surface [34].

We have then plotted at 750°C, 800°C and 850°C the Si growth rate without HCl as a function of the DCS partial pressure in order to determine k_{GR} (DCS) and z (see Fig. 5). Mean values of 6.4×10^{10} and $z = 0.36$ are associated to those two constants. Our z value is half the one of Kongetira et al. (0.7).

We thus have three unknowns remaining, E_{ET}, k_{ET} and y. The Si growth rate with some HCl added is given by:

$$\mathrm{GR}_{\text{with some HCl added}}(\mathrm{nm/min}) = k_{\mathrm{GR}}(\mathrm{DCS})e^{-E_{\mathrm{GR}}(\mathrm{DCS})/k_B T}(P_{\mathrm{DCS}})^z(P_{H_2}) - k_{\mathrm{ET}}e^{-E_{\mathrm{ET}}/k_B T}(P_{\mathrm{HCl}})^y.$$

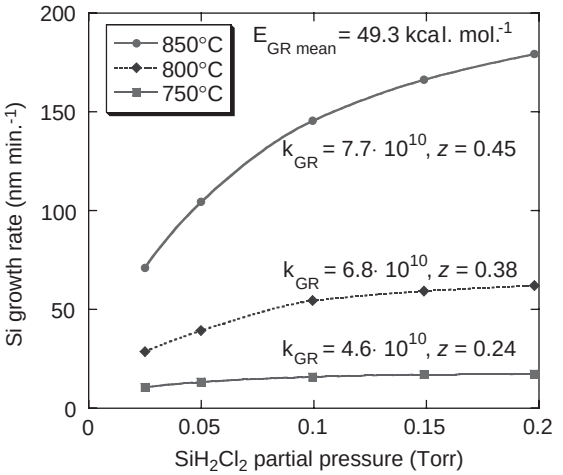

Fig. 5. Si growth rate at 750°C, 800°C and 850°C as a function of the dichlorosilane partial pressure. The associated k_{GR} (DCS) and z values are given next to each curve.

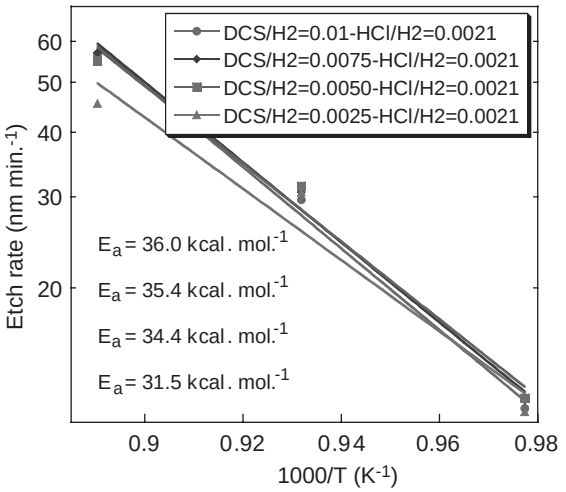

Fig. 6. Arrhenius plot of the Si etch rate by HCl as a function of the reverse absolute temperature for several $F(SiH_2Cl_2)/F(H_2)$ mass flow ratios. The associated activation energies E_{ER} are reported in the figure.

The etching rate by HCl is thus given by (for a given value of the SiH_2Cl_2 flow):

$$\mathrm{ER\ (nm/min)} = k_{ET} e^{-E_{ET}/k_B T} (P_{HCl})^y = \mathrm{GR_{without\ HCl\ added}} - \mathrm{GR_{with\ some\ HCl\ added}}.$$

Proceeding in the same way as before (Arrhenius plot of the etching rate as a function of the reverse absolute temperature, see Fig. 6), values for E_{ET} can be obtained. A mean value of 34.3 kcal mol^{-1} is associated to this etching rate activation energy, to be compared to the 31.1 kcal mol^{-1} value of Kongetira et al.

We have then plotted at 750°C, 800°C and 850°C the Si etching rate as a function of the HCl partial pressure to determine k_{ET} and y (see Fig. 7). Mean values of 1.4×10^9 and $y = 0.52$ are associated to those two constants. Our y value is much lower than the one of Kongetira et al. (1.2).

The Si growth rate (at 20 Torrs on blanket wafers) as a function of the SiH_2Cl_2 and HCl partial pressures (in Torr) and of the absolute temperature is thus given by:

$$\mathrm{GR(nm/min)} = 6.4 \times 10^{10} e^{-49.3\ \mathrm{kcal\ mol^{-1}}/k_B T} \times (P_{DCS})^{0.36} (P_{H_2}) - 1.4 \times 10^9 \times e^{-34.3\ \mathrm{kcal\ mol^{-1}}/k_B T} (P_{HCl})^{0.52}.$$

This expression is valid in the low-temperature, H-desorption limited regime (i.e. $T \leqslant 850$°C).

4.2. The silane chemistry

By analogy with the model adopted just above for the dichlorosilane + hydrochloric acid chemistry, we have decided to use for the low-temperature ($700°C \leqslant T \leqslant 800°C$) modeling of the Si growth rate with a silane chemistry the following equation:

$$\mathrm{GR(nm/min)} = k_{GR}(SiH_4) e^{-E_{GR}(SiH_4)/k_B T} (P_{SiH_4})^w (P_{H_2})$$

We have determined from an Arrhenius plot of the Si growth rate as a function of the reverse absolute temperature (as in Fig. 4) the growth activation energy E_{GR} (SiH_4) for several silane mass flows ($F(SiH_4)/F(H_2)$ in between 0.0025 and 0.01). In opposition to dichlorosilane, the growth activation energy does not really depend upon the silane flow. A value of 50.0 ± 0.8 kcal mol^{-1} is found for E_{GR} (SiH_4), very close to the mean activation energy found for the dichlorosilane chemistry, i.e. E_{GR} (DCS) = 49.3 kcal mol^{-1}.

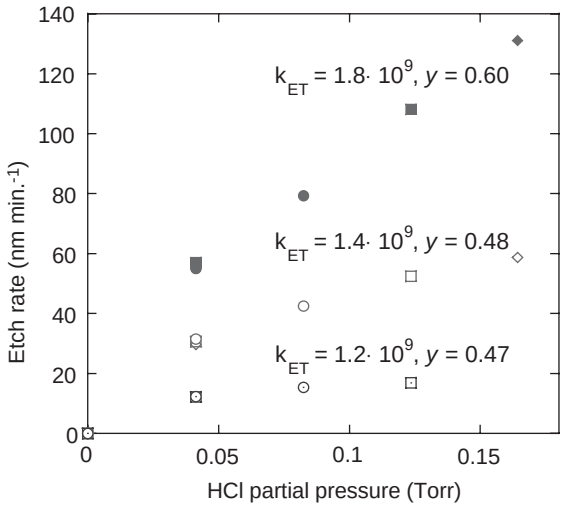

Fig. 7. Si growth rate at 750°C, 800°C and 850°C as a function of the hydrochloric acid partial pressure. The associated k_{ER} and y values are given next to each curve. Lozenges, squares and circles correspond to $F(SiH_2Cl_2)/F(H_2)$ mass flow ratios equal to 0.01, 0.0075 and 0.0050, respectively. Full symbols (open symbols, open symbols with a dot in the middle) correspond to 850°C (800°C, 750°C) etch rates.

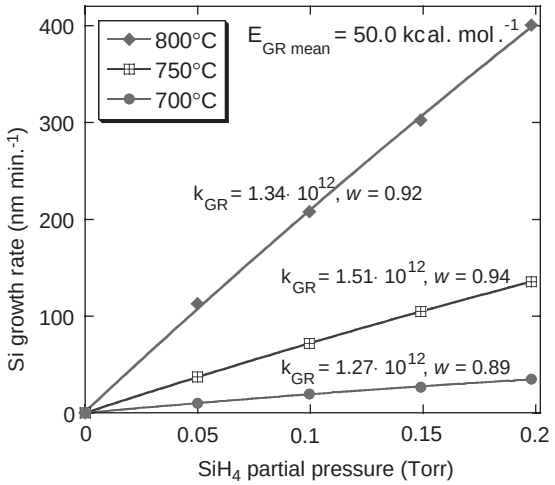

Fig. 8. Si growth rate at 750°C, 800°C and 850°C as a function of the silane partial pressure. The associated k_{GR} (SiH_4) and w values are given next to each curve.

We have then plotted at 700°C, 750°C and 800°C the Si growth rate as a function of the SiH_4 partial pressure in order to determine k_{GR} (SiH_4) and w (see Fig. 8). Mean values of 1.4×10^{12} and $w = 0.92$ are associated to those two constants. We thus have a close to linear ($w = 0.92 \rightleftharpoons 1.0$) dependency of the Si growth rate on the silane partial pressure (in agreement with previously reported results [35]), in stark contrast with the DCS, for which the dependency is strongly sub-linear ($z = 0.36$). The fact that the growth rate is higher for silane that for dichlorosilane at a given temperature for the same mass flows [5] is partially accounted for by a rate constant more than twenty times higher for silane than for dichlorosilane (k_{GR} (SiH_4) $= 1.4 \times 10^{12}$ versus k_{GR} (DCS) $= 6.4 \times 10^{10}$).

The Si growth rate (at 20 Torrs on blanket wafers) as a function of the SiH_4 partial pressure (in Torr) and of the absolute temperature is thus given by:

$$\mathrm{GR(nm/min)} = 1.4 \times 10^{12} e^{-50.0\ \mathrm{kcal\ mol^{-1}}/k_B T} (P_{SiH_4})^{0.92} (P_{H_2}).$$

This expression is valid in the low-temperature, H-desorption limited regime (i.e. $T \leqslant 800$°C).

5. Selective epitaxial growth of Si on patterned wafers

We have also studied the low-temperature selective epitaxial growth of Si on patterned wafers using a dichlorosilane + hydrochloric acid chemistry. 92% of the surface area of those patterned wafers is covered by a 250 nm-thick LOCOS (LOCal Oxydation of Silicon) type thermally grown SiO_2 film. Si windows of varying sizes and shapes (mainly rectangular however, with sides along the $\langle 1\,1\,0 \rangle$ directions) have been defined by optical lithography on each of the 49 dies (18 mm × 18 mm area each) of those patterned wafers. Those windows are approximately 110 nm below the surface of the LOCOS-covered parts of the wafers.

It is quite easy when plotting the Si deposited thickness as a function of the growth time to determine the associated growth rates (see Fig. 9). As far as the growth of Si using a dichlorosilane + hydrochloric acid chemistry is concerned, we have found on patterned wafers at 775°C

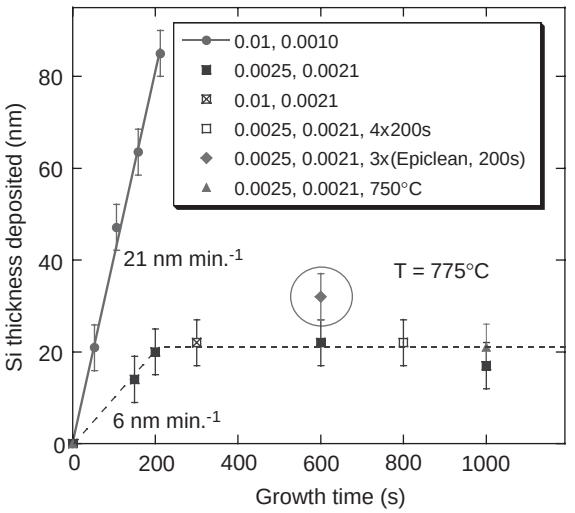

Fig. 9. Si thickness deposited inside ($110\,\mu m \times 110\,\mu m$) Si windows of patterned wafers using a dichlorosilane + hydrochloric acid chemistry as a function of the growth time. The $F(SiH_2Cl_2)/F(H_2)$ and the $F(HCl)/F(H_2)$ mass flow ratios are (from left to right) the first and the second numbers next to each type of symbol in the figure insert, respectively. The Si layer of the 4×200 s sample has been deposited in 4 times 200 s, separated by growth interrupts under H_2 for 50 s. The Si layer of the $3 \times$ (EpiClean, 200 s) sample has been deposited in three times 200 s of growth, separated by ex-situ wet "EpiClean" wet cleaning. The growth temperature was always 775°C, except for one sample (for which it was 750°C).

significant differences between high and low $F(HCl)/F(SiH_2Cl_2)$ mass flow ratios (see Fig. 9).

For a $F(HCl)/F(SiH_2Cl_2)$ mass flow ratio equal to 0.1 (i.e. $F(SiH_2Cl_2)/F(H_2) = 0.01$ and $F(HCl)/F(H_2) = 0.001$), the deposited thickness increases as expected linearly with the deposition time, with an associated growth rate of 21 nm min^{-1}, very close to the one found on fullsheet wafers. Adding some HCl to SiH_2Cl_2 effectively suppresses at 775°C any *global* or *local* loading effect (i.e. the growth rate increase when switching between blanket and patterned wafers, and on patterned wafers between large and small Si windows).

With a $F(HCl)/F(SiH_2Cl_2)$ mass flow ratio equal to 0.8 (i.e. $F(SiH_2Cl_2)/F(H_2) = 0.0025$ and $F(HCl)/F(H_2) = 0.0021$), we are faced at 775°C (and 750°C) with a limitation of the Si thickness deposited inside the Si windows of our patterned wafers at 20 nm. What is quite puzzling however is that over the first 200 s of the growth, the Si growth rate is very close to that found on fullsheet wafers (i.e. 6 nm min^{-1}). Keeping in mind that the balance between the pure growth rate by SiH_2Cl_2 and the etch rate by HCl might be affected by the fact that we are using patterned wafers, we have multiplied by four the SiH_2Cl_2 mass flow with the same HCl mass flow (Si growth rate increase on fullsheet wafers from 6 up to 14 nm min^{-1}), with no apparent effects. Growing for 800 s in 4 times 200 s separated by 50 s of growth interrupt under H_2 (hypothesis that the etch rate becomes more important than the pure growth rate over time on patterned wafers) does not enable to exceed this 20 nm limit either. Thinking that this 20 nm limit might be due to some chemical poisoning of the surface, we have also tried after 200 s of growth to take the wafer out of the cluster tool, clean-up the surface with the "EpiClean" recipe, re-load it, bake it with H_2 and deposit Si for another 200 s, then do this sequence all over again. This way, we have obtained (instead of the nominal 3×20 nm = 60 nm) a Si deposited thickness slightly above 30 nm, which sort of validates at 775°C for high $F(HCl)/F(SiH_2Cl_2)$ mass flow ratios this "chemical poisoning of the surface" theory. It should be noted that this 20 nm limit disappears (for the same SiH_2Cl_2 and HCl mass flows) at 800°C [18].

We have however to be sure that this 20 nm deposited thickness limit is not an experimental artifact linked to an unintended etch of the LOCOS during the growth and thus to a step height measurement which is meaningless. We have therefore exposed 22 nm thick SiO_2 layers (grown at 800°C using a $SiH_4 + N_2O$ chemistry onto Si(0 0 1)) to either a H_2 flow at 1100°C for up to 300 s or to a $HCl + H_2$ gaseous mixture ($F(HCl)/F(H_2) = 0.0021$) at 800°C for up to 1000 s. The thickness difference as measured by SE is at most 0.25 nm, meaning that almost no thermally stable SiO_2 is consumed during a high-temperature H_2 bake (prior to epitaxy) or a selective epitaxial growth using a $SiH_2Cl_2 + HCl$ chemistry. Similar conclusions were reached in the past by Oldham and Holmstrom [36] or Watts and Neudeck [37] (albeit at higher temperatures or higher growth pressures).

6. Si growth kinetics on SOI wafers

Finally, we have worked on the growth of silicon (using either a) on SOIs substrates. State-of-the-art SOI wafers from SOITEC with miscellaneous buried SiO_2 (BOX) and Si over-layers' thickness were used for this study. The eventual thinning of the Si over-layer (from for example the typical 2000 Å thickness of commercial wafers available nowadays down to 100 Å) was carried out thanks to several {dry oxidation–wet de-oxidation} cycles.

We have plotted in Fig. 10 the Si thickness deposited as a function of the growth time on bulk and on ultra-thin Si over-layer SOI substrates, this for a dichlorosilane only chemistry at 750°C or a dichlorosilane + hydrochloric acid chemistry at 800°C. The Si growth rate (slope of the curves) is significantly lower on those ultra-thin SOI wafers than on bulk wafers for both chemistries. What is also quite obvious is that the Si growth rate decreases with the thickness deposited on those ultra-thin SOI substrates, as attested by the slope reduction with time.

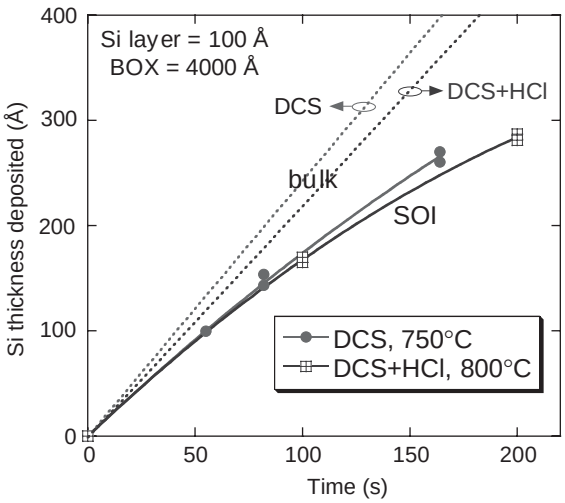

Fig. 10. Si thickness deposited as a function of the growth time on un-patterned bulk (dotted lines) and ultra-thin (Si: 100 Å, BOX: 4000 Å) SOI wafers (symbols linked by full lines). The $F(SiH_2Cl_2)/F(H_2)$ and the $F(HCl)/F(H_2)$ mass flow ratios are equal to 0.0025 and 0.0021, respectively. The growth temperatures are equal to 750°C and 800°C for the dichlorosilane only and the dichlorosilane + hydrochloric acid chemistries, respectively.

We have studied some of those ultra-thin SOI samples on which an epitaxy step was carried out using miscellaneous structural characterization methods. After the deposition of several tens of nm of Si, the surface is smoother, as attested by the lower root mean square roughness than prior to epitaxy: 0.9 Å versus 1.7 Å (AFM, (1 μm × 1 μm) fields). No C, O or F contamination peak was observed in SIMS at the interface between the Si epilayer and the ultra-thin Si layer underneath for the kind of low thermal budget surface preparation described in Section 3 (800°C, 2 min H_2 bake). No interfacial contamination layer is observed in cross-sectional TEM either (see Fig. 11). The Si layer is perfect at the atomic scale, as attested by the absence of any defects such as stacking faults, etc. and by the prolongation of the atomic columns of the ultra-thin Si over-layer in the Si epilayer overhead.

A beneficial side effect of using an epitaxy step to thicken up the Si over-layer lays in the *macroscopic* smoothening of the surface. Indeed, the thickness standard deviation over a 200 mm substrate is typically of the order of 17% just after

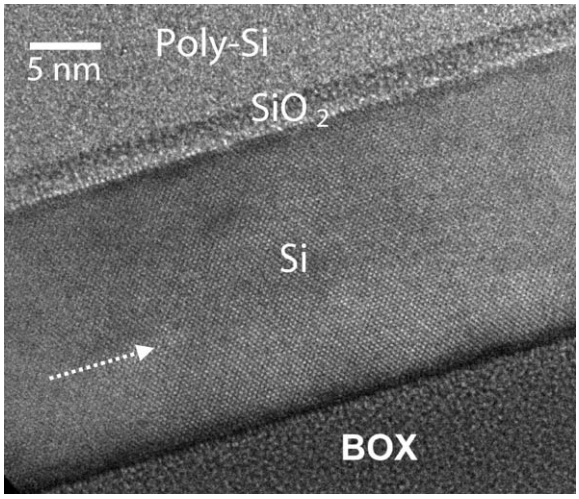

Fig. 11. Cross-sectional high-resolution transmission electron microscopy image of an ultra-thin SOI wafer on which an epitaxy step was carried out (sample subsequently capped by 3 nm of SiO_2 and 75 nm of poly-Si). The dotted arrow shows the approximate boundary between the Si epilayer and the Si seed layer underneath.

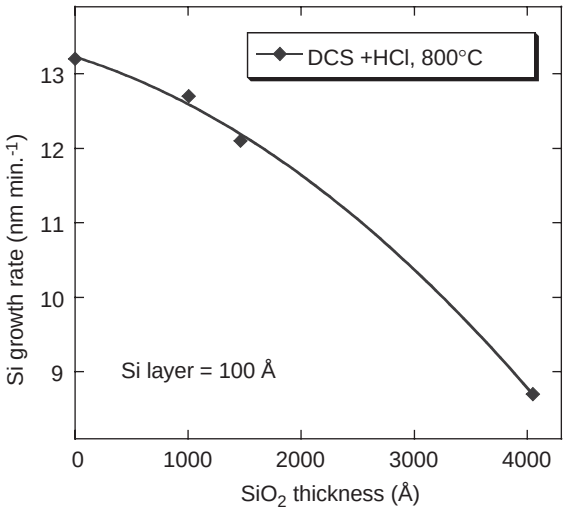

Fig. 12. Si mean growth rate (over 200 s of growth time) on ultra-thin (Si over-layer: 100 Å) SOI wafers as a function of the buried SiO_2 thickness. The $F(SiH_2Cl_2)/F(H_2)$ and the $F(HCl)/F(H_2)$ mass flow ratios are equal to 0.0025 and 0.0021, respectively. The growth temperature is equal to 800°C.

the several {dry oxidation–wet de-oxidation} thinning cycles necessary to bring the Si over-layer thickness from 2000 Å down to 100 Å. After an epitaxy of 100 Å of Si, it drops down to only 3% (49 points wafer mapping in SE).

We have also studied the impact of the BOX thickness upon the growth rate of Si for the SiH_2Cl_2+HCl chemistry at 800°C. Not unexpectedly, the Si growth rate converges towards the bulk value as the buried oxide gets thinner and thinner, as illustrated in Fig. 12. In the same manner, the growth rate, lower than the bulk value for ultra-thin SOI wafers (as illustrated in Fig. 10), increases with the Si over-layer thickness towards the bulk value. Indeed, the mean growth rate (over a 200 s growth time) on 100 Å thick Si over-layers is equal to $8.7\,nm\,min^{-1}$ for the SiH_2Cl_2+HCl chemistry at 800°C (buried oxide thickness: 4000 Å). It goes up to $12.3\,nm\,min^{-1}$ for 1400 Å thick Si over-layers. For bulk Si, it is equal to $13.2\,nm\,min^{-1}$.

To the best of our knowledge, only one other study has dealt with the growth kinetics of Si of SOI wafers [38]. On thicker SOI wafers (4000 Å BOX, 500 Å thick Si over-layers), they have found that the growth rate, while being slightly lower than the bulk value for the first 1500 Å of Si deposited (as in Fig. 10), increased more or less monotonously with the deposited thickness. For 4500 Å of Si deposited, it was 25% higher than the bulk value. The behavior was explained in terms of wafer surface absorptivity and emissivity changes as the Si over-layer got thicker and thicker (see Ref. [38]).

7. Conclusion

Using a RP-CVD cluster tool, we have studied at a growth pressure of 20 Torr the growth kinetics of Si on fullsheet, patterned and SOI wafers using either a dichlorosilane + hydrochloric acid or a silane chemistry.

We have first of all developed a (“HF-last” advanced wet cleaning + an 800°C, 2 min in situ H_2 bake) low-thermal budget combination that yields atomically smooth, C, O and F free Si starting surfaces for both fullsheet and patterned wafers.

We have then modeled semi-empirically the Si growth rate with a dichlorosilane + hydrochloric acid chemistry on fullsheet wafers. It is given at 20 Torrs as a function of the SiH_2Cl_2, H_2 and HCl partial pressures (in Torr) and of the absolute temperature T by

$$\mathrm{GR\ (nm/min)} = 6.4\times10^{10}e^{-49.3\ \mathrm{kcal\ mol^{-1}}/k_BT}(P_{DCS})^{0.36}(P_{H_2}) - 1.4\times10^{9}e^{-34.3\ \mathrm{kcal\ mol^{-1}}/k_BT}(P_{HCl})^{0.52}.$$

This expression is valid in the low-temperature, H-desorption limited regime (i.e. $T<1100$ K). Using silane instead of dichlorosilane as the Si gaseous precursor leads to the following dependency of the Si growth rate at 20 Torrs on the SiH_4 partial pressure and the absolute growth temperature T (valid for $T<950$ K):

$$\mathrm{GR\ (nm/min)} = 1.4\times10^{12}e^{-50.0\ \mathrm{kcal\ mol^{-1}}/k_BT}(P_{SiH_4})^{0.92}(P_{H_2}).$$

On patterned wafers, we are faced at 775°C (and 750°C) with a limitation of the Si thickness deposited selectively inside the Si windows at

20 nm for high $F(HCl)/F(SiH_2Cl_2)$ mass flow ratios. This limit (thought to be due to some sort of chemical poisoning of the surface) disappears when (i) the growth temperature is increased up to 800°C (ii) the $F(HCl)/F(SiH_2Cl_2)$ mass flow ratio is substantially decreased at 775°C.

Finally, we have found that the growth rate is significantly lower on ultra-thin Si over-layer SOI wafers than on bulk ones. The difference between the two kinds of substrates gets less and less pronounced as the buried oxide layer gets thinner and/or the Si over-layer thickness increases. A Si over-layer thickened by an epitaxy step is of high crystalline quality, with a flatter surface and a higher thickness spatial homogeneity over the wafer surface than just after the thinning-down cycles.

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