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Electrical Characterization of Vertically Stacked p-FET SOI Nanowires

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Abstract—This work presents the performance and transport characteristics of vertically stacked p-type MOSFET SOI nanowires (NWs) with inner spacers and epitaxial growth of SiGe raised source/drain. The conventional procedure to extract the effective oxide thickness (EOT) and Shift and Ratio Method (S&R) have been adapted and validated through tridimensional numerical simulations. Electrical characterization is performed for NWs with [110]- and [100]-oriented channels, as a function of both fin width (W_{FIN}) and channel length (L). Results show a good electrostatic control and reduced short channel effects (SCE) down to 15 nm gate length, for both orientations. Effective mobility is found around two times higher for [110]- in comparison to [100]-oriented NWs due to higher holes mobility contribution in (110) plan. Improvements obtained on I_{ON}/I_{OFF} by reducing W_{FIN} are mainly due to subthreshold slope decrease, once small and none mobility increase is obtained for [110]- and [100]-oriented NWs, respectively.

Keywords—performance; transport; electrical characterization; vertically stacked nanowire; SOI MOSFET; channel orientation

I. Introduction

Once increasing the number of gates results in stronger immunity against short channel effects due to higher electrostatic coupling, triple gate (3G) and Gate-All-Around (GAA) MOSFETs attracted the interest of both scientific community and semiconductor industry [1]–[3]. Multiple gate MOSFETs with nanoscale silicon thickness and fin width, also called nanowires, have shown great performance and scalability, turning into one of the best candidates for future technological nodes [2], [4]. In these devices the silicon film thickness and the fin width are of the same order of magnitude.

The use of carrier mobility boosters, such as the implementation of different materials, mechanical stress and rotated substrates, demonstrated to be an important ally to the continuity of the CMOS roadmap, so multiple gate MOSFETs would be able to fulfill higher drive current requests imposed by the International Technology Roadmap for Semiconductors (ITRS). While the use of compressive and tensile stress can enhance holes and electrons mobility, respectively [5], [100]-orientated channel can boost n-type NWs current due to higher electrons mobility along (100) sidewalls [6].

Thanks to advances on tridimensional integration process, vertically stacked nanowires have been fabricated to increase the on-state current by footprint (I_{ON}/W_{FIN}) due to higher device aspect ratio, once the overall channel width (W_{eff}) is proportional to the number of beams [7]–[9]. On the other hand, stacking nanowires makes the reduction of intrinsic parasitic capacitances one of the main challenges to the implementation of such transistors.

Recently, vertically stacked p-type NW MOSFETs have been fabricated combining inner spacers and SiGe source/drain for the first time. This innovative structure aims to contribute for alleviating two problems at the same time, reducing the intrinsic parasitic capacitances and boosting carriers' mobility [9]. In this work, a systematic electrical characterization of these advanced transistors is presented, deepen and expanding the preliminary results of [10] and their interpretation.

Precise EOT extraction is crucial to allow further investigations of any new technology, because EOT consists on an important parameter that defines the structure and it is required in different methodologies of electrical characterization, such as Y-function method [10]. Although wide-planar transistors (W_{FIN} on the order of micrometers) are adequate test structures to extract EOT due to big channel area, such devices are not available as stacked nanowires because limitations during the selective etching step reveals remaining SiGe along the channel of wide stacked MOSFETs. Moreover, using standard fitting procedures of expressions that depend on the W_{eff} may lead to significant errors in EOT because of imprecisions on determining the real W_{eff} of experimental narrow NWs. To overcome these problems, a different approach to extract EOT is presented, based on capacitance measurements, and the results are confirmed by tridimensional numerical simulations.

The Shift and Ratio Method (S&R) was developed and modified in literature to extract the effective physical values for either the channel length or the fin width [11], [12] after the device fabrication. Although the method has been already applied to multiple gate transistors, its implementation considered constant mobility and used planar transistors (W_{FIN} up to 10 μm) as reference devices.

Applying S&R to extract the fin width of aggressive scaled nanowires without using wide-planar transistors as reference requires a modified systematic procedure, which is also proposed in this work.

Performance and transport characteristics are discussed through I_{ON}/I_{OFF} behavior, threshold voltage (V_{TH}), subthreshold slope (SS), DIBL, series resistance (R_S) and effective mobility (μ_{eff}). The discussion on the performance of the fabricated stacked NWs is taken as a function of both fin width and channel length, for NWs orientated along [110] and [100] directions.

The paper is organized as follows: Section II details the devices characteristics. Section III presents the proposed modifications on EOT (Section III-A) and Shift and Ratio (Section III-B) methods, followed by the extracted mentioned electrical (section III-C) and transport (Section III-D) characteristics. Finally, the conclusions of this work are pointed out in Section IV.

II. DEVICES DESCRIPTION

Vertically stacked p-type nanowires MOSFETs with two levels (also called beams) have been fabricated at CEA-LETI, starting from Silicon-On-Insulator (SOI) wafers with 145 nm buried oxide thickness and using a replacement metal gate (RMG) process. Transmission Electron Microscopy (TEM) images of the studied stacked NWs cross section (a) and the longitudinal section (b) are presented in Figure 1. The bottom level NW is Ω-gate (triple gate) type architecture and the top level is GAA one. Each level has a 10 nm thick Si channel (t_{Si}) and both levels are attached by common metal gate and $Si_{0.7}Ge_{0.3}$:B raised source/drain. The transistors have been fabricated in multi finger structures with 50 fins in parallel, along two different crystallographic orientations, [110] and [100], and present a gate stack composed by HfO_2/TiN/W. Further fabrication details of the stacked-NWs studied in this work can be found in [9].

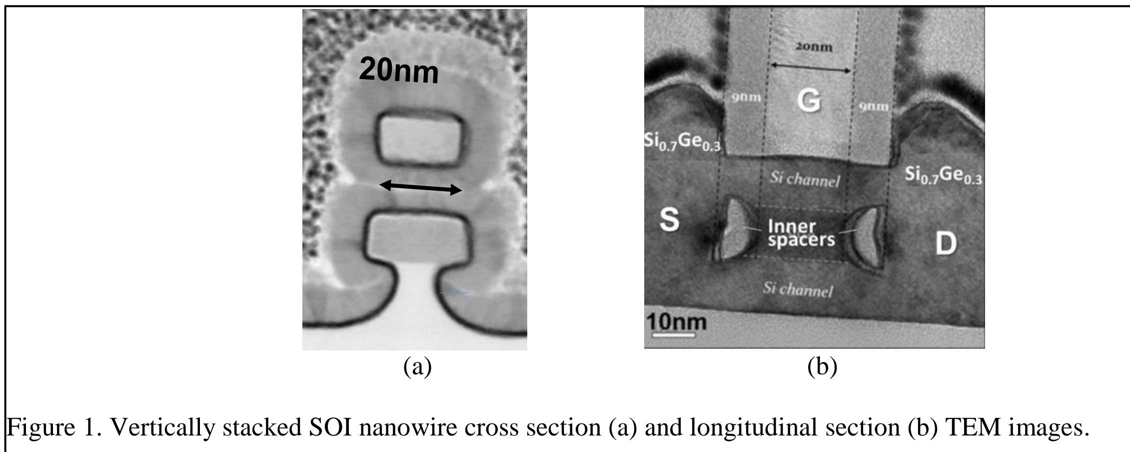

Figure 1. Vertically stacked SOI nanowire cross section (a) and longitudinal section (b) TEM images.

III. RESULTS AND DISCUSSION

A. EOT extraction

In order to extract the EOT obtained from the gate stack deposition process, C-V measurements were performed in stacked NWs with different W_{FIN} and same long L. To overcome the limitation on EOT extraction imposed by the absence of wide stacked NWs, we developed an alternative procedure as follows. By taking the difference between the capacitance of two adjacent transistors with different fin width, $C_{GC,1}$ and $C_{GC,2}$, as indicated in Figure 2, the following expression to the differential gate to channel capacitance per unit of area (C_{GC}') can be obtained:

$$C_{GC}' = \frac{C_{GC,2} - C_{GC,1}}{3 \times \Delta W \times L} \quad (1)$$

It is important to note that C_{GC}' does not dependent on W_{eff} (calculated by $4t_{Si} + 3W_{FIN}$)¸ but on ΔW, which is equal to the difference between the fin width masks, $W_{FIN,mask,2} - W_{FIN,mask,1}$, and consists in a more reliable parameter, since systematic mismatches between the top and bottom levels and between the mask and real fin widths are suppressed.

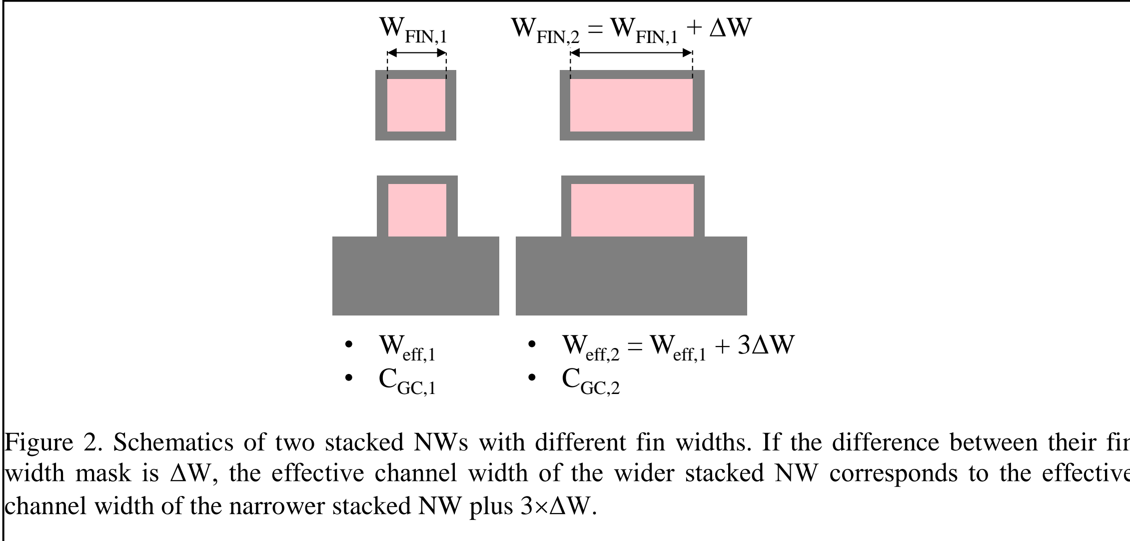

Figure 2. Schematics of two stacked NWs with different fin widths. If the difference between their fin width mask is ΔW, the effective channel width of the wider stacked NW corresponds to the effective channel width of the narrower stacked NW plus $3 \times \Delta W$.

The experimental results of C_{GC}' have been fitted to modelled curves obtained from a 2D Poisson-Schrödinger solver considering quantum confinement effects for fully depleted SOI layers [13], [14]. Fitting procedure has been carried out by comparing measured C_{GC}' values at high gate voltage overdrive ($V_{GT} = V_{GS} - V_{TH}$) to modelled curves to obtain EOT that leads to the best adjustment. Figure 3 presents C_{GC}' as a function of the gate voltage overdrive for stacked NWs with L = 100 nm and ΔW = 50 nm, where the extracted EOT is equal to 1.15 ± 0.1 nm. It is important to mention that the presented methodology can be applied as described in cases where V_{TH} mismatches are observed between the two transistors, because $C_{GC,1}$ and $C_{GC,2}$ are taken at the same V_{GT} to minimize the effect of V_{TH} differences.

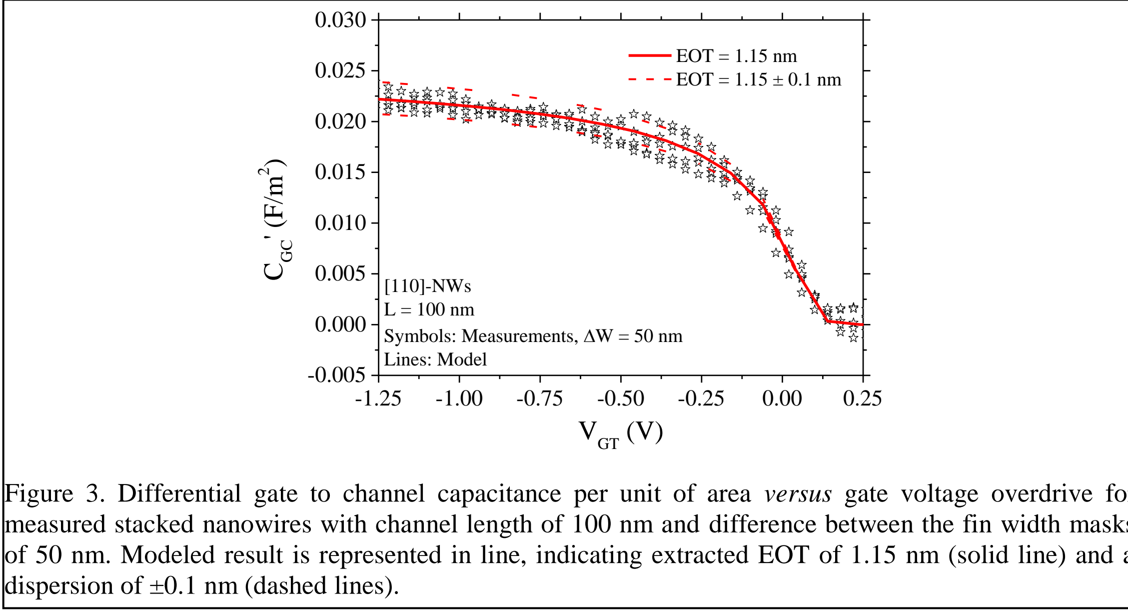

Figure 3. Differential gate to channel capacitance per unit of area *versus* gate voltage overdrive for measured stacked nanowires with channel length of 100 nm and difference between the fin width masks of 50 nm. Modeled result is represented in line, indicating extracted EOT of 1.15 nm (solid line) and a dispersion of ±0.1 nm (dashed lines).

B. Modified Shift and Ratio method

In this section we present a new approach to implement S&R, taking into account the mobility degradation with V_{GS}, which may vary significantly among the nanowires. Moreover, the proposed procedure considers all devices as reference, after analyzing two transistors per time, using the difference among the fin width masks to obtain the final mismatch between mask and real fin widths.

Starting from the basic drain current equation at linear regime, if μ_{eff} is function of V_{GS}, $I_{DS}(V_{GS})$ is given by

$$I_{DS}(V_{GS})=\frac{\mu_{eff}(V_{GS})\times C_{OX}\times W_{eff}}{L}\left(V_{GS}-V_{TH}-\frac{V_{DS}}{2}\right)\times V_{DS} \tag{2}$$

The derivative of the total resistance (S) and the total resistance (R_T) are given by (3) and (4), respectively.

$$S(V_{GS})=\frac{\partial R_T}{\partial V_{GS}} \tag{3}$$

$$R_T(V_{GS})=\frac{V_{DS}}{I_{DS}(V_{GS})} \tag{4}$$

From (2), (3) and (4), S can be written as

$$S(V_{GS})=\frac{-L}{\mu_{eff}(V_{GS})\times C_{OX}\times W_{eff}\times\left(V_{GS}-V_{TH}-\frac{V_{DS}}{2}\right)}\left(\frac{\frac{\partial\mu_{eff}}{\partial V_{GS}}}{\mu_{eff}(V_{GS})}+\frac{1}{V_{GS}-V_{TH}-\frac{V_{DS}}{2}}\right) \tag{5}$$

where C_{OX} is the gate oxide capacitance and V_{TH} is the threshold voltage.

The ratio of the derivative of the total resistance between two devices, discerned by indexes "0" and "i", is

$$r(\delta = V_{TH,0} - V_{TH,i}) = \frac{S_0(V_{GS})}{S_i(V_{GS})} = \frac{\mu_{eff,i}^2(V_{GS}) \times W_{eff,i}}{\mu_{eff,0}^2(V_{GS}) \times W_{eff,0}} \left(\frac{\frac{\partial \mu_{eff,0}}{\partial V_{GS}} \times \left(V_{GS} - V_{TH,0} - \frac{V_{DS}}{2} \right) + \mu_{eff,0}(V_{GS})}{\frac{\partial \mu_{eff,i}}{\partial V_{GS}} \times \left(V_{GS} - V_{TH,i} - \frac{V_{DS}}{2} \right) + \mu_{eff,i}(V_{GS})} \right) \quad (6)$$

where δ indicates that V_{GS} of the device with index "i" must be shifted in $V_{TH,0} - V_{TH,i}$ [11].

$S_0(V_{GS})$ and $S_i(V_{GS} - \delta)$ are obtained from the experimental $I_{DS}(V_{GS})$ curves, through (3), after series resistance correction, and then compared to (6). The experimental I_{DS} can be corrected by the usual expression

$$I_{DS,c}(V_{GS}) = \frac{I_{DS}(V_{GS})}{1 - R_S \frac{I_{DS}(V_{GS})}{V_{DS}}} \quad (7)$$

where $I_{DS,c}$ indicates I_{DS} after series resistance correction and R_S can be extracted through different methods. The series resistance of the studied stacked nanowires and the method used for extraction are shown in section D.

After (6), the ratio between the effective channel widths of devices "i" and "0", $W_{eff,i}/W_{eff,0}$, is obtained. To improve the accuracy of the extraction, each studied stacked nanowire, indexed by "i", is compared to several others, indexed by "0", i. e. different reference devices are considered. Figure 4 shows the extracted $W_{eff,i}/W_{eff,0}$ as a function of the fin width mask of the studied device ($W_{FIN,mask,i}$), for stacked NWs with L = 100 nm, taking three different NWs as references, $W_{FIN,mask,0}$ = 10, 40 and 60 nm. Note that $W_{eff,i}/W_{eff,0}$ is equal to 1 when $W_{FIN,mask,i} = W_{FIN,mask,0}$.

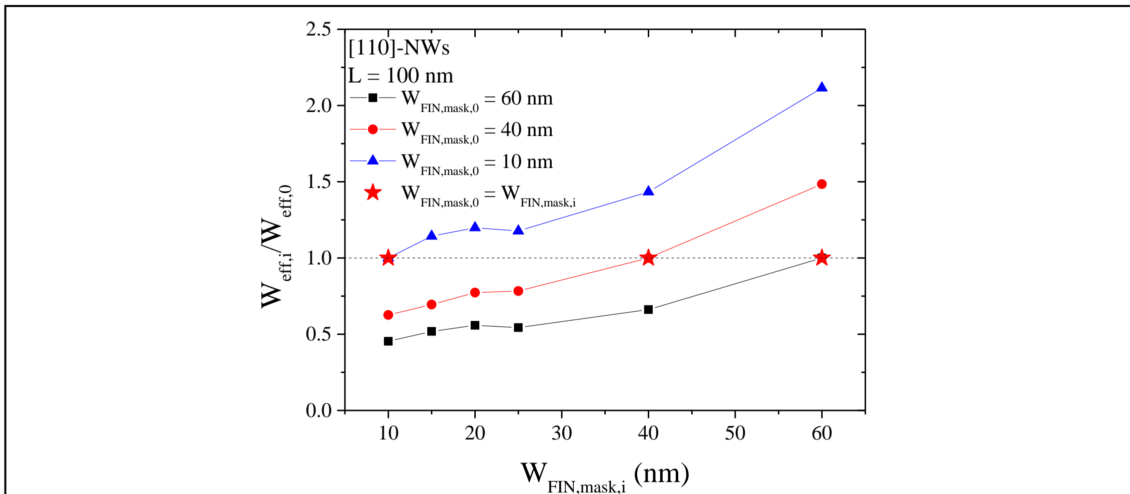

Figure 4. Extracted effective channel width ratio *versus* the fin width mask of the studied device, considering references stacked nanowires with fin width mask of 10, 40 and 60 nm. A dotted line for y-axis equal to 1 indicates when reference and studied devices are the same. Channel length is 100 nm.

Instead of attributing a given fin width for any of the reference devices, the difference between the fin width masks, $\Delta W = W_{FIN,mask,0} - W_{FIN,mask,i}$, will be used to extract the real fin width of each stacked NW, as indicated below:

$$\frac{W_{eff,i}}{W_{eff,0}} = \frac{4t_{Si}+3W_{FIN}}{4t_{Si}+3W_{FIN}+3\Delta W} \tag{8}$$

$$W_{FIN} = \frac{\frac{W_{eff,i}}{W_{eff,0}}(4t_{Si}+3\Delta W)-4t_{Si}}{3\times\left(1-\frac{W_{eff,i}}{W_{eff,0}}\right)} \tag{9}$$

A systematical procedure to extract W_{FIN} through (9) is then applied. Two devices are analyzed per time, until all NWs are compared among them and considered both $W_{FIN,mask,i}$ and $W_{FIN,mask,0}$. Moreover, samples with the same fin width mask are studied in different dies and plotted as a function of the fin width mask, as indicated in Figure 5. A constant mismatch is considered for all W_{FIN}, as expected after process fabrication, once all the silicon fins are defined after the same etching step. Finally, from the analysis of the obtained results, an average mismatch of 5 nm is observed in the real physical W_{FIN}, in respect to the mask values, as highlighted by the dashed line in Figure 5.

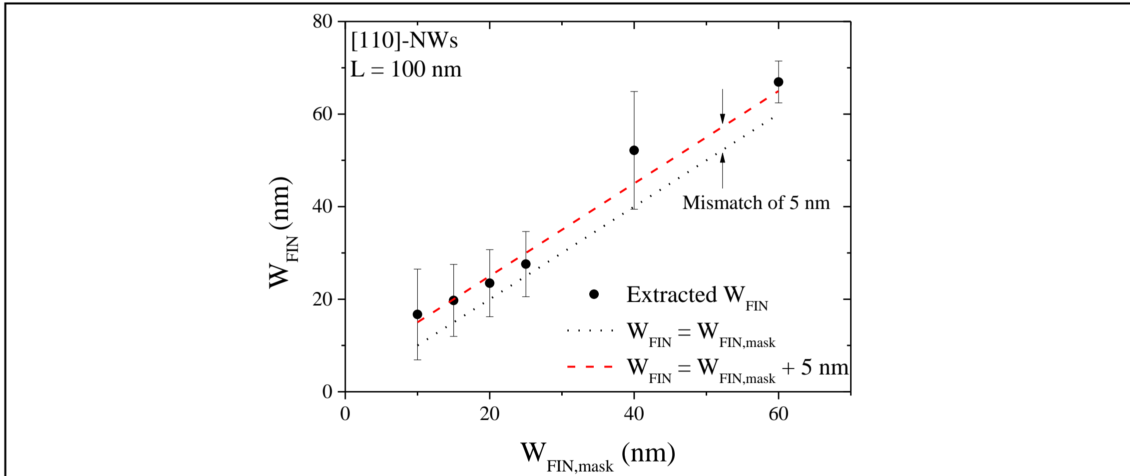

Figure 5. Extracted fin width *versus* the fin width mask for stacked NWs with channel length of 100 nm. The dotted line indicates the ideal case where no mismatch is observed comparing extracted and mask values of W_{FIN}. The dashed line indicates a constant mismatch of 5 nm between extracted and mask values of W_{FIN}, which fits well the extracted W_{FIN} results.

In order to confirm the extracted results of EOT and fin width mismatch, tridimensional numerical simulations were performed using Sentaurus Device Simulator, from Synopsys [15]. Simulations were carried out with quantum effects and the structures were generated through Sentaurus Process, from Synopsys [16].

Figure 6 presents C_{GC} as a function of V_{GT} for simulated stacked NWs with W_{FIN} = 15 nm and EOT of 1.15 ± 0.1 nm (a) and EOT = 1.15 nm and W_{FIN} = 15 ± 3 nm (b). Symbols indicate measurements for devices with $W_{FIN,mask}$ = 10 nm. All simulated and measured devices present L = 100 nm. The dashed lines in Figure 6.a represent numerical simulations considering the dispersion of ±0.1 nm on EOT found with the method applied in Section A. The dashed lines in Figure 6.b indicate numerical simulations resulted from the dispersion of ±3 nm on W_{FIN}, which was necessary to describe all the $C_{GC}(V_{GS})$ curves keeping EOT constant at 1.15 nm. As good description of the measured results were obtained with the tridimensional numerical simulations and small dispersion has been obtained, it is possible to conclude that EOT equal to 1.15 nm and fin width mismatch of 5 nm can be adopted to express the real physical characteristics of the measured stacked NWs. Although EOT extraction and modified Shift and Ratio methodologies are presented for [110]-oriented NWs, the same results are observed for [100]-NWs because all nanowires in both orientations present similar C-V curves, which is expected since they were fabricated together in the same wafer.

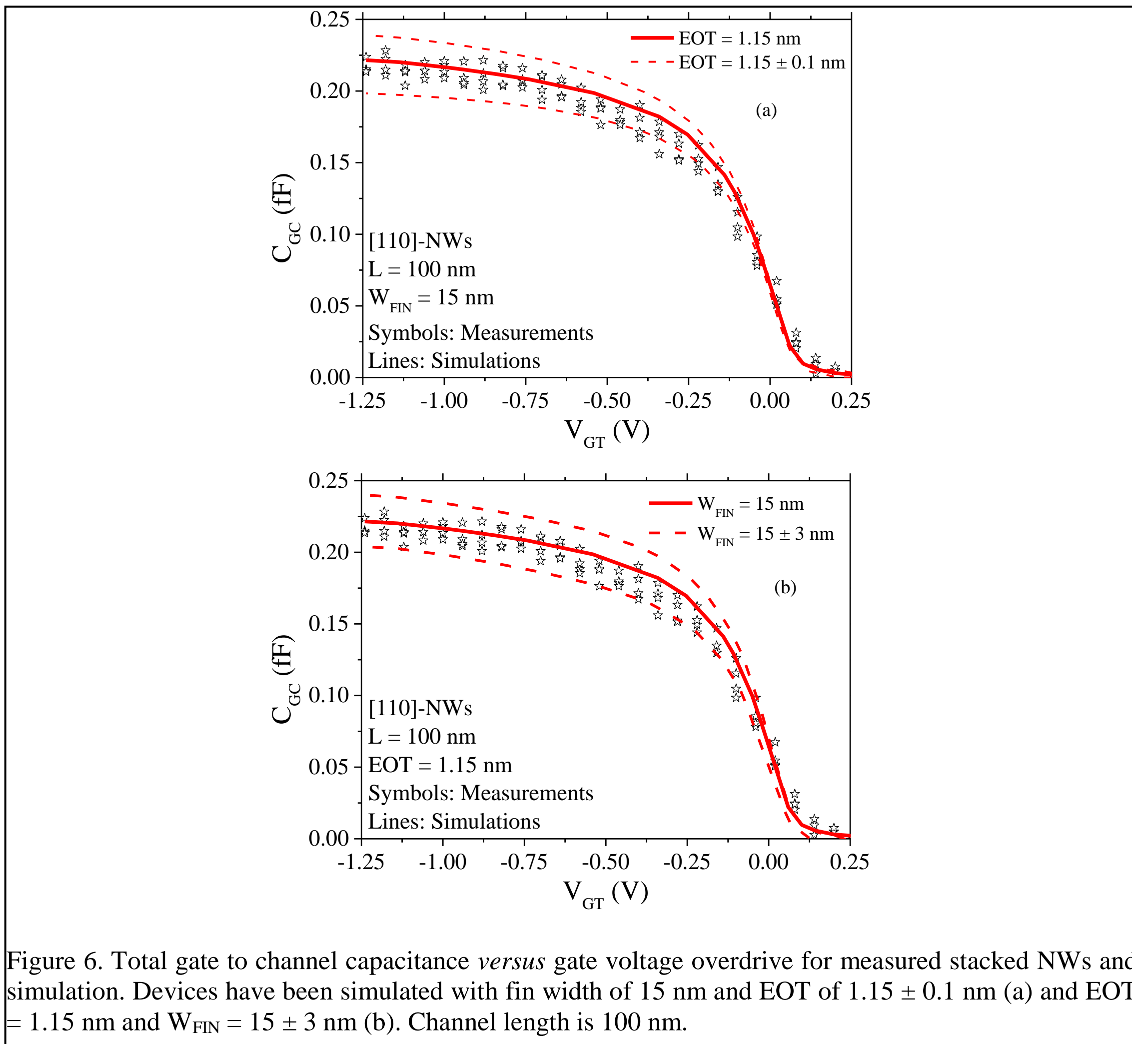

Figure 6. Total gate to channel capacitance *versus* gate voltage overdrive for measured stacked NWs and simulation. Devices have been simulated with fin width of 15 nm and EOT of 1.15 ± 0.1 nm (a) and EOT = 1.15 nm and W_{FIN} = 15 ± 3 nm (b). Channel length is 100 nm.

C. Basic parameters extraction

Figure 7 shows schematics of triple gate nanowires oriented in both [110] and [100] directions. Since the conventional channel orientation for MOSFETs is [110], transistors oriented in [100] direction are rotated in 45° with respect to [110]-MOSFETs (0°). It is observed that [110]-oriented NWs present top and lateral surfaces at (100) and (110) plans, respectively, while [100]-oriented NWs present both top and lateral surfaces at (100) plan. The holes mobility is higher in the (110)-oriented sidewalls in comparison to (100) plan, so [110] is the preferred orientation for p-type NWs [17].

The vertically stacked nanowires analyzed in this work have 4 lateral channels and 3 channels parallel to the top surface. By increasing W_{FIN}, the top surface contribution increases as well, which means that as [110]-NWs become narrower, the overall holes mobility is expected to improve due to increase of (110) plan contribution. On the other hand, as [100]-NWs present all 7 channels at (100) plan, μ_{eff} is expected to be constant with W_{FIN} variation.

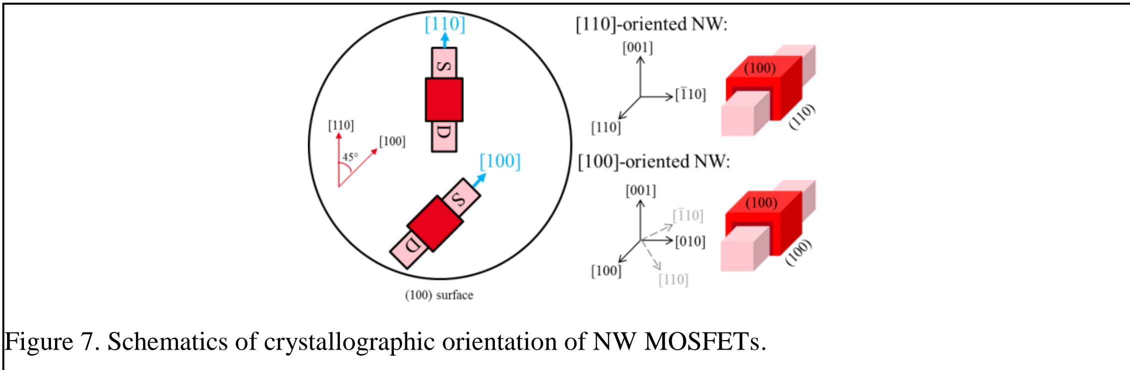

Figure 7. Schematics of crystallographic orientation of NW MOSFETs.

The drain current as a function of V_{GS} for stacked NWs with L = 100 and 30 nm are presented in Figure 8. Both channel orientations are compared at small (a) and strong (b) horizontal electric field, V_{DS} of –40 mV and –0.9 V, respectively. As all devices present the same W_{FIN} but different L, I_{DS} was multiplied by the channel length to emphasize that shorter NWs present lower $|I_{DS}|.L$ due to mobility degradation and increase of series resistance effect. As discussed in Figure 7, higher drain current is observed for stacked [110]-NWs due to higher holes mobility in (110) plan in comparison to (100) plan. Additionally, [18] reported that uniaxial compressive stress, induced in the channel by SiGe source and drain, degrades holes mobility in [100]-oriented NWs. It has been verified that the longitudinal piezoresistive coefficients of [100]-oriented NWs ($\pi_{L,NW}^{[100]}$) decrease with W_{FIN} reduction, reaching high negative values, which characterizes tensile stress. Figure 5 in [18] shows $\pi_{L,NW}^{[100]} < 0$ and clearly indicates detrimental contribution of the applied stress, corroborating with the measured results.

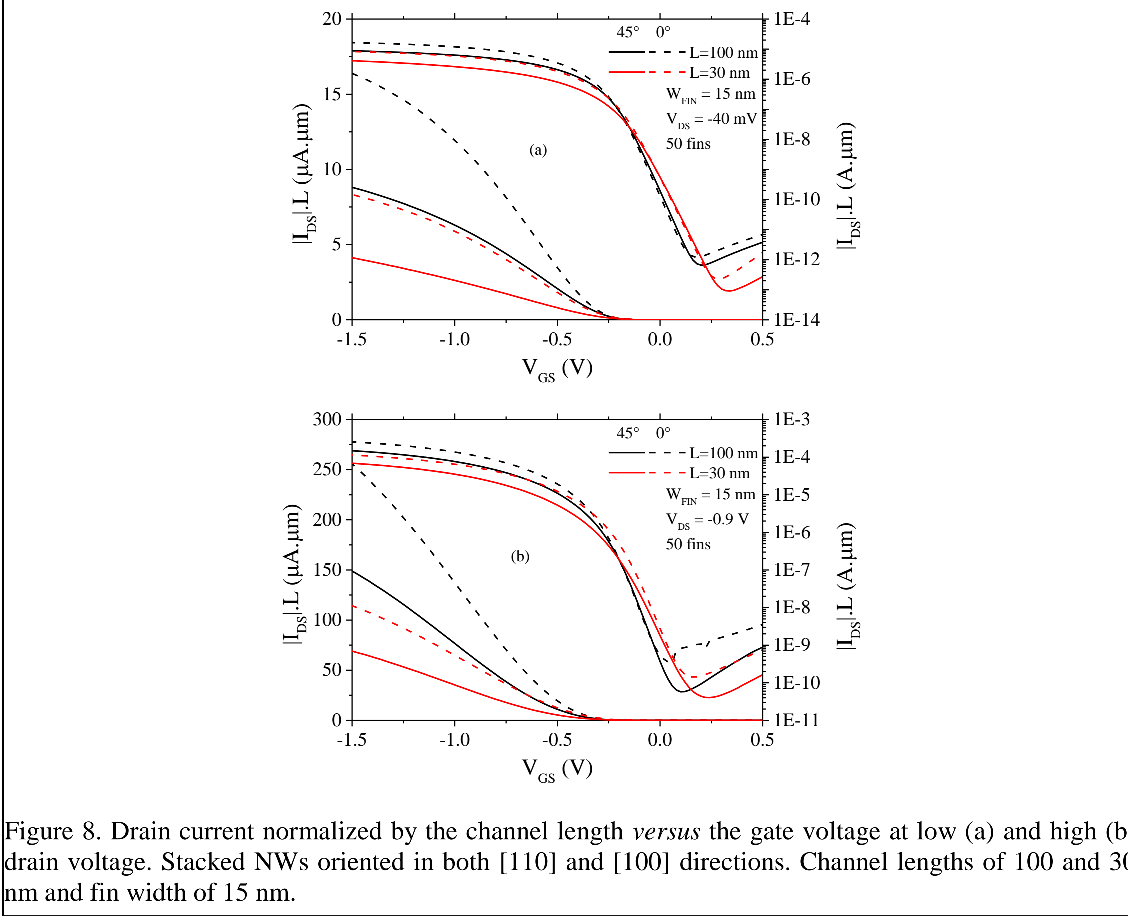

Figure 8. Drain current normalized by the channel length *versus* the gate voltage at low (a) and high (b) drain voltage. Stacked NWs oriented in both [110] and [100] directions. Channel lengths of 100 and 30 nm and fin width of 15 nm.

Figure 9 presents I_{OFF}/W_{eff} as a function of I_{ON}/W_{eff} (a) and I_{ON}/I_{OFF} as a function of W_{FIN} (b) for L = 30 nm, at V_{DS} = –0.9 V. The off-state and on-state currents were extracted at V_{GS} = 0 and –0.9 V, respectively. Figure 9.a presents not only the results normalized by W_{eff}, but also by W_{FIN} for transistors with W_{FIN} = 15 nm. The normalization of I_{ON} by W_{eff} has an important physical meaning, once it calculates the amount of current per micrometer that flows considering all the seven conduction channels formed in both bottom and top levels. On the other hand, stacking two or more levels aims to increase the current by top view area, which can be evaluated only by normalizing I_{ON} by W_{FIN}. I_{ON}/W_{eff} of [110]-oriented NWs reaches up to 450 µA/µm, while I_{ON}/W_{FIN} can reach up to 2500 µA/µm, in comparison to 250 µA/µm (I_{ON}/W_{eff}) and 1100 µA/µm (I_{ON}/W_{FIN}) for [100]-oriented NWs. Moreover, similar off-state current for both channel orientations is observed in Figure 9.a and Figure 9.b shows I_{ON}/I_{OFF} ratio in the order of ~10^4, higher for [110]-oriented NWs and increasing with W_{FIN} reduction. By scaling W_{FIN} from 65 nm down to 15 nm, improvements of 6.3 and 14.1 times are obtained for [110]- and [100]-oriented NWs. I_{ON}/I_{OFF} improvements with W_{FIN} reduction are related to the subthreshold slope decrease, which reduces I_{OFF}, and holes mobility increase, which increases I_{ON}.

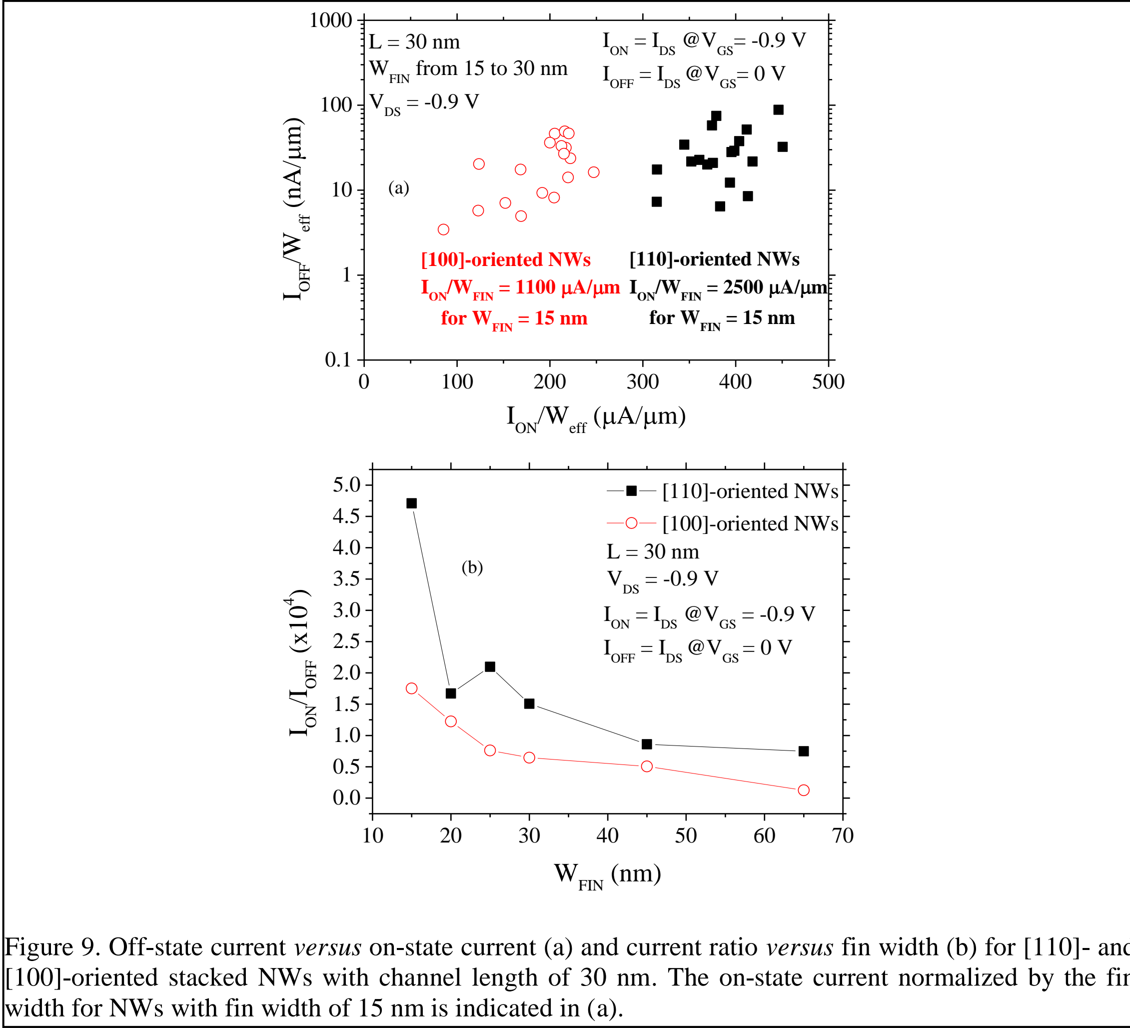

Figure 9. Off-state current *versus* on-state current (a) and current ratio *versus* fin width (b) for [110]- and [100]-oriented stacked NWs with channel length of 30 nm. The on-state current normalized by the fin width for NWs with fin width of 15 nm is indicated in (a).

In order to evaluate the short channel effects the stacked NWs may suffer varying L, Figure 10 shows V_{TH} (a), SS (b) and |DIBL| (c) as a function of L, for [110]- and [100]-oriented NWs with W_{FIN} = 15, 25 and 65 nm. Threshold voltage was extracted by the second derivative method [19]. It is observed that very small V_{TH} roll-off (lower than 60 mV or 24% with respect to the longest device) and subthreshold slope degradation (lower than 18 mV/dec or 26% with respect to the longest device) are observed while reducing L down to 15 nm for [110]-oriented NWs with W_{FIN} of 25 nm, whose SS is lower than 88 mV/dec and |DIBL| is lower than 100 mV/V. Besides both [110] and [100] channel orientations exhibit similar results, as predicted by the logarithmic scaled curves in Figure 8, SS and DIBL results for [100]-oriented NWs with W_{FIN} of 65 nm present higher degradation as L reduces in comparison to [110]-NWs.

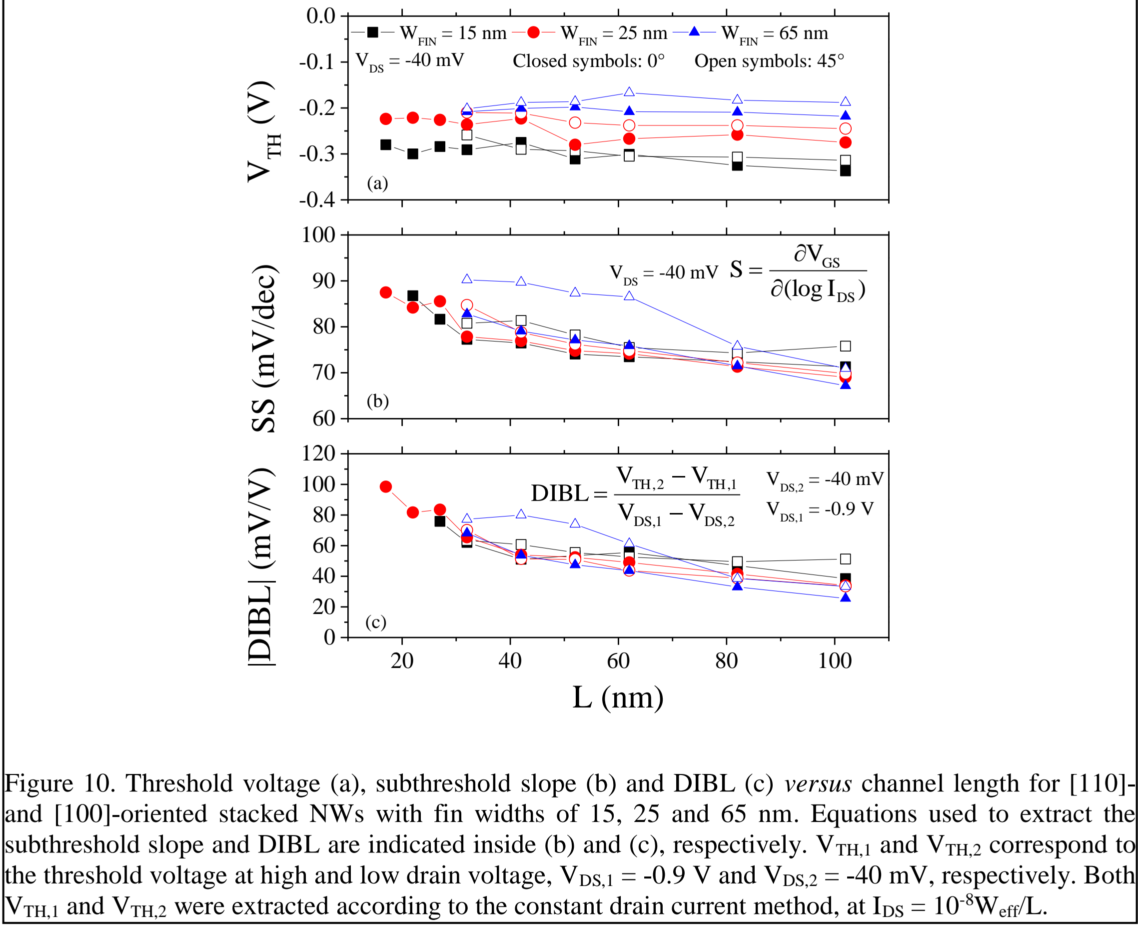

Figure 10. Threshold voltage (a), subthreshold slope (b) and DIBL (c) *versus* channel length for [110]- and [100]-oriented stacked NWs with fin widths of 15, 25 and 65 nm. Equations used to extract the subthreshold slope and DIBL are indicated inside (b) and (c), respectively. $V_{TH,1}$ and $V_{TH,2}$ correspond to the threshold voltage at high and low drain voltage, $V_{DS,1}$ = -0.9 V and $V_{DS,2}$ = -40 mV, respectively. Both $V_{TH,1}$ and $V_{TH,2}$ were extracted according to the constant drain current method, at $I_{DS} = 10^{-8}W_{eff}/L$.

To evaluate the fin width influence on the SCEs, Figure 11 shows V_{TH} (a), SS (b) and |DIBL| (c) as a function of W_{FIN}, for [110]- and [100]-oriented NWs with L = 30, 60 and 100 nm. One can note that V_{TH} varies around 150 mV, comparing W_{FIN} = 65 and 15 nm. Through both SS and |DIBL|, it is observed approximately constant dependence with W_{FIN} for L = 100 nm and 60 nm. For L = 30 nm, 5 and 10 mV/dec of improvement are obtained for SS scaling W_{FIN} down to 15 nm, for [110]- and [100]-oriented NWs, respectively. Stronger short channel effects immunity with W_{FIN} reduction is due to improved electrostatic integrity provided by the better gate control over the charges in the channel region [20]. The subthreshold slope reduction strongly improves the off-state current and the higher SS decrease of [100]-oriented NWs corroborates with their I_{ON}/I_{OFF} increase (14.1 times in comparison to 6.3 times for [110]-oriented NWs, from W_{FIN} = 65 down to 15 nm as discussed in Figure 9).

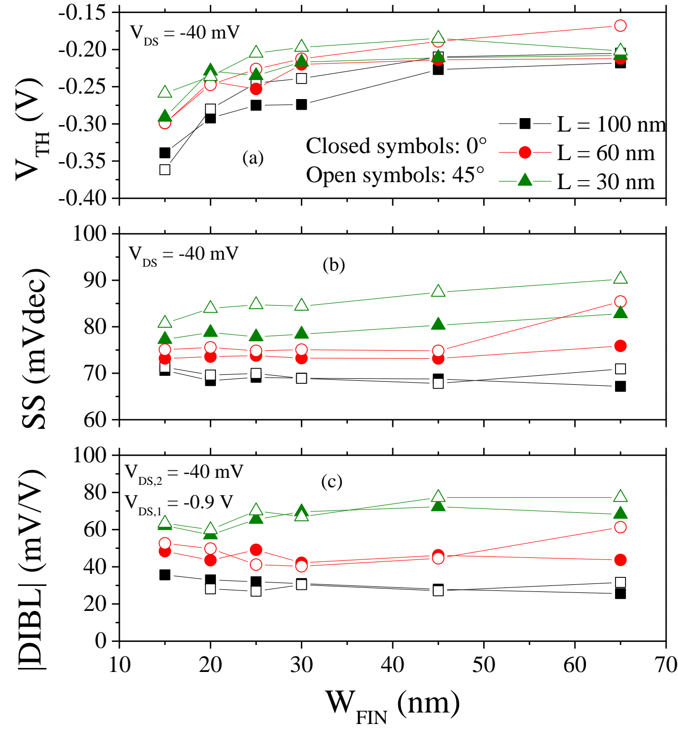

Figure 11. Threshold voltage (a), subthreshold slope (b) and DIBL (c) *versus* fin width for [110]- and [100]-oriented stacked NWs with channel lengths of 30, 60 and 100 nm.

The overall behavior of all parameters (V_{TH}, SS and DIBL) varying both W_{FIN} and L should be similar between vertically stacked nanowires and GAA devices, since the studied NWs are narrow, the Ω-shaped level may induce significant gate control in the bottom surface channel, presenting similar behavior to GAA MOSFETs. Optimized vertically stacked structures would be able to deliver not only high drain current levels due to wide W_{eff}, but also better results for SCE than FinFET-like devices with similar dimensions for W_{FIN} and thicker silicon thickness, once the sum of Ω-shaped bottom level and GAA top level provide better electrostatic coupling improvements for short channel transistors.

D. Transport parameters extraction

Figure 12 shows the results for the total resistance, calculated by (4) and normalized by W_{eff}, as a function of the inverse of the NW gain ($\beta = \mu_{eff}C_{OX}W_{eff}/L$), for [110]- (a) and [100]-oriented (b) NWs, V_{DS} = –40 mV and V_{GT} = –1 V. In these figures the solid straight lines were plotted through the linear regression of all measured data points for each W_{FIN}. The gain of the transistors was extracted following the Y-function method [10] and the crossing points of the straight lines with the y-axis indicate the series resistance. Although some dispersion of the data is observed mainly for narrower transistors, good linearity allowed the extraction of R_S values around 140 and 360 Ωμm, for [110]- and [100]-oriented

NWs, respectively. Approximately the same $R_T.W_{eff}$ values at $1/\beta = 0$ are obtained for all W_{FIN} studied, from 15 to 65 nm, indicating that R_S scales with W_{FIN} for the entire range of L, from 100 down to 15 nm.

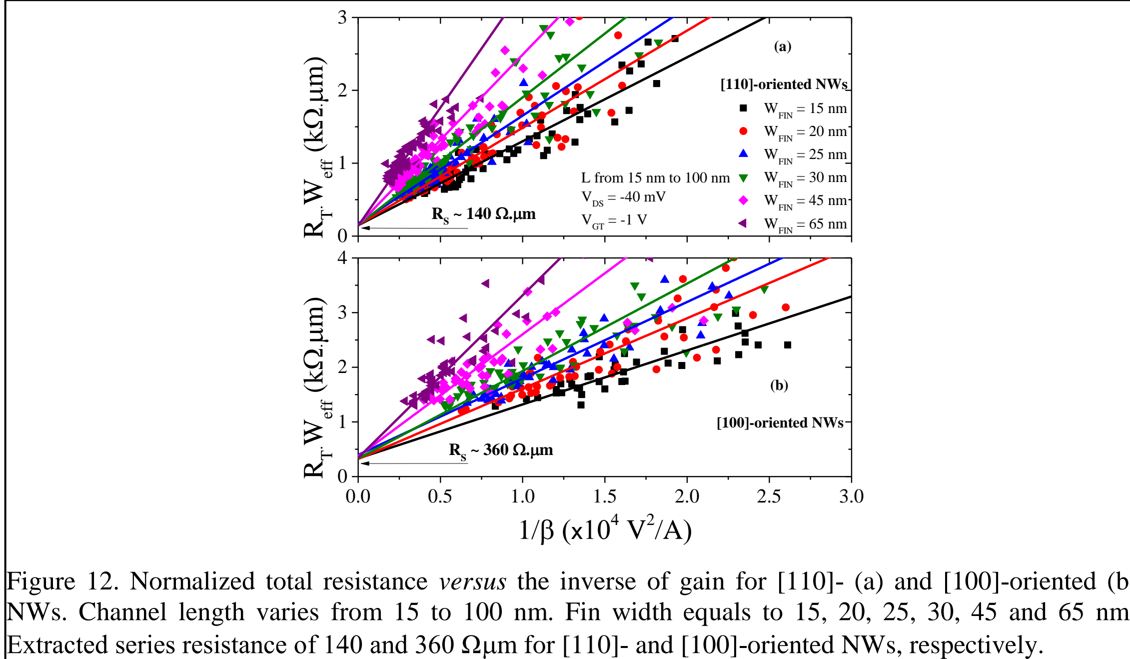

Figure 12. Normalized total resistance *versus* the inverse of gain for [110]- (a) and [100]-oriented (b) NWs. Channel length varies from 15 to 100 nm. Fin width equals to 15, 20, 25, 30, 45 and 65 nm. Extracted series resistance of 140 and 360 Ωµm for [110]- and [100]-oriented NWs, respectively.

After correcting the series resistance effect in the I-V characteristics using (7), a study of the effective holes mobility was performed. Figure 13 shows μ_{eff} as a function of the inversion carrier density (N_{inv}) extracted by split-CV technique [21] for [110]- and [100]-oriented NWs, with L = 100 nm and W_{FIN} = 15 nm. It is indicated that a factor close to 2 separates the maximum mobility for devices in [110] and [100] direction, which agrees with the results obtained for the drain current in Figure 8. The stacked nanowires with channel orientation in [110] direction present higher mobility, lower series resistance and slightly lower subthreshold slope (Figure 11.b), which explains I_{ON}/W_{eff} results obtained in Figure 9.

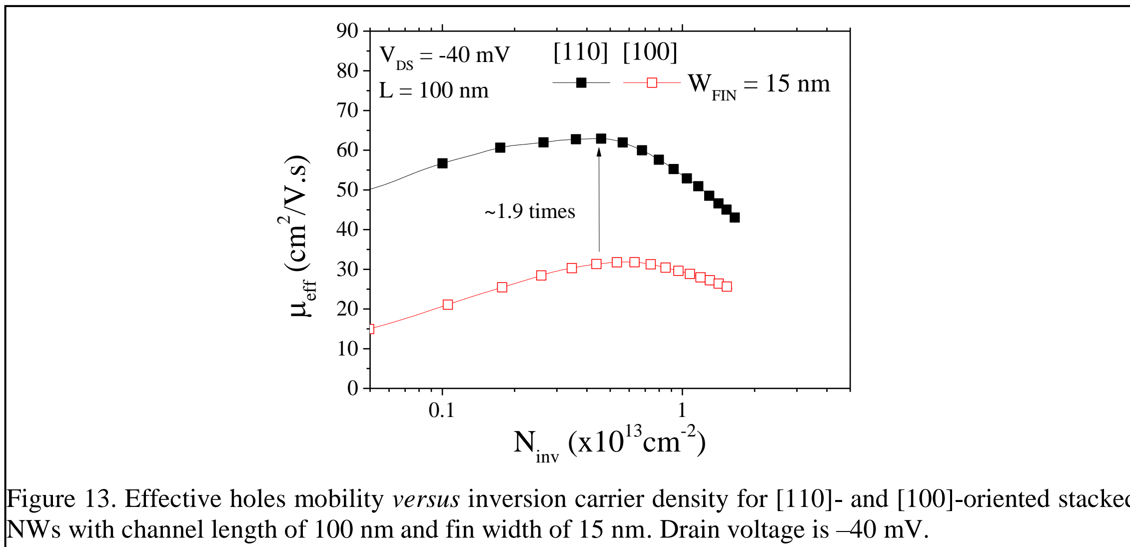

Figure 13. Effective holes mobility *versus* inversion carrier density for [110]- and [100]-oriented stacked NWs with channel length of 100 nm and fin width of 15 nm. Drain voltage is –40 mV.

Figure 14 presents μ_{eff} as a function of L (a), extracted by Y-function method, and as a function of W_{FIN} (b), extracted by split-CV technique. From Figure 14.a, it is observed that mobility is higher for [110]-oriented NWs although they present significant degradation for L < 60 nm. For [100]-oriented NWs, mobility is almost constant down to L = 30 nm, and similar values are obtained varying N_{inv}, as expected from Figure 13, where one can note small degradations of μ_{eff} varying N_{inv}. Figure 14.b shows improvements of up to 17% with W_{FIN} reduction for [110]-NWs, while [100]-NWs show approximately constant behavior, which is agreement with triple gate MOSFETs results [22]. These results indicate that benefits of scaling W_{FIN} down to 15 nm observed in I_{ON}/I_{OFF} (Figure 9.b) are more related to subthreshold slope improvements (decrease of I_{OFF}) than mobility increase (increase of I_{ON}), especially for [100] channel orientation.

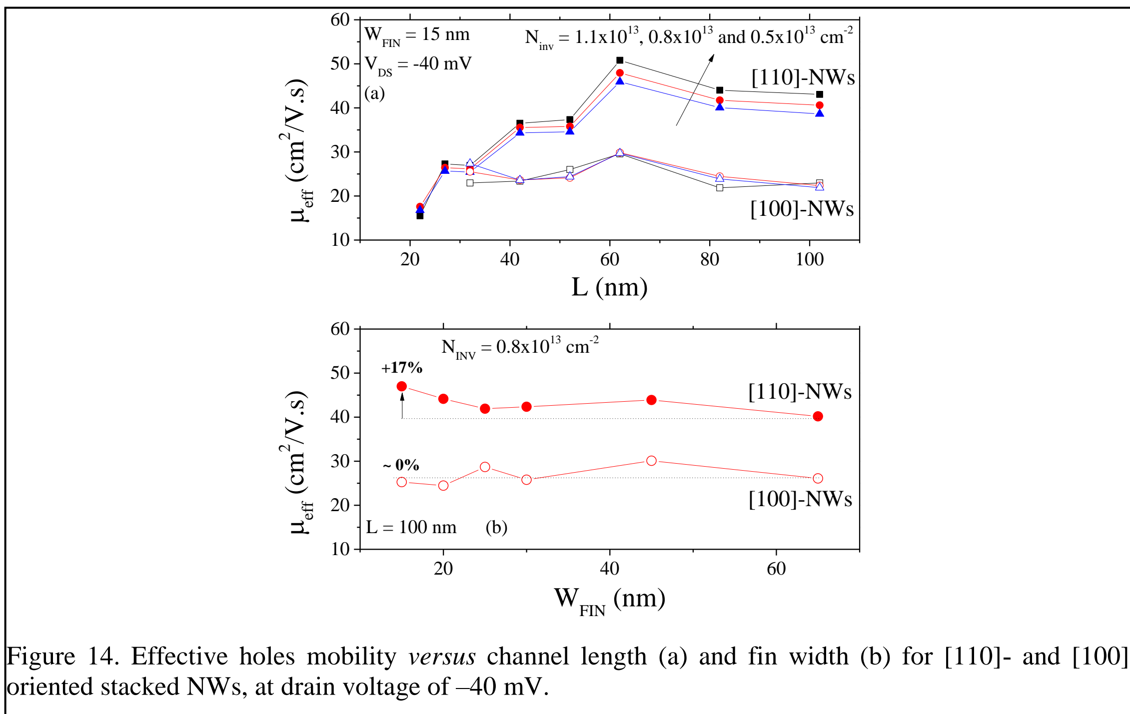

Figure 14. Effective holes mobility *versus* channel length (a) and fin width (b) for [110]- and [100]-oriented stacked NWs, at drain voltage of –40 mV.

IV. Conclusions

This paper depicted the electrical characteristics of vertically stacked p-type nanowires fabricated with inner spacers and SiGe source/drain, as a function of channel length and fin width. To allow for accurate data interpretation, EOT extraction and Shift and Ratio method have been successfully adapted and validated.

High I_{ON}/W_{FIN} has been obtained in two levels stacked NWs (up to 2500 µA/µm for [110]-NWs with L = 30 nm and W_{FIN} = 15 nm), although slightly smaller μ_{eff} is expected in comparison to 3G

MOSFETs due to stronger top surface (100) contribution. While [110]-oriented 3G MOSFETs have 1 interface (over 3) at the (100) plan, [110]-oriented stacked NWs have 3 interfaces (over 7) at the (100) plan.

Excellent SCE control has been obtained for both [110]- and [100]-oriented NWs due to good electrostatic coupling and channel control provided by the sum of Ω-Gate and GAA wires. This conclusion comes after the evaluation of V_{TH}, SS and DIBL degradations down to 15 nm gate length.

Despite complex source and drain engineering, the extracted value of series resistance for [110]-stacked NWs (140 Ωμm) are comparable to those obtained for advanced planar MOSFETs. Transport analysis performed through both split-CV and Y-function method allowed to conclude that, on the same way as for 3G NWs, [110] orientation is better for p-type stacked NWs due to holes mobility improvement in (110)-oriented sidewalls.

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