Performance and Transport Analysis of Vertically Stacked p-FET SOI Nanowires

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***Abstract*—This work presents the performance and transport characteristics of vertically stacked p-MOSFET SOI nanowires (NWs) with inner spacers and epitaxial growth of SiGe raised source/drain. Electrical characterization is performed for NWs with [110] and [100] channel orientations, as a function of both fin width (W_{FIN}) and channel length (L). Results show a good electrostatic control and reduced short channel effects (SCE) down to 15nm gate length. Improved effective mobility is obtained for [110]-oriented NWs due to higher sidewall mobility contribution.**

Keywords—performance; transport; electrical characterization; vertically stacked nanowire; SOI MOSFET; channel orientation.

I. INTRODUCTION

Multiple gate transistors have been designed to improve the electrostatic control of the gate over the charges in the channel, allowing stronger immunity against short channel effects [1]. Since higher electrostatic coupling is obtained increasing the number of gates and reducing the distance among them, triple gate (3G) and Gate-All-Around (GAA) MOSFETs have demonstrated to outperform short channel FinFETs, attracting interest of both scientific community and semiconductor industry [2].

Nanoscale multiple gate MOSFETs called nanowires, characterized by thin silicon thickness and narrow fin width, have shown to be a good alternative to FinFET technology for the continuity of the CMOS roadmap due to their great performance and scalability [3], [4].

To fulfill higher drive current requests imposed by the International Technology Roadmap for Semiconductors (ITRS), the performance of multiple gate structures have been improved through the development of new technologies and implementation of different materials and process techniques, such as mechanical stress and rotated substrates. While the use of compressive and tensile stress can enhance holes and electrons mobility, respectively [5], [100]-orientated channel can boost n-type NWs current due to higher electrons mobility along (100) sidewalls [6].

Recently, vertically stacked NWs have been successfully fabricated due to advanced process developments. These devices combine reduced SCE and improved on-state current (I_{ON}) due to higher device aspect ratio, as the overall channel width (W_{eff}) is increased and proportional to the number of beams [7]–[9].

In this work, we present the performance and transport of vertically stacked p-FET SOI NWs fabricated with inner spacers and SiGe raised source/drain [9]. The analysis is performed as a function of both W_{FIN} and L, for NWs orientated along [110] and [100] directions. Electrical characterization is performed from I-V and C-V curves to evaluate I_{ON}/I_{OFF} behavior, gate-to-channel capacitance (C_{GC}), effective oxide thickness (EOT), threshold voltage (V_{TH}) roll-off, subthreshold slope (S), DIBL, series resistance (R_S) and effective mobility (μ_{eff}).

II. DEVICES CHARACTERISTICS

Vertically stacked NWs with two levels have been fabricated at CEA-LETI, starting from SOI wafers with 145nm buried oxide thickness and using a replacement metal gate (RMG) process. TEM images of the cross section (a) and the longitudinal section (b) of the studied stacked-NWs MOSFETs are presented in Fig. 1. It is observed that the wire at the bottom presents a Ω-shaped gate while the wire at the top is GAA. Both levels have a 10nm thick Si channel and $Si_{0.7}Ge_{0.3}$:B raised source/drain have been used in order to induce a compressive strain of up to 1% in both top and bottom channels [9]. The transistors have been fabricated along two different crystallographic orientations, [110] and [100], and present a gate stack composed by HfO_2/TiN/W. Further fabrication details of the stacked-NWs studied in this work can

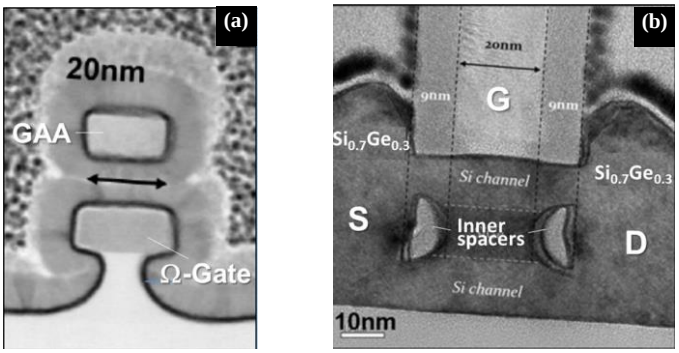

Fig.1. Vertically stacked SOI NW cross section (a) and longitudinal section (b) TEM images.

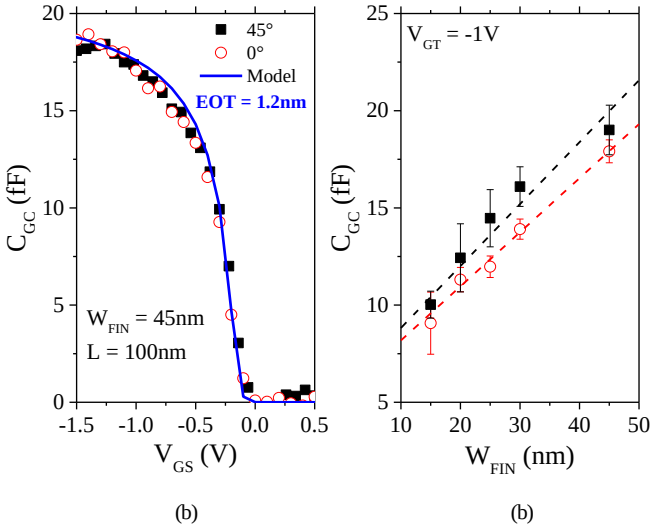

Fig.2. C_{GC} as a function of V_{GS} (a) and C_{GC} as a function of W_{FIN} (b) for [110] and [100]-NWs, L = 100nm. C_{GC} modelling allowed EOT extraction of 1.2nm.

be found in [9].

In order to extract the EOT resulted from the gate stack deposition after RMG process, capacitance measurements were performed and compared to results obtained from a Poisson-Schrödinger solver considering quantum confinement effects for FDSOI MOSFETs. Fig. 2.a presents C_{GC} as a function of V_{GS} for [110]- and [100]-NWs, W_{FIN} = 45nm and L = 100nm. The solid line indicate the modelled result considering EOT of 1.2nm. After fitting the experimental C-V curves, 1.2nm of EOT has been extracted for both transport orientations. Fig. 2.b presents C_{GC} as a function of W_{FIN} for NWs biased at the same gate voltage overdrive ($V_{GT} = V_{GS} - V_{TH} = -1V$). The linear behavior, highlighted by the dashed lines, allows to conclude that EOT is sustained with W_{FIN} scaling and channel orientation, indicating uniform and well controlled gate stack deposition process.

III. Results and Discussion

Fig. 3 presents the normalized drain current (I_{DS}.L) as a function of the gate voltage (V_{GS}) for [110] (0°) and [100] (45°) NWs in multiple finger structures (50 fins), with L = 30nm and 100nm, at small (a) and strong (b) horizontal electric field, V_{DS} of –40mV and –0.9V, respectively. Higher drain current is observed in [110]-NWs, as expected for p-FETs. Indeed, holes mobility is enhanced in the (110)-oriented sidewalls in comparison to (100) plan [10]. Additionally, the SiGe source and drain induce a uniaxial compressive stress, which may become detrimental in narrow p-NWs with [100]-oriented channel. As reported in [11], the longitudinal piezoresistive coefficient of [100]-oriented NWs are lower than zero (see Fig. 5 in [11], where $\pi_{L,NW}^{[100]} < 0$), which degrades even more the holes mobility in such narrow devices. From the logarithmic scaled curves in Fig. 3, it is possible to state that neither by reducing L from 100nm to 30nm nor by decreasing V_{DS} down to –0.9V significant degradations of the subthreshold characteristics are observed.

Fig. 4 presents I_{OFF}/W_{eff} as a function of I_{ON}/W_{eff} (a) and I_{ON}/I_{OFF} as a function of W_{FIN} (b) for L = 30nm, at V_{DS} = –0.9V. I_{OFF} and I_{ON} have been extracted at V_{GS} = 0 and –0.9V, respectively. For W_{FIN} ranging between 15 and 30nm, I_{ON}/W_{eff} of [110]-NWs reaches up to 450µA/µm, while I_{ON}/W_{FIN} can reach up to 2500µA/µm for W_{FIN} = 15nm. The normalization of I_{ON} by the effective channel width (calculated by $4.t_{Si} + 3.W_{FIN}$) has an important physical meaning, once it aims to calculate the amount of current per unit of length that flows considering all the seven conduction channels formed in both bottom and top wires. On the other hand, the normalization of I_{ON} by W_{FIN} allows a comparison from the point of view of the top area, highlighting the benefit of increasing W_{eff} by stacking

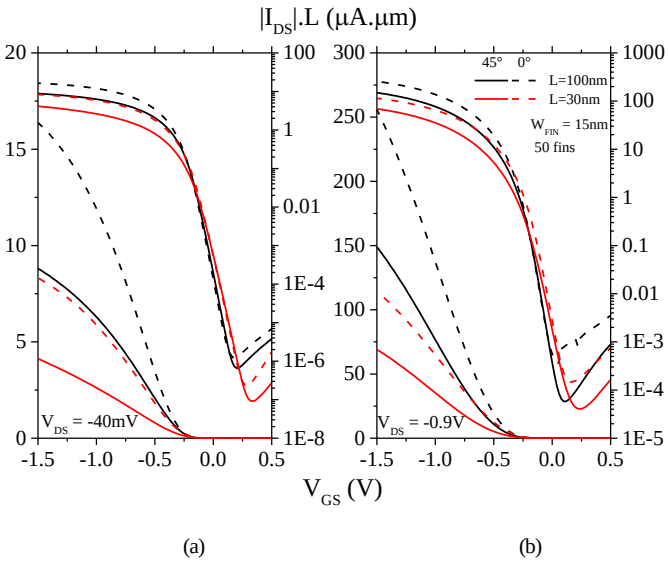

Fig.3. $|I_{DS}|$.L as a function of V_{GS} at V_{DS} = –40mV (a) and –0.9V (b) for [110] and [100]-NWs, L = 100 and 30nm.

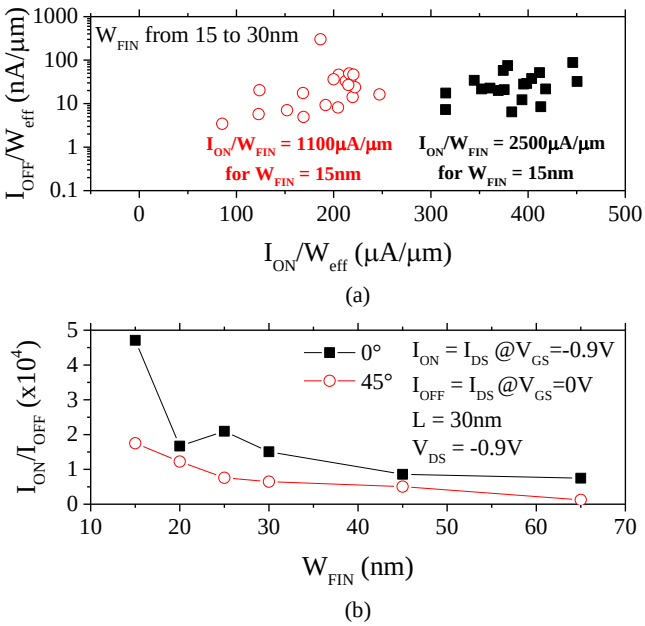

Fig.4. I_{ON}/I_{OFF} characteristics for [110] and [100]-NWs with L = 30nm, at V_{DS} = –0.9V.

2 levels of NWs. Moreover, one can observe similar I_{OFF} for both channel directions and I_{ON}/I_{OFF} ratio in the order of ~10^4, higher for 0° NWs and increasing with W_{FIN} reduction.

Fig. 5.a shows the V_{TH} behavior with W_{FIN} and L, extracted by the second derivative method, at V_{DS} = –40mV. Improvements for narrower NWs and very small V_{TH} roll-off

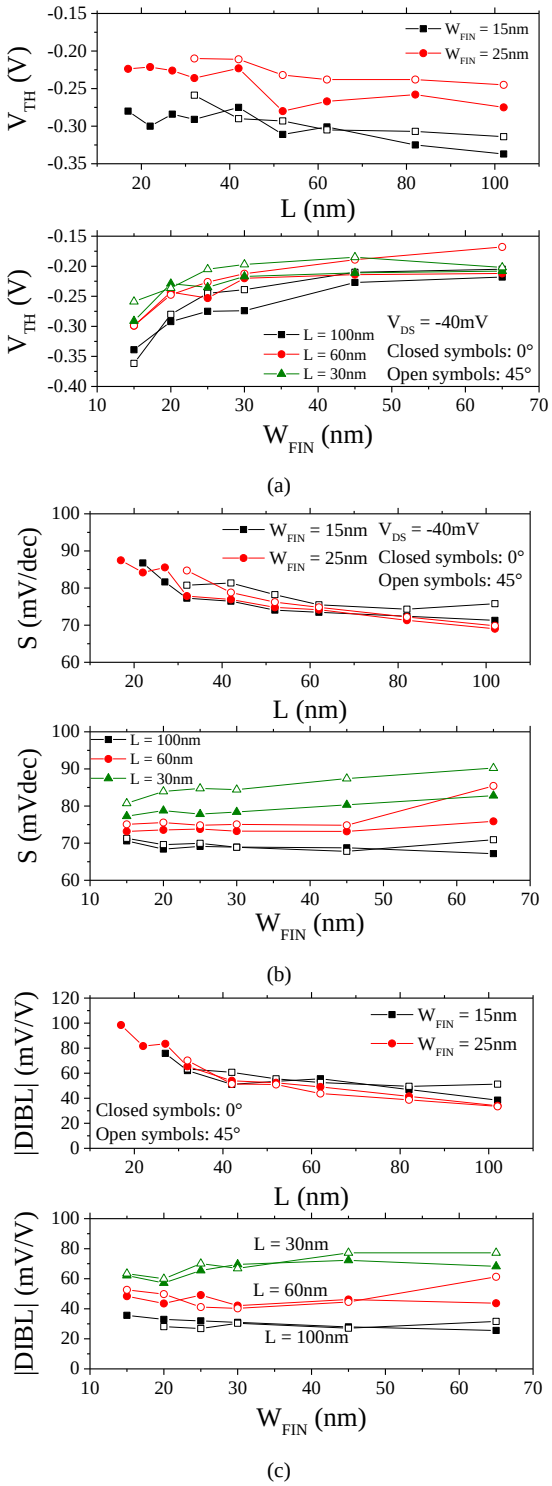

Fig.5. V_{TH} (a), S (b) and |DIBL| (c) as a function of both L and W_{FIN}, for several [110] and [100]-NWs, at V_{DS} = –40mV.

(lower than 60mV) is observed while reducing L down to 15nm. Figs. 5.b and 5.c show, respectively, S and |DIBL| results as a function of W_{FIN} and L. A small subthreshold slope degradation is obtained with channel shortening. For [110]-NWs with W_{FIN} of 25nm, S is lower than 88mV/dec down to L = 15nm. Through both S and |DIBL|, it is observed approximately constant dependence with W_{FIN} for L = 100nm and 60nm, reduced SCE for narrower NWs for L = 30nm and that both [110]- and [100]-NWs exhibit similar results, as predicted by the logarithmic scaled curves in Fig. 3. Besides, |DIBL| is lower than 100mV/V for [110]-oriented NWs with W_{FIN} = 25nm and L down to 15nm.

Fig. 6 shows the results for the total resistance (R_T = V_{DS}/I_{DS}) as a function of the inverse of the NW gain (β), for [110] and [100]-NWs, W_{FIN} of 15, 30 and 65nm, V_{DS} = –40mV and V_{GT} = –1V. From these curves, R_S is extracted following the Y-function method [12]. Good linearity of the data points is demonstrated by the solid lines, which lead to series resistance values around 140 and 360Ω.μm, for [110] and [100]-NWs, respectively. The linear curves observed in Fig. 6 cross the y-axis at the same $R_T.W_{eff}$ value for all W_{FIN} studied, indicating that R_S scales with W_{FIN} for the entire range of L, from 100 down to 15nm.

The hole mobility as a function of the inversion carrier density (N_{inv}) extracted by split-CV technique [13] for L = 100nm and W_{FIN} = 15nm is shown in Fig. 7. The maximum mobility is found equal to 63 and 32cm^2/V.s for standard and rotated NWs, respectively. Moreover, the inner figure shows that the μ_{eff} ratio between both [110] and [100]-NWs is close to 2, which agrees with the I_{ON}/W_{eff} results obtained in Fig. 4.

Fig. 8 presents μ_{eff} as a function of L (a), extracted by Y-function method, and as a function of W_{FIN} (b), extracted by split-CV technique, for several NWs, at N_{inv} of 0.8×10^{13}cm^{-2}. Standard NWs show strong μ_{eff} degradation for L < 60nm while rotated NWs present a constant, but lower, mobility down to L = 30nm. Besides, μ_{eff} shows improvements of up to 17% with W_{FIN} reduction for [110]-NWs, while [100]-NWs

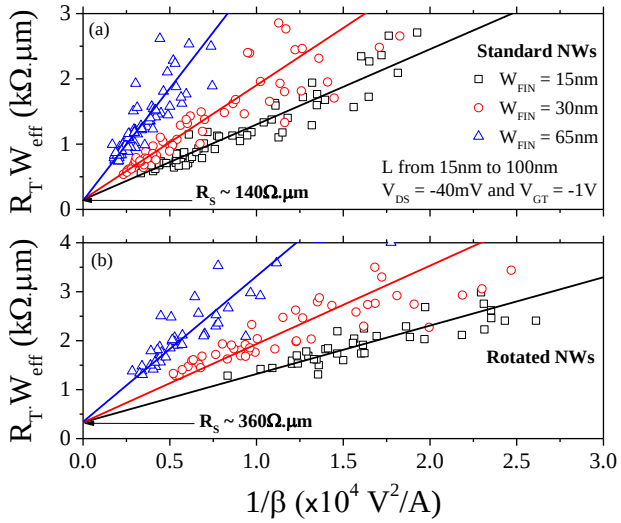

Fig.6. $R_T.W_{eff}$ as a function of 1/β for several [110] (a) and [100]-NWs (b), at V_{DS} = –40mV and V_{GT} = –1V.

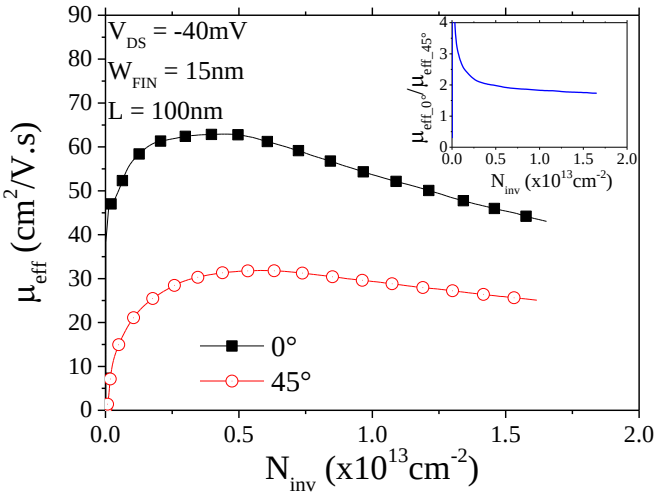

Fig.7. μeff and μeff_0°/μeff_45° as a function of N_{inv} for [110] and [100]-NWs, L = 100nm and W_{FIN} = 15nm, at V_{DS} = –40mV.

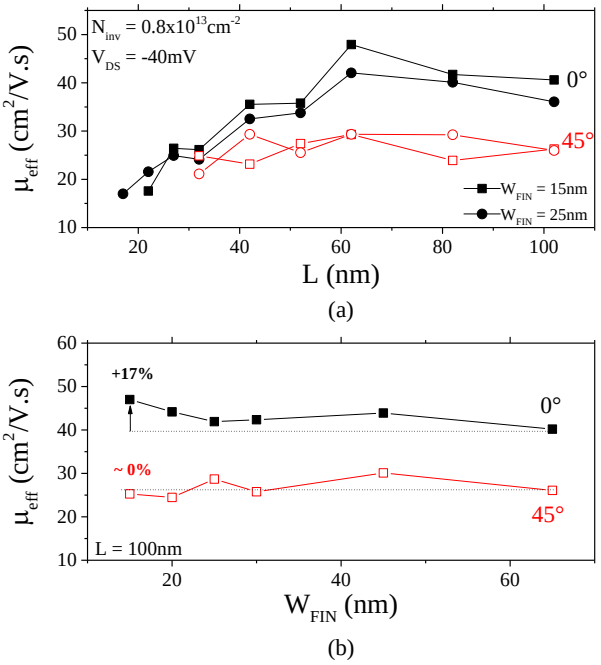

Fig.8. μ_{eff} as a function of L (a) and W_{FIN} (b) for several [110] and [100]-NWs, at N_{inv} = 0.8×10^{13}cm^{-2} and V_{DS} = –40mV.

show constant behavior, which is agreement with triple gate MOSFETs results [14].

IV. Conclusions

Two levels stacked NWs present high I_{ON}/W_{FIN} (up to 2500μA/μm for [110]-NWs), although smaller μ_{eff} is expected for stacked p-NWs in comparison to 3G MOSFETs due to stronger top surface (100) contribution.

Despite complex source and drain engineering, the small values of series resistance extracted for [110]-stacked NWs are comparable to those obtained for advanced planar MOSFETs.

Excellent SCE control (small V_{TH}, S and DIBL degradations down to 15nm gate length) have been obtained for both [110] and [100]-oriented NWs due to good electrostatic coupling and channel control provided by the sum of Ω-Gate and GAA wires.

On the same way as for 3G NWs, [110] orientation is better for p-type stacked NWs due to hole mobility improvements in (110)-oriented sidewalls.

Acknowledgments

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References

[1] J.-P. Colinge, "Multiple-gate SOI MOSFETs," *Solid-State Electron.*, vol. 48, no. 6, pp. 897–905, Jun. 2004.

[2] K. J. Kuhn, "Considerations for Ultimate CMOS Scaling," *IEEE Trans. Electron Devices*, vol. 59, no. 7, pp. 1813–1828, Jul. 2012.

[3] R. Coquand *et al.*, "Strain-induced performance enhancement of tri-gate and omega-gate nanowire FETs scaled down to 10nm Width," in *2012 Symposium on VLSI Technology (VLSIT)*, 2012, pp. 13–14.

[4] R. Coquand *et al.*, "Scaling of high-k/metal-gate Trigate SOI nanowire transistors down to 10nm width," in *2012 13th International Conference on Ultimate Integration on Silicon (ULIS)*, 2012, pp. 37–40.

[5] S. Barraud *et al.*, "Strained Silicon Directly on Insulator N- and P-FET nanowire transistors," in *2014 15th International Conference on Ultimate Integration on Silicon (ULIS)*, 2014, pp. 65–68.

[6] M. Saitoh *et al.*, "Short-channel performance and mobility analysis of <110>- and <100>-oriented tri-gate nanowire MOSFETs with raised source/drain extensions," in *2010 Symposium on VLSI Technology*, 2010, pp. 169–170.

[7] H. Mertens *et al.*, "Gate-all-around MOSFETs based on vertically stacked horizontal Si nanowires in a replacement metal gate process on bulk Si substrates," in *2016 IEEE Symposium on VLSI Technology*, 2016, pp. 1–2.

[8] C. Dupre *et al.*, "15nm-diameter 3D stacked nanowires with independent gates operation: ΦFET," in *2008 IEEE International Electron Devices Meeting*, 2008, pp. 1–4.

[9] S. Barraud *et al.*, "Vertically stacked-NanoWires MOSFETs in a replacement metal gate process with inner spacer and SiGe source/drain," in *2016 IEEE International Electron Devices Meeting (IEDM)*, 2016, p. 17.6.1-17.6.4.

[10] S. Takagi, A. Toriumi, M. Iwase, and H. Tango, "On the universality of inversion layer mobility in Si MOSFET's: Part II-effects of surface orientation," *IEEE Trans. Electron Devices*, vol. 41, no. 12, pp. 2363–2368, Dec. 1994.

[11] J. Pelloux-Prayer *et al.*, "Study of the piezoresistive properties of NMOS and PMOS Ω-gate SOI nanowire transistors: Scalability effects and high stress level," in *Electron Devices Meeting (IEDM), 2014 IEEE International*, 2014, p. 20.5.1-20.5.4.

[12] G. Ghibaudo, "New method for the extraction of MOSFET parameters," *Electron. Lett.*, vol. 24, no. 9, pp. 543–545, Apr. 1988.

[13] A. Ohata, M. Cassé, and S. Cristoloveanu, "Front- and back-channel mobility in ultrathin SOI-MOSFETs by front-gate split CV method," *Solid-State Electron.*, vol. 51, no. 2, pp. 245–251, Feb. 2007.

[14] J. Pelloux-Prayer *et al.*, "Transport in TriGate nanowire FET: Cross-section effect at the nanometer scale," in *2016 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)*, 2016, pp. 1–2.