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A simple interpolation model for the carrier mobility in Trigate and gate-all-around silicon NWFETs

Zaiping Zeng, François Triozon, Sylvain Barraud and Yann-Michel Niquet

Abstract—We compute the electron and hole mobilities in Trigate and gate-all-around silicon nanowires (SiNWs) within the non equilibrium Green’s Functions (NEGF) framework. We then derive a simple model for the dependence of the mobility on the SiNW width and height. This model interpolates between the square SiNW and thin film limits. In order to provide a complete description of the mobility in SiNW devices, we calculate the phonon, surface roughness and remote Coulomb limited mobilities of square nanowires and of thin films with side or thickness $t = 5, 7$ and 10 nm. The mobility of arbitrary rectangular SiNWs with width $W = t$ or height $H = t$ can then be reconstructed from these partial mobilities using Matthiessen’s rule. We show that these models successfully reproduce the trends measured on n - and p -type devices with different widths and orientations.

Index Terms—Green’s functions; Mobility; Nanowire devices

I. INTRODUCTION

FOR the past two decades, metal-oxide-semiconductor field-effect transistors have evolved from planar, single-gate to three-dimensional multi-gate structures such as Trigate and Gate-all-around (GAA) silicon nanowire (SiNW) devices [1]–[4]. The transport properties of SiNWs channels have been extensively studied, both experimentally [5]–[11] and theoretically [12]–[29]. Nonetheless, the transition from rectangular SiNWs to thin films remains unclear. A facet model has been widely used to interpret the size dependence of the carrier mobility in rectangular SiNWs devices [8], [11]. In this model, the SiNW is split into four independent facets, which are assumed to behave as planar channels. However, the facet model does not always reproduce the experimental trends. Sekaric *et al.* have related these discrepancies to the formation of “corner channels” in SiNWs [8]. The simplest facet model also likely breaks down in ultra-thin SiNWs where the carriers flow closer to the axis of the device.

In this work, we compute the carrier mobility in n -type and p -type Trigate and GAA silicon nanowire field effect transistors (NWFETs) with [100] and [110] orientations. We use a non-equilibrium Green’s Functions (NEGF) approach

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[30], which explicitly accounts for quantum confinement and carrier scattering by phonons (PH), surface roughness (SR) and remote Coulomb charges (RCS) (section II). Based on the numerical results, we develop a simple but effective model that describes the size dependence of the carrier mobility in rectangular SiNWs over a wide range of dimensions (section III). This model only takes the mobilities of the thin film devices and of the square NW devices as inputs. These two limits are widely studied experimentally, and are among the easiest to address numerically. In order to provide a complete description of the mobility in these devices, we also compute the partial PH, SR and RCS electron and hole mobilities, for square NW and planar devices with different thicknesses and orientations. We finally show that these models successfully reproduce the experimental trends for different channel orientations (section IV).

II. DEVICES AND METHODOLOGY

The simulated devices are undoped, rectangular GAA and Trigate SiNW channels with width W and height H . The Trigate devices are etched in a (001) Silicon-On-Insulator (SOI) layer. They are lying on a 25 nm thick buried oxide (BOX), and either a n -doped substrate for n -NWFETs (donor concentration $N_d = 10^{18} \text{ cm}^{-3}$) or a p -doped substrate for p -NWFETs (acceptor concentration $N_a = 10^{18} \text{ cm}^{-3}$). All facets except the bottom one are surrounded by the gate. We consider both [100] [with {001} facets] and [110] [with horizontal (001) and vertical ($\bar{1}\bar{1}0$) facets] channel orientations. The gate-stack is made of 0.6 nm of SiO_2 (dielectric constant $\epsilon = 3.9$) and 2.4 nm of HfO_2 ($\epsilon = 20$). Surface roughness disorder (and remote Coulomb charges at the $\text{SiO}_2/\text{HfO}_2$ interface when specified) are explicitly included in the geometries. We use a Gaussian auto-correlation function model for SR with correlation length $\Lambda_{\text{SR}} = 1.0$ nm [31]. The current is computed in a self-consistent NEGF framework [30], [32], on top of the effective mass approximation (EMA) or two bands $\mathbf{k} \cdot \mathbf{p}$ model for electrons, and on top of the three bands $\mathbf{k} \cdot \mathbf{p}$ model for holes. The NEGF equations are solved in a fully coupled mode space approach (80 modes to 420 modes depending on the device cross section and on the band structure model), on a finite differences grid with step 2 \AA . Carrier-phonon scattering is described by local, imaginary self-energies and the deformation potential theory. For electron-phonon scattering, we include intra-valley acoustic phonon scattering (with deformation potential $D_{\text{ac}} = 14.6 \text{ eV}$) and

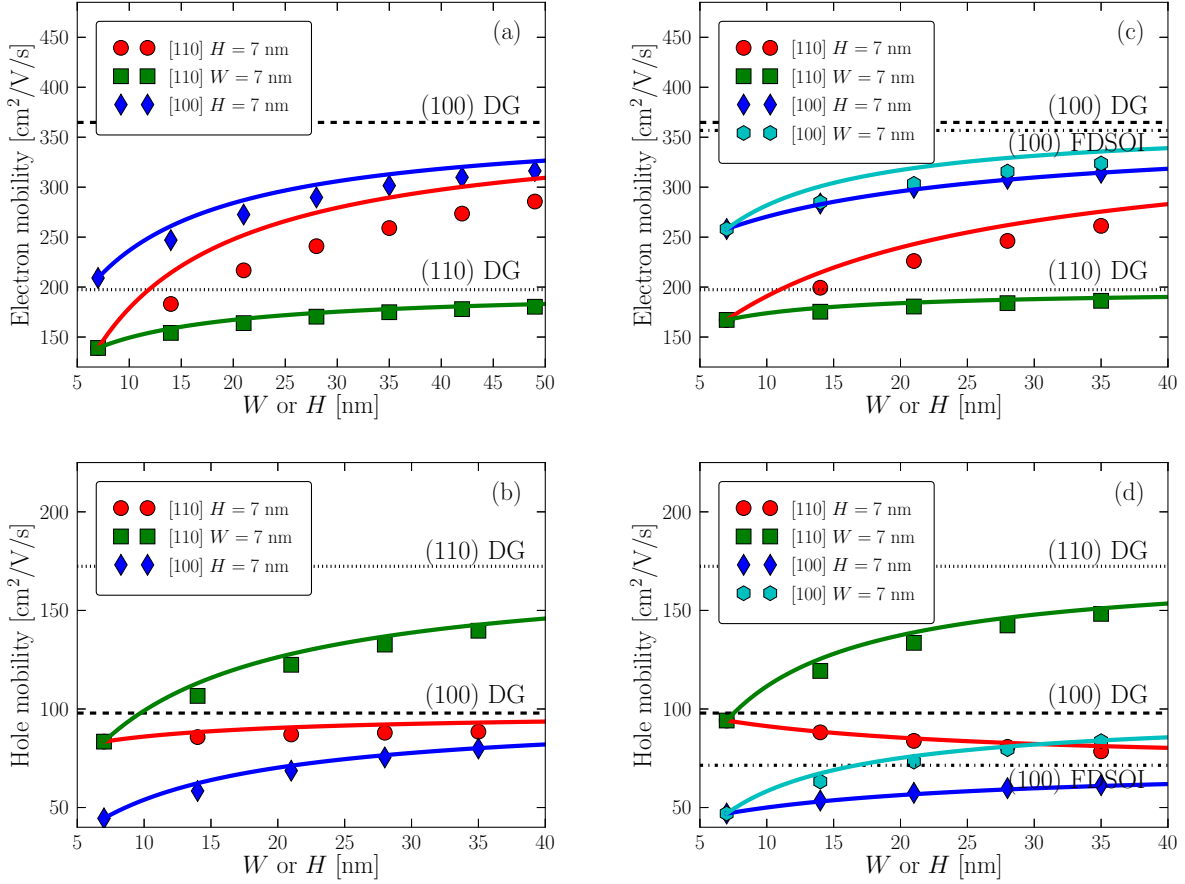


Fig. 1. Phonon+SR electron (a, c) and hole (b, d) mobilities in rectangular [100] and [110] GAA (a, b) and Trigate (c, d) SiNW devices as a function of width (W) or height (H) at carrier density $n = 10^{13} \text{ cm}^{-2}$. The symbols are the NEGF results. The horizontal dashed lines, dash-dotted lines and dotted lines are the reference NEGF mobilities in planar (100) DG, (100) FDSOI and (110) DG devices, respectively. The solid lines are the interpolations from square NW devices to the limiting planar devices using Eqs. (2)–(3).

the 3 f -type and the 3 g -type processes of Ref. [33]. We use a diagonal hole-phonon interaction with one single acoustic deformation potential $D_{\text{ac}} = 16.5 \text{ eV}$ and one single optical deformation potential $DK_{\text{opt}} = 15 \text{ eV/\AA}$ [34]. Details about the NEGF implementation can be found in Ref. [32].

The carrier mobility is calculated with two different methods. First, the quasi-Fermi level profile can be reconstructed from the NEGF data, and the mobility extracted from the slope of the quasi-Fermi level in the channel [35]. Second, the mobility can be computed from the slope of the total resistance R of the device with respect to the channel length L (numerical transmission line method) [32]. This method is more accurate but more demanding than the quasi-Fermi level analysis, since the calculation must be repeated on long devices. The device-to-device variability is small for SR but is significant once RCS is included [32]. We choose the distributions of RCS charges according to Ref. [32] in order to reduce that variability. Moreover, the mobilities are averaged over 5 distributions of RCS charges (but a single SR profile). In the following, the carrier densities per unit area are normalized with respect to the perimeter W_{eff} of the SiNWs ($W_{\text{eff}} = 2W + 2H$ for GAA and $W_{\text{eff}} = W + 2H$ for Trigate devices).

III. RESULTS AND DISCUSSION

A. Size dependence of the carrier mobilities

In this section, we analyze the dependence of the electron and hole mobilities in rectangular GAA and Trigate SiNWs on width W , height H , and orientation. For that purpose, we have computed the phonon+SR mobility in devices with one fixed dimension W or $H = 7 \text{ nm}$, and the other dimension ranging from 7 to 49 nm. The surface roughness rms is $\Delta_{\text{SR}} = 0.45 \text{ nm}$. We have also computed the mobility for the planar limits: in GAA SiNWs, W or $H \rightarrow \infty$ corresponds to a double-gate (DG) device. In Trigate SiNWs, $H \rightarrow \infty$ also corresponds to a DG device while $W \rightarrow \infty$ corresponds to a planar fully-depleted SOI (FDSOI) device. The electron and hole band structures are described with the EMA and three bands $\mathbf{k} \cdot \mathbf{p}$ models, respectively, and the wave function can not penetrate into the oxide. The mobility has been extracted from a quasi-Fermi level analysis in 30 nm long channels.

The results are shown in Fig. 1 (symbols). For electrons, we find that (i) [100] n -NWFETs perform better than [110] n -NWFETs, and (ii) [110] n -NWFETs with width $W > H$ show larger mobilities than [110] n -NWFETs with height $H > W$. This holds for both GAA and Trigate devices. This can be

TABLE I
PARAMETERS α (cm²), β (cm⁴) AND γ_{RCS} [SEE EQS. (5) AND (6)] FOR THE PH, SR AND RCS ELECTRON AND HOLE MOBILITIES IN [100] AND [110] SQUARE GAA SiNW AND DOUBLE GATE (DG) DEVICES. μ^0 (cm²/V/s) IS THE NEGF MOBILITY AT CARRIER DENSITY $n_0 = 2 \times 10^{12}$ cm⁻².

		Thickness (nm)	μ_{PH}^0	α_{PH}	β_{PH}	μ_{SR}^0	α_{SR}	β_{SR}	μ_{RCS}^0	γ_{RCS}	
Square Gate-all-around	Electrons [100]	5	372	2.73×10^{-14}	-2.38×10^{-28}	953	-1.09×10^{-14}	3.21×10^{-26}	281	1.19	
		7	476	1.38×10^{-14}	2.90×10^{-27}	1680	1.28×10^{-13}	4.45×10^{-26}	463	0.77	
		10	509	6.34×10^{-14}	1.98×10^{-28}	2200	2.07×10^{-12}	6.05×10^{-26}	491	0.79	
	Holes [100]	5	68	-2.63×10^{-14}	1.87×10^{-27}	102	7.24×10^{-14}	2.45×10^{-27}	203	1.38	
		7	88	7.42×10^{-16}	1.85×10^{-27}	304	2.44×10^{-13}	1.15×10^{-27}	458	0.76	
		10	100	3.58×10^{-15}	1.18×10^{-27}	749	2.88×10^{-13}	3.69×10^{-26}	506	0.63	
	Electrons [110]	5	417	1.83×10^{-14}	1.09×10^{-27}	648	9.29×10^{-14}	2.03×10^{-26}	317	1.08	
		7	459	4.62×10^{-14}	2.44×10^{-28}	1240	2.29×10^{-13}	5.29×10^{-26}	486	0.70	
		10	452	4.48×10^{-14}	-4.74×10^{-28}	1620	1.52×10^{-12}	6.08×10^{-26}	474	0.79	
	Holes [110]	5	216	-2.51×10^{-16}	3.85×10^{-27}	336	2.77×10^{-13}	1.32×10^{-26}	310	1.06	
		7	213	-5.82×10^{-16}	3.06×10^{-27}	451	2.33×10^{-13}	5.29×10^{-27}	425	0.82	
		10	205	-4.44×10^{-14}	5.22×10^{-27}	682	2.65×10^{-13}	3.31×10^{-26}	585	0.57	
	Double Gate	Electrons (100)	5	517	3.90×10^{-14}	-6.27×10^{-28}	2360	2.42×10^{-13}	9.56×10^{-27}	547	0.88
			7	556	1.77×10^{-14}	8.94×10^{-28}	3610	2.37×10^{-13}	4.43×10^{-26}	676	0.77
			10	577	3.36×10^{-14}	4.98×10^{-28}	4250	1.20×10^{-12}	1.24×10^{-25}	736	0.68
Holes (100)		5	115	-1.63×10^{-14}	9.53×10^{-28}	396	1.45×10^{-15}	9.17×10^{-27}	85	1.79	
		7	130	-1.69×10^{-14}	1.15×10^{-27}	957	1.10×10^{-13}	3.49×10^{-26}	158	1.49	
		10	146	-2.51×10^{-14}	3.59×10^{-27}	1400	4.65×10^{-13}	7.23×10^{-26}	302	0.98	
Electrons (110)		5	378	-1.3×10^{-14}	1.4×10^{-27}	1130	-3.7×10^{-15}	1.1×10^{-26}	524	1.06	
		7	436	1.6×10^{-14}	1.3×10^{-27}	2610	1.7×10^{-13}	4.9×10^{-26}	677	0.72	
		10	441	4.6×10^{-14}	-8.3×10^{-28}	3150	1.4×10^{-12}	1.9×10^{-25}	728	0.66	
Holes (110)		5	337	2.80×10^{-15}	1.92×10^{-27}	1180	3.86×10^{-13}	-2.01×10^{-27}	158	1.47	
		7	315	-2.60×10^{-14}	3.22×10^{-27}	1530	5.62×10^{-13}	6.88×10^{-27}	216	1.22	
		10	302	-3.95×10^{-14}	3.92×10^{-27}	1650	1.25×10^{-12}	-3.64×10^{-27}	271	1.02	

explained by band structure effects [21]–[25]. In [100] SiNWs, the Δ valleys split into light ($m^* = 0.19 m_0$) $\Delta_{y,z}$ valleys at the Γ point, and much heavier ($m^* = 0.92 m_0$) Δ_x valleys at $k \neq 0$. In the strong inversion regime, the electron gas is confined at the surface of the SiNW by the electric field, mostly in the light Δ_y valleys on the lateral (010) facets, and mostly in the light Δ_z valleys on the top and bottom (001) facets. In [110] SiNWs, the Δ valleys split into light ($m^* = 0.19 m_0$) Δ_z valleys at Γ and heavier ($m^* = 0.55 m_0$) $\Delta_{x,y}$ valley off Γ . Again, in the strong inversion regime the electron gas is mostly confined in the light Δ_z valleys on the top and bottom (001) facets, but in the heavier $\Delta_{x,y}$ valleys on the lateral (1 $\bar{1}$ 0) facets. Therefore, wide [110] SiNWs with dominant (001) facets ($W > H$) perform better than tall [110] SiNWs with dominant (1 $\bar{1}$ 0) facets ($W < H$). Likewise, [100] NWs with only {001} facets show better mobilities than [110] SiNWs with mixed facets.

The trends are opposite for p -NWFETs. Tall [110] SiNWs ($H > W$) indeed perform better than wide [110] SiNWs ($W > H$), and [110] always outperform [100] p -NWFETs. These trends can again be understood with band structure arguments [23]–[28]. Indeed, holes confined on {110} facets tend to show lighter transport masses than holes confined on {001} facets [36]. In strongly confined square [110] SiNWs, the highest valence subbands have a clear light hole character and are well separated from the others, while in square [100] SiNWs, the topmost valence bands are almost degenerate and heavy, which decreases carrier velocity and enhances inter-subband scattering [24].

We find that the carrier mobility generally increases with increasing NW cross section. The only exception is [110] p -type Trigate NWFETs with $W > H$ [28], since the increase of the (100) facet area with lower hole mobility is detrimental.

When increasing W or H , the carrier mobility tends to the expected DG or FDSOI limit. However, the convergence can be slow, especially for electrons in [110] SiNWs with $W > H$. W and H play the same role in [100] GAA devices as (010) and (001) facets are equivalent. This is not the case, however, in [100] Trigate devices as the side and top/bottom facets are not equivalent any more: the [100] Trigates with $H \gg W$ actually perform better than the [100] Trigates with $W \gg H$. This is particularly evident for p -NWFETs. As a matter of fact, the limiting (100) DG devices show better mobilities than the limiting (100) FDSOI devices because the carriers are distributed slightly more homogeneously over the thickness of the film [37].

B. A simple interpolation model

In order to model these trends, we have analyzed the carrier density in the channel. We focus on n -type GAA devices, but the same arguments hold for Trigates. As shown in Fig. 2a, the density in the moderate to strong inversion regime peaks in four “corner channels” that tend to merge in two “side channels” when the size of the small facets is in the sub-10 nm range [8]. The electron and hole mobility can then be written:

$$\mu = \frac{n_{\text{in}}}{n_{\text{in}} + n_{\text{side}}} \mu_{\text{DG}} + \frac{n_{\text{side}}}{n_{\text{in}} + n_{\text{side}}} \mu_{\text{side}}, \quad (1)$$

where n_{in} and n_{side} are the charge densities per unit length in the inner region and side channels of Fig. 2a, and μ_{DG} is the mobility in the limiting DG device. The mobility μ_{side} in the side channels can be extracted from the NEGF data at a given size. We set $T = 3.5$ nm for the thickness of the side channels, which gives a reasonable partition of the carrier density in the $n = 2 \times 10^{12} - 10^{13}$ cm⁻² range. μ_{side} is plotted in Fig. 2b

TABLE II
SAME AS TABLE I BUT FOR SQUARE TRIGATE SiNW DEVICES AND (100) FDSOI DEVICES.

		Thickness (nm)	μ_{PH}^0	α_{PH}	β_{PH}	μ_{SR}^0	α_{SR}	β_{SR}	μ_{RCS}^0	γ_{RCS}
Square Trigate	Electrons [100]	5	378	2.90×10^{-14}	-6.58×10^{-28}	1000	3.60×10^{-14}	2.45×10^{-26}	330	0.99
		7	482	1.14×10^{-14}	1.93×10^{-27}	1860	2.26×10^{-13}	3.10×10^{-26}	493	0.72
		10	514	5.17×10^{-14}	3.21×10^{-28}	2390	2.49×10^{-12}	2.43×10^{-26}	559	0.65
	Holes [100]	5	67	-1.95×10^{-14}	1.18×10^{-27}	107	5.17×10^{-14}	2.72×10^{-27}	118	1.17
		7	87	-6.82×10^{-15}	2.37×10^{-27}	356	3.04×10^{-13}	-1.60×10^{-27}	159	0.84
		10	98	1.86×10^{-14}	2.53×10^{-28}	853	1.55×10^{-12}	-2.28×10^{-26}	309	0.69
	Electrons [110]	5	425	1.46×10^{-14}	8.94×10^{-28}	703	9.66×10^{-14}	1.56×10^{-26}	411	0.91
		7	467	4.13×10^{-14}	9.01×10^{-29}	1450	2.66×10^{-13}	4.86×10^{-26}	465	0.73
		10	452	4.11×10^{-14}	-6.86×10^{-28}	1800	1.70×10^{-12}	3.66×10^{-26}	589	0.61
	Holes [110]	5	219	-3.85×10^{-16}	2.54×10^{-27}	369	2.19×10^{-13}	1.21×10^{-26}	186	0.97
		7	211	-3.59×10^{-14}	5.12×10^{-27}	501	3.28×10^{-13}	-5.23×10^{-27}	207	0.94
		10	205	-3.24×10^{-14}	3.38×10^{-27}	722	3.73×10^{-13}	1.52×10^{-26}	229	0.85
FDSOI	Electrons (100)	5	532	2.83×10^{-14}	5.69×10^{-28}	2180	4.74×10^{-14}	4.29×10^{-26}	628	0.77
		7	554	2.33×10^{-14}	9.76×10^{-28}	2940	2.45×10^{-13}	6.50×10^{-26}	750	0.67
		10	570	3.43×10^{-14}	3.12×10^{-28}	3460	3.42×10^{-13}	1.00×10^{-25}	852	0.59
	Holes (100)	5	116	-3.65×10^{-17}	1.15×10^{-27}	366	-1.21×10^{-14}	1.76×10^{-26}	151	1.32
		7	128	1.54×10^{-14}	4.24×10^{-28}	895	3.28×10^{-16}	6.57×10^{-26}	221	1.05
		10	136	3.45×10^{-14}	-8.32×10^{-28}	1300	1.27×10^{-13}	1.43×10^{-25}	309	0.84

for [110] GAA SiNW devices. It is, as expected, smaller on $(\bar{1}\bar{1}0)$ than on (001) facets. It is also smaller than in DG (or FDSOI) devices due to lateral quantum confinement in the side channel, which enhances SR and phonon scattering. μ_{side} is, therefore, dependent on the thickness of the Si channel, which is not accounted for in the simplest facet model [8], [11]. Eq. (1) with the data of Fig. 2b provides a fair description of the mobility for all sizes and carrier densities. n_{in} increases linearly with W or H , while n_{side} remains nearly constant. However, over 20% of the total charge remains located in the side channels with much lower mobility even when W or $H \simeq 50$ nm. This explains the slow convergence of the mobility towards the planar limit.

We can further simplify the model if we assume that the charge in both the inner and side channels is ruled by simple electrostatics and is thus proportional to the inner/side perimeters, e.g. $n_{\text{in}} \simeq \alpha(W - 2T)$ and $n_{\text{side}} \simeq \alpha(H + 2T)$ when $W > H$. Then Eq. (1) turns into a simple interpolation formula between the mobility μ_{SQ} of the square NW ($H = W$) and the mobility of the limiting DG device μ_{DG} , namely:

$$\mu \approx \frac{W - H}{W + H} \mu_{\text{DG}} + \frac{2H}{W + H} \mu_{\text{SQ}} \quad (2a)$$

when $W > H$, and:

$$\mu \approx \frac{H - W}{W + H} \mu_{\text{DG}} + \frac{2W}{W + H} \mu_{\text{SQ}} \quad (2b)$$

when $W < H$. For Trigate devices, the interpolation formula is:

$$\mu \approx \frac{W - H}{W + 2H} \mu_{\text{FDSOI}} + \frac{3H}{W + 2H} \mu_{\text{SQ}} \quad (3a)$$

when $W > H$, and:

$$\mu \approx 2 \frac{H - W}{W + 2H} \mu_{\text{DG}} + \frac{3W}{W + 2H} \mu_{\text{SQ}}. \quad (3b)$$

when $W < H$. In Eqs. (3), μ_{FDSOI} is the mobility of the limiting FDSOI device, and μ_{SQ} the mobility of the square Trigate device. These equations reproduce the NEGF results very well over a wide range of dimensions and carrier densities, as shown in Figs. 1 and 2c. The discrepancies

between this model and the NEGF data are maximal for [110] GAA n -NWFETs with $W > H$.

C. Carrier mobilities in square nanowires and thin films

Eqs. (2) and (3) use the carrier mobilities of the square NW devices (μ_{SQ}) and of the limiting thin film devices (μ_{DG} and μ_{FDSOI}) as inputs. These mobilities are limited by phonons, SR and RCS. In order to deconvolve the different contributions in the experimental data, we have computed the PH, SR and RCS mobilities in n -type and p -type, square Trigate and GAA SiNW devices with various sizes ($W = H = 5, 7, 10$ nm), and in the corresponding DG and FDSOI devices. The SR and RCS mobilities are defined with respect to the phonon-limited mobility μ_{PH} as

$$\mu_{\text{M}}^{-1} = \mu_{\text{PH+M}}^{-1} - \mu_{\text{PH}}^{-1}, \quad (4)$$

where M is a given elastic mechanism (SR or RCS), and $\mu_{\text{PH+M}}$ is the NEGF mobility computed with phonons and that scattering mechanism. Including phonons in each calculation limits wave interferences and localization, and the partial mobilities defined above satisfy Matthiessen's rule for multiple mechanisms better than the usual, direct single mechanism calculations [32]. We report data for a reference SR rms $\Delta_{\text{SR}}^{\text{ref}} = 0.45$ nm and correlation length $\Lambda_{\text{SR}}^{\text{ref}} = 1$ nm, and for a reference density of RCS charges $n_{\text{RCS}}^{\text{ref}} = 2 \times 10^{13}$ cm $^{-2}$. It is well known that the EMA tends to overestimate the electron mobility though it is computationally less demanding. In what follows, we have therefore employed a two bands $\mathbf{k} \cdot \mathbf{p}$ model for the electrons in order to provide more accurate results for comparison with experiment. The wave function is also allowed to penetrate into the oxide layer. The carrier mobilities are extracted with the transmission line method.

The phonon mobility μ_{PH} and the SR mobility μ_{SR} decrease, in general, as a function of carrier density. SR scattering is, however, dominant at high inversion density, as the carriers get confined to the Si/SiO $_2$ interface by the electric field. μ_{PH} and μ_{SR} also tend to decrease when the cross sectional area of the SiNW is reduced (except notably for [110])

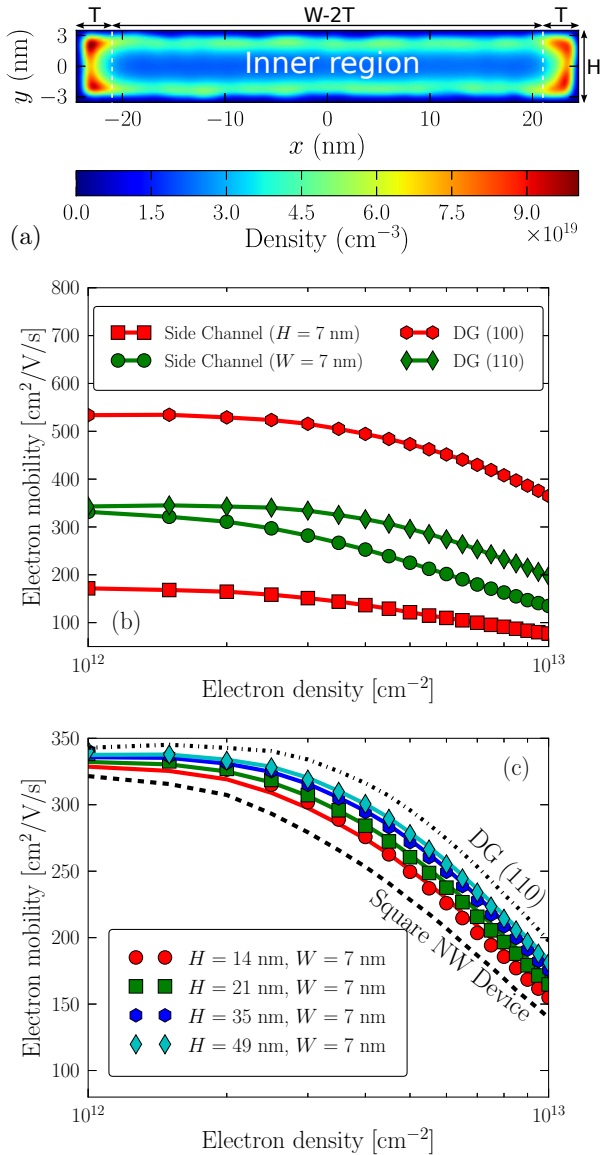


Fig. 2. (a) Map of the electron density in a rectangular [100] GAA device with $W = 49$ nm and $H = 7$ nm, at carrier density $n = 9.75 \times 10^{12}$ cm $^{-2}$. The charge can be split into two contributions, one from the “side channels” with thickness T , and one from the inner region with width $W - 2T$. (b) Phonon+SR electron mobility in the “side channels” of [110] GAA SiNWs with $W = 7$ nm or $H = 7$ nm (extracted from the $W = 7$ nm \times $H = 14$ nm and $W = 14$ nm \times $H = 7$ nm devices of Fig. 1, respectively, using $T = 3.5$ nm). The mobilities computed in 7 nm-thick (100) and (110) DG devices are also plotted. (c) Phonon+SR electron mobility in [110] GAA SiNWs with $W = 7$ nm as a function of carrier density for different H . The solid lines are the interpolations with Eq. (2b), while the symbols, dashed and dash-dotted lines are the raw NEGF mobilities.

p -NWFETs [38]). Structural confinement indeed enhances the interactions with phonons and with surface roughness on all facets. For practical purposes, μ_{PH} and μ_{SR} can be modeled empirically with the following function for carrier densities n in the $10^{12} - 10^{13}$ cm $^{-2}$ range:

$$\mu_{\text{M}} = \mu_{\text{M}}^0 \frac{1 + \alpha_{\text{M}} n_0 + \beta_{\text{M}} n_0^2}{1 + \alpha_{\text{M}} n + \beta_{\text{M}} n^2}, \quad (5)$$

where “M” is either “PH” or “SR”, μ_{M}^0 is the “M”-limited mobility at a reference carrier density $n_0 = 2 \times 10^{12}$ cm $^{-2}$,

and $\alpha_{\text{M}}, \beta_{\text{M}}$ are fitting parameters. The values of $\mu_{\text{M}}^0, \alpha_{\text{M}}$ and β_{M} are reported in Tables I and II for all considered devices.

RCS is known to be a very important scattering mechanism at low inversion density [39], [40]. It is, however, efficiently screened by the electron gas at large carrier density. It can be modeled by the following function:

$$\mu_{\text{RCS}} = \mu_{\text{RCS}}^0 (n/n_0)^{\gamma_{\text{RCS}}}, \quad (6)$$

where μ_{RCS}^0 is the RCS mobility at carrier density n_0 , and γ_{RCS} is an exponent that characterizes screening.

The total mobility μ can be reconstructed from the partial PH, SR and RCS mobilities with Matthiessen’s rule. Since $\mu_{\text{SR}} \propto 1/\Delta_{\text{SR}}^2$ [31], [32] and $\mu_{\text{RCS}} \propto 1/n_{\text{RCS}}$ [39], [40], μ can be written for arbitrary Δ_{SR} and n_{RCS} [34]:

$$\frac{1}{\mu} = \frac{1}{\mu_{\text{PH}}} + \left(\frac{\Delta_{\text{SR}}}{\Delta_{\text{SR}}^{\text{ref}}} \right)^2 \frac{1}{\mu_{\text{SR}}^{\text{ref}}} + \frac{n_{\text{RCS}}}{n_{\text{RCS}}^{\text{ref}}} \frac{1}{\mu_{\text{RCS}}^{\text{ref}}}, \quad (7)$$

where $\mu_{\text{SR}}^{\text{ref}}$ is the SR mobility computed with $\Delta_{\text{SR}}^{\text{ref}} = 0.45$ nm, and $\mu_{\text{RCS}}^{\text{ref}}$ is the RCS mobility computed with $n_{\text{RCS}}^{\text{ref}} = 2 \times 10^{13}$ cm $^{-2}$ (Tables I and II). It should be noted that μ_{SR} also depends on the correlation length Λ_{SR} . However, different $(\Delta_{\text{SR}}, \Lambda_{\text{SR}})$ pairs can yield similar mobilities [41], so that Δ_{SR} and Λ_{SR} can hardly be adjusted independently. Therefore, we use Δ_{SR} as the only parameter. Likewise, μ_{RCS} has a strong exponential dependence on the thickness of the interfacial layer of SiO $_2$ [39], [40]; Δ_{SR} and n_{RCS} shall therefore be regarded as “effective” parameters, especially if the gate stack differs significantly from the present design. From a practical point of view, Δ_{SR} and n_{RCS} can be adjusted on the experimental mobilities measured on a few test devices, then Eqs. (2), (3) and (7) used to interpolate/extrapolate the mobilities for arbitrary rectangular nanowires.

IV. COMPARISON WITH EXPERIMENTAL DATA

As an illustration, we compare the calculated mobilities with experimental data on rectangular Trigate devices with height $H = 11$ nm fabricated at CEA/LETI [42]. The equivalent oxide thickness (EOT) of the high- k /metal gate stack is approximately 1.3 nm. The parameters Δ_{SR} and n_{RCS} in Eq. (7) have been adjusted in order to reproduce the dependence of the experimental mobility on carrier density for the n -type [110] square Trigate device and for the n -type, 11 nm thick FDSOI device. In this procedure, we have used the partial mobilities computed for the 10 nm square Trigate and FDSOI thin film. The optimal values are $\Delta_{\text{SR}} = 0.43$ nm and $n_{\text{RCS}} = 1.42 \times 10^{13}$ cm $^{-2}$.

The mobility can then be computed for arbitrary n - and p -type devices with Eq. (3a) and Tables I and II. The experimental and calculated mobilities are plotted as a function of W in Fig. 3, at carrier density $n = 10^{13}$ cm $^{-2}$. The agreement is not perfect, but there is some experimental variability for the smallest W ’s. We point out that we are not only able to reproduce the mobility of the target [110] n -type Trigates, but also the mobility of the [100] n -type Trigates and, more importantly, of all p -type devices (which were not included in the optimization of Δ_{SR} and n_{RCS}). A two parameters model for the mobility, Eq. (7), and the interpolation formula,

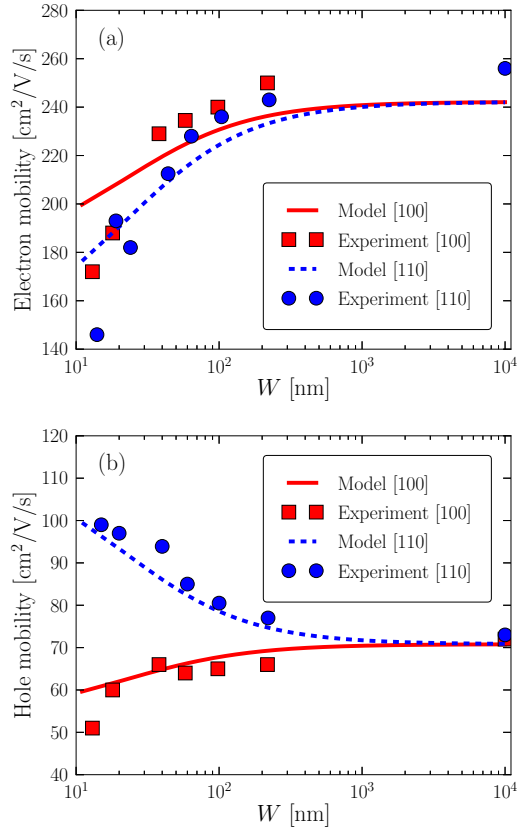


Fig. 3. (a) Electron and (b) hole mobilities as a function of W in rectangular Trigate devices ($H = 11$ nm), at carrier density $n = 10^{13}$ cm $^{-2}$. The symbols are the experimental data, while the solid and dashed lines are the mobilities interpolated from Eqs. (3a), (7) and Table II ($\Delta_{SR} = 0.43$ nm, $n_{RCS} = 1.42 \times 10^{13}$ cm $^{-2}$).

Eq. (3a), can hence describe the experimental trends whatever the SiNW orientation and nature of the carriers. The above equations can, therefore, be used to explore the performances of next generation FinFETs or stacked SiNWs devices.

V. CONCLUSIONS

We have performed quantum calculations of the carrier mobilities in n -type and p -type, gate-all-around and Trigate SiNW devices using a non equilibrium Green's Functions approach. The mobility tends to the planar double gate or FDSOI limit when the nanowire width or height is increased. However, the convergence can be rather slow. This results from the formation of "side channels" with low mobility. Their contribution remains significant even in rectangular devices with large width or height up to 50 nm.

We have derived from the numerical results a simple but effective interpolation model for the size dependent carrier mobilities in rectangular SiNW devices. The inputs of this model are the mobilities of the square SiNW devices and of the limiting thin film devices. These mobilities can be reconstructed from the contributions of the main scattering mechanisms using Matthiessen's rule. We have therefore computed the phonons, SR and RCS mobilities of square SiNW devices and thin films with various sizes in the sub-10 nm

range, and have given simple analytical expressions for practical usage. Finally, we have successfully validated these models against experimental data on Trigate devices. The results shall be useful for compact modeling and optimization of SiNW devices such as FinFETs and stacked nanowire transistors.

REFERENCES

- [1] J.-P. Colinge, *FinFETs and Other Multi-Gate Transistors*. Springer US, 2008.
- [2] M. C. McAlpine, R. S. Friedman, S. Jin, K.-h. Lin, W. U. Wang, and C. M. Lieber, "High-Performance Nanowire Electronics and Photonics on Glass and Plastic Substrates," *Nano Lett.*, vol. 3, no. 11, pp. 1531–1535, 2003.
- [3] J. Goldberger, A. I. Hochbaum, R. Fan, and P. Yang, "Silicon Vertically Integrated Nanowire Field Effect Transistors," *Nano Lett.*, vol. 6, no. 5, pp. 973–977, 2006.
- [4] X. Liu, Y.-Z. Long, L. Liao, X. Duan, and Z. Fan, "Large-Scale Integration of Semiconductor Nanowires for High-Performance Flexible Electronics," *ACS Nano*, vol. 6, no. 3, pp. 1888–1900, 2012.
- [5] O. Gunawan, L. Sekaric, A. Majumdar, M. Rooks, J. Appenzeller, J. W. Sleight, S. Guha, and W. Haensch, "Measurement of Carrier Mobility in Silicon Nanowires," *Nano Lett.*, vol. 8, no. 6, pp. 1566–1571, 2008.
- [6] J. Chen, T. Saraya, K. Miyaji, K. Shimizu, and T. Hiramoto, "Electron Mobility in Silicon Gate-All-Around [100]- and [110]-Directed Nanowire MetalOxideSemiconductor Field-Effect Transistor on (100)-Oriented Silicon-on-Insulator Substrate Extracted by Improved Split Capacitance Voltage Method," *Jpn. J. Appl. Phys.*, vol. 48, no. 1R, p. 011205, 2009.
- [7] J. Chen, T. Saraya, and T. Hiramoto, "Experimental Investigations of Electron Mobility in Silicon Nanowire nMOSFETs on (110) Silicon-on-Insulator," *IEEE Electron Device Lett.*, vol. 30, no. 11, pp. 1203–1205, 2009.
- [8] L. Sekaric, O. Gunawan, A. Majumdar, X. H. Liu, D. Weinstein, and J. W. Sleight, "Size-dependent modulation of carrier mobility in top-down fabricated silicon nanowires," *Appl. Phys. Lett.*, vol. 95, no. 2, p. 023113, 2009.
- [9] P. Hashemi, J. T. Teherani, and J. L. Hoyt, "Investigation of hole mobility in gate-all-around Si nanowire p-MOSFETs with high-k/metal-gate: Effects of hydrogen thermal annealing and nanowire shape," in *IEDM Tech. Dig.*, 2010, pp. 34.5.1–34.5.4.
- [10] K. Mao, T. Saraya, and T. Hiramoto, "Effects of Side Surface Roughness on Carrier Mobility in Tri-Gate Single Silicon Nanowire MetalOxideSemiconductor Field-Effect Transistors," *Jpn. J. Appl. Phys.*, vol. 52, no. 4S, p. 04CC11, 2013.
- [11] R. Coquand, S. Barraud, M. Cass, P. Leroux, C. Vizioz, C. Comboroure, P. Perreau, E. Ernst, M.-P. Samson, V. Maffini-Alvaro, C. Tabone, S. Barnola, D. Munteanu, G. Ghibaudo, S. Monfray, F. Boeuf, and T. Poiroux, "Scaling of high-/metal-gate TriGate SOI nanowire transistors down to 10 nm width," *Solid-State Electronics*, vol. 88, pp. 32–36, 2013.
- [12] S. Jin, M. V. Fischetti, and T.-w. Tang, "Modeling of electron mobility in gated silicon nanowires at room temperature: Surface roughness scattering, dielectric screening, and band nonparabolicity," *J. Appl. Phys.*, vol. 102, no. 8, p. 083715, 2007.
- [13] M. Lenzi, A. Gnudi, S. Reggiani, E. Gnani, M. Rudan, and G. Bacarani, "Semiclassical transport in silicon nanowire FETs including surface roughness," *J. Comput. Electronics*, vol. 7, no. 3, pp. 355–358, 2008.
- [14] E. B. Ramayya, D. Vasileska, S. M. Goodnick, and I. Knezevic, "Electron transport in silicon nanowires: The role of acoustic phonon confinement and surface roughness scattering," *J. Appl. Phys.*, vol. 104, no. 6, p. 063711, 2008.
- [15] A. Cresti, M. G. Pala, S. Poli, M. Mouis, and G. Ghibaudo, "A Comparative Study of Surface-Roughness-Induced Variability in Silicon Nanowire and Double-Gate FETs," *IEEE Transactions on Electron Devices*, vol. 58, no. 8, pp. 2274–2281, 2011.
- [16] S. Kim, M. Luisier, A. Paul, T. B. Boykin, and G. Klimeck, "Full Three-Dimensional Quantum Transport Simulation of Atomistic Interface Roughness in Silicon Nanowire FETs," *IEEE Trans. Electron Devices*, vol. 58, no. 5, pp. 1371–1380, 2011.
- [17] M. Aldegunde, A. Martinez, and J. R. Barker, "Study of individual phonon scattering mechanisms and the validity of Matthiessen's rule in a gate-all-around silicon nanowire transistor," *J. Appl. Phys.*, vol. 113, no. 1, p. 014501, 2013.

- [18] H. E. Jung and M. Shin, "Surface-Roughness-Limited Mean Free Path in Silicon Nanowire Field Effect Transistors," *IEEE Trans. Electron Devices*, vol. 60, no. 6, pp. 1861–1866, 2013.
- [19] R. Rhyner and M. Luisier, "Atomistic modeling of coupled electron-phonon transport in nanowire transistors," *Phys. Rev. B*, vol. 89, p. 235311, Jun 2014.
- [20] H. Ryu, "A multi-subband Monte Carlo study on dominance of scattering mechanisms over carrier transport in sub-10-nm Si nanowire FETs," *Nanoscale Res. Lett.*, vol. 11, no. 1, pp. 1–9, 2016.
- [21] I. M. Tienda-Luna, F. G. Ruiz, A. Godoy, B. Biel, and F. Gmiz, "Surface roughness scattering model for arbitrarily oriented silicon nanowires," *J. Appl. Phys.*, vol. 110, no. 8, p. 084514, 2011.
- [22] R. Granzner, V. M. Polyakov, C. Schippel, and F. Schwierz, "Empirical Model for the Effective Electron Mobility in Silicon Nanowires," *IEEE Trans. Electron Devices*, vol. 61, no. 11, pp. 3601–3607, 2014.
- [23] A. K. Buin, A. Verma, and M. P. Anantram, "Carrier-phonon interaction in small cross-sectional silicon nanowires," *J. Appl. Phys.*, vol. 104, no. 5, p. 053716, 2008.
- [24] Y. M. Niquet, C. Delerue, D. Rideau, and B. Videau, "Fully Atomistic Simulations of Phonon-Limited Mobility of Electrons and Holes in $\langle 001 \rangle$ -, $\langle 110 \rangle$ -, and $\langle 111 \rangle$ -Oriented Si Nanowires," *IEEE Trans. Electron Devices*, vol. 59, no. 5, pp. 1480–1487, 2012.
- [25] Y.-M. Niquet, C. Delerue, and C. Krzeminski, "Effects of Strain on the Carrier Mobility in Silicon Nanowires," *Nano Letters*, vol. 12, no. 7, pp. 3545–3550, 2012.
- [26] M. D. Michielis, D. Esseni, P. Palestri, and L. Selmi, "Semiclassical Modeling of Quasi-Ballistic Hole Transport in Nanoscale pMOSFETs Based on a Multi-Subband Monte Carlo Approach," *IEEE Trans. Electron Devices*, vol. 56, no. 9, pp. 2081–2091, 2009.
- [27] N. Neophytou, O. Baumgartner, Z. Stanojevic, and H. Kosina, "Band structure and mobility variations in p-type silicon nanowires under electrostatic gate field," *Solid-State Electronics*, vol. 90, pp. 44 – 50, 2013.
- [28] N. Neophytou and H. Kosina, "Hole mobility increase in ultra-narrow si channels under strong (110) surface confinement," *Appl. Phys. Lett.*, vol. 99, no. 9, p. 092110, 2011.
- [29] R. Kotlyar, T. D. Linton, R. Rios, M. D. Giles, S. M. Cea, K. J. Kuhn, M. Povolotskyi, T. Kubis, and G. Klimeck, "Does the low hole transport mass in 110 and 111 Si nanowires lead to mobility enhancements at high field and stress: A self-consistent tight-binding study," *J. Appl. Phys.*, vol. 111, no. 12, p. 123718, 2012.
- [30] M. P. Anantram, M. S. Lundstrom, and D. E. Nikonov, "Modeling of nanoscale devices," *Proceedings of the IEEE*, vol. 96, pp. 1511–1550, 2008.
- [31] S. M. Goodnick, D. K. Ferry, C. W. Wilmsen, Z. Liliental, D. Fathy, and O. L. Krivanek, "Surface roughness at the Si(100)-SiO₂ interface," *Phys. Rev. B*, vol. 32, pp. 8171–8186, 1985.
- [32] Y.-M. Niquet, V.-H. Nguyen, F. Triozon, I. Duchemin, O. Nier, and D. Rideau, "Quantum calculations of the carrier mobility: Methodology, Matthiessen's rule, and comparison with semi-classical approaches," *J. Appl. Phys.*, vol. 115, no. 5, p. 054512, 2014.
- [33] C. Jacoboni and L. Reggiani, "The Monte Carlo method for the solution of charge transport in semiconductors with applications to covalent materials," *Rev. Mod. Phys.*, vol. 55, pp. 645–705, Jul 1983.
- [34] V. H. Nguyen, Y. M. Niquet, F. Triozon, I. Duchemin, O. Nier, and D. Rideau, "Quantum Modeling of the Carrier Mobility in FDSOI Devices," *IEEE Trans. Electron Devices*, vol. 61, no. 9, pp. 3096–3102, 2014.
- [35] L. Bourdet, J. Li, J. Pelloux-Prayer, F. Triozon, M. Casse, S. Barraud, S. Martinie, D. Rideau, and Y.-M. Niquet, "Contact resistances in trigate and FinFET devices in a non-equilibrium Green's functions approach," *J. Appl. Phys.*, vol. 119, no. 8, p. 084503, 2016.
- [36] P. Packan, S. Cea, H. Deshpande, T. Ghani, M. Giles, O. Golonzka, M. Hattendorf, R. Kotlyar, K. Kuhn, A. Murthy, P. Ranade, L. Shifren, C. Weber, and K. Zawadzki, "High performance Hi-K + metal gate strain enhanced transistors on (110) silicon," in *2008 IEEE International Electron Devices Meeting*, 2008, pp. 1–4.
- [37] F. Gamiz and M. V. Fischetti, "Monte Carlo simulation of double-gate silicon-on-insulator inversion layers: The role of volume inversion," *Journal of Applied Physics*, vol. 89, no. 10, pp. 5478–5487, 2001.
- [38] Strong confinement indeed promotes light hole bands in [110] p-NWFETs. The increase of hole velocities can overcome the enhancement of scattering. Therefore, the mobility might be non monotonous with carrier density and/or NW size depending on the strength of SR and RCS.
- [39] F. Gamiz, J. B. Roldan, J. E. Carceller, and P. Cartujo, "Monte Carlo simulation of remote-Coulomb-scattering-limited mobility in metalloxidesemiconductor transistors," *Appl. Phys. Lett.*, vol. 82, no. 19, pp. 3251–3253, 2003.
- [40] P. Toniutti, P. Palestri, D. Esseni, F. Driussi, M. De Michielis, and L. Selmi, "On the origin of the mobility reduction in n- and p-metalloxidesemiconductor field effect transistors with hafnium-based/metal gate stacks," *J. Appl. Phys.*, vol. 112, no. 3, p. 034502, 2012.
- [41] A. Pirovano, A. L. Lacaita, G. Ghidini, and G. Tallarida, "On the correlation between surface roughness and inversion layer mobility in Si-MOSFETs," *IEEE Electron Device Lett.*, vol. 21, no. 1, pp. 34–36, 2000.
- [42] S. Barraud, M. Casse, L. Gaben, Y. Pelloux-Prayer, Z. Zeng, F. Triozon, and Y. M. Niquet, "Carrier mobility in Silicon, Strained-Si and Strained-Si_{0.7}Ge_{0.3} Nanowire Transistors," submitted for publication.