High and low-field contact Resistances in Trigate Devices in a Non-Equilibrium Green's Functions Framework

L Bourdet, Jing Li, J Pelloux-Prayer, F. Triozon, M. Cassé, S. Barraud, S. Martinie, D. Rideau, Y.-M Niquet

High and low-field contact Resistances in Trigate Devices in a Non-Equilibrium Green's Functions Framework

L. Bourdet[1,2], Jing Li[1,2], J. Pelloux-Prayer[2,3], F. Triozon[2,3], M. Cassé[2,3], S. Barraud[2,3], S. Martinie[2,3], D. Rideau[4], and Y.-M. Niquet[1,2,5]

[1] CEA, INAC-MEM, L_Sim, Grenoble, France and [2] Université Grenoble Alpes, Grenoble France,
[3] CEA, Leti, Minatec Campus, Grenoble, France.
[4] STMicroelectronics, Crolles, France
([5] e-mail : yniquet@cea.fr)

I. INTRODUCTION

As the gate length L of field-effect transistors is reaching the sub-20 nm range, the contact resistances are increasingly limiting the electrical performances of the devices. In the low field (low V_{ds}) regime, the "apparent" contact resistance R_c can be defined as the extrapolation to zero gate length of the total resistance of the device, $R(L) = V_{ds}/I_{ds}$, where I_{ds} is the drain current and V_{ds} the source-drain voltage. This contact resistance is dominated by i) the quality of the metal-semiconductor contact, ii) the transport through the lowly doped regions of the devices such as the spacers, and iii) the "ballistic" resistance of the channel (usually mixed into the apparent contact resistance as it is independent on the gate length). In the high V_{ds} regime, the total resistance is no more linear with respect to the gate length, so that the question is whether it is still possible to define a meaningful contact resistance. In this work, we compute components ii) and iii) of the contact resistance at low and high field in Fully-Depleted Silicon-on-Insulator (FDSOI) Trigate and FinFET devices in a Non-Equilibrium Green's Functions (NEGF) framework [1,2]. The simulation results are compared to recent electrical measurements on Trigate devices fabricated at CEA-LETI.

II. SIMULATION METHODOLOGY AND DEVICES

The channel is a rectangular [110] oriented silicon nanowire with width W and height H in the 4 to 24 nm range, etched in a (001) SOI layer [3]. It is lying on a 25 nm thick buried oxide (BOX) and a n-doped Si substrate (donor concentration $N_d = 10^{18}$ cm^{-3}). The gate stack is made of 0.8 nm SiO_2 and 2.2 nm HfO_2. The gate is separated from bulk source and drain contacts by 6 nm long Si_3N_4 spacer regions (see Fig. 1). Point-like dopants are added to the source and drain according to the different target distributions plotted in Fig. 2, in order to capture impurity scattering in these regions. Surface roughness, Remote Coulomb Scattering (RCS) in the channel and electron-phonon interactions are also included in the simulations. The current is computed with NEGF in the effective mass approximation.

III. RESULTS

At low bias (V_{ds} = 10mV), the resistance $R(L)$ of the devices is linear with L in the 20-100 nm range and can therefore be extrapolated to L = 0 [4]. A quasi-Fermi level (QFL) analysis has also been performed, plotted in Fig. 3 for a 10 × 10 nm Trigate with length L = 30 nm. The QFL highlights where the potential drops in the system. The drop is much smaller in the highly-doped source and drain regions than under the spacers, which thus give the main contribution to the contact resistance. The QFL decreases almost linearly in the channel, which shows that the concept of mobility remains valid in a 30 nm long channel.

The influence of some relevant technological parameters on the contact resistance has also been investigated. Devices with different doping profiles (Fig. 2) have been studied and their contact resistances are plotted in Fig. 4. In Fig. 5, the contact resistances of devices with different channel with $W = H$ are plotted. R_c as well as the local variability (standard deviation computed on eight different devices) increase for decreasing cross-sections, For rectangular FinFET and Trigate devices, R_c has been computed for different shapes (Fig. 6). The contact resistances of devices with $H >> W$ tend to the contact resistance of the symmetric double gate device, while for devices with $W >> H$ they tend to the contact resistance of the planar FDSOI device. Finally experimental data for $W = 40 \times H = 12$ nm and $W = 14 \times H = 12$ nm devices with 9 nm thick spacers are compared to simulations: the measured R_c are in good agreement with the simulations, and show the same $1/V_{gt}^{\beta}$ dependence.

At high V_{ds} non linear effects appear, due to the presence of hot carriers in the channel (see Fig. 8), and the contributions of the source and drain to the contact resistance are no more symmetric. The contributions of scattering by phonons and impurities in the source and drain have been investigated and the results are shown Fig. 9. The most resistive part is the drain, where phonons are the main scattering mechanism. The method of extraction of the contact resistances at high V_{ds} and their additivity will be discussed at the conference.

This work was supported by the French National Research Agency (ANR) project Noodles. The calculations were run on the TGCC/Curie machine thanks to allocations from PRACE and GENCI.

REFERENCES

[1] Y.-M. Niquet, V.-H. Nguyen, F. Triozon, I. Duchemin, O. Nier, and D. Rideau, *Journal of Applied Physic*, 115, 054512 (2014).

[2] M. P. Anantram, M. S. Lundstrom, and D. E. Nikonov, *Proceedings of the IEEE*, 96, 1511 (2008).

[3] R. Coquand, M. Cassé, S. Barraud, D. Cooper, V. Maffini-Alvaro, M. Samson, S. Monfray, F. Boeuf, G. Ghibaudo, O. Faynot, and T. Poiroux, *IEEE Transactions on Electron Devices* 60, 727 (2013).

[4] L. Bourdet, J. Li, J. Pelloux-Prayer, F. Triozon, M. Cassé, S. Barraud, S. Martinie, D. Rideau, and Y.-M. Niquet, *Journal of Applied Physics* 119(8), 084503 (2016).

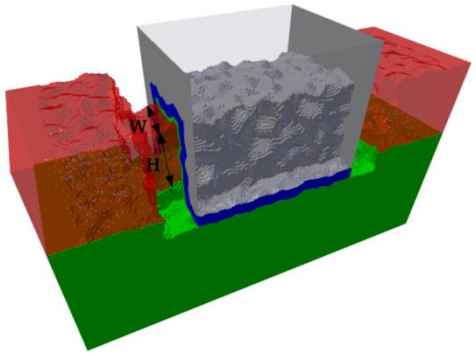

Fig. 1: *A W = 10 × H = 10 nm Trigate device, with overgrown source and drain contacts. Silicon is in red, SiO_2 in green, HfO_2 in blue and the gate in gray. The dots in the contacts are single dopants impurities. The spacers are 6 nm long.*

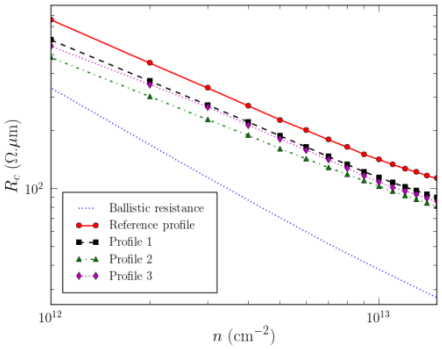

Fig.4: *The contact resistance R_c as a function of the carrier density n for the different doping profiles of Fig. 2.*

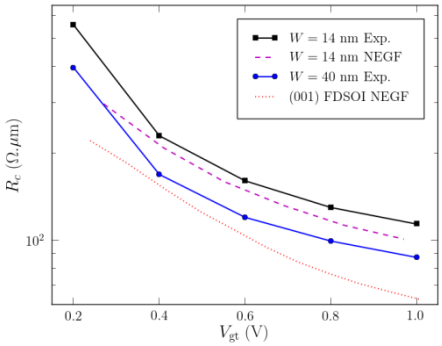

Fig 7: *Measured contact resistances in W = 40 × H = 12 nm and W = 14 × H = 12 nm Trigate devices, as a function of gate overdrive. They are compared with simulations for a planar (001), 12 nm thick FDSOI device and for a W = 14 × H = 12 nm Trigate device.*

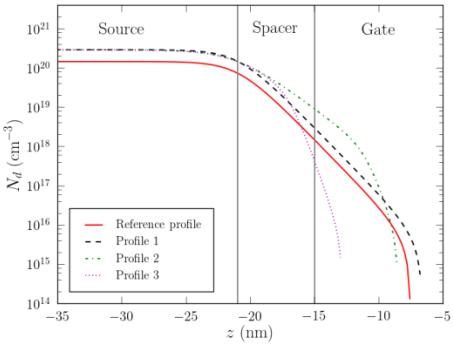

Fig. 2: *Target doping profiles in the source of Fig. 1 (doping profiles are symmetric in the drain), used to generate random dopant distribution.*

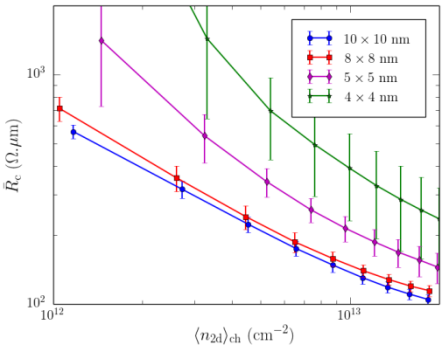

Fig 5: *The contact resistance R_c as a function of n for different nanowire cross-sections of "square" devices (W = H), with the "Reference" doping profile of Fig. 2. The bars correspond to the standard deviation computed on eight different samples.*

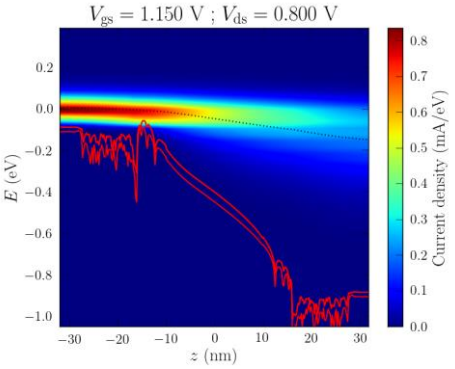

Fig 8: *Spectral density of current along the nanowire axis at V_{ds} = 0.8 V and in strong inversion for a W = 10 × H = 10 nm Trigate device with 20 nm gate length. The red lines are the conduction band profiles of the X, Y and Z valleys.*

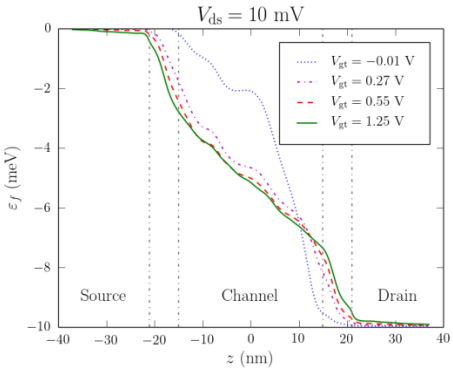

Fig. 3: *Quasi-Fermi level in a 30 nm long device (Fig. 1) with the reference doping profile of Fig. 2, at different gate overdrives. The drain bias is V_{ds} = 10 mV.*

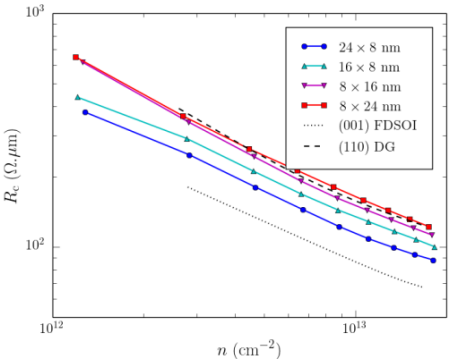

Fig 6: *The contact resistance R_c as a function of n for different nanowire cross-sections W × H. The doping profile is the "Reference" profile of Fig. 2. The data are compared with reference (001) FDSOI (H = 8 nm, W→∞) and (110) double gate devices (W = 8 nm, H→∞).*

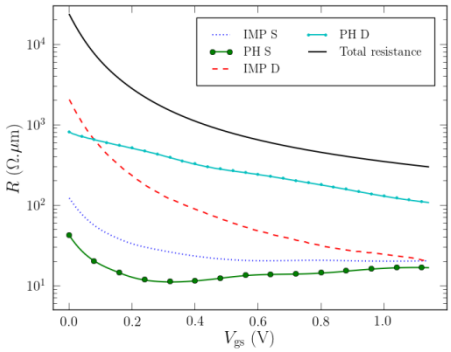

Fig 9: *Contributions of scattering by phonons (PH) and by impurities (IMP) in the source (S) and drain (D) to the total resistance at V_{ds} = 0.8 V in a W = 10 × H = 10 nm Trigate device with 20 nm gate length. The total resistance includes the channel resistance.*