Stacked-Wires FETs for advanced CMOS scaling

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Abstract

We present recent progress on vertically stacked-wires MOSFETs with a replacement metal gate process for CMOS scaling beyond FinFET technology. Key technological challenges (such as 3D integration process including inner spacer, mobility, and strain engineering) will be discussed in relation to recent research results.

1. Introduction

Gate-All-Around (GAA) field-effect-transistors have long been recognized as offering the best solution to short-channel-effects (SCE) with a high current drivability per layout footprint due to 3D vertically stacked channels [1-4]. Moreover, horizontal GAA NanoWires (NWs) also have the advantage of being fabricated with minimal deviation from FinFET devices in contrast to vertical NWs which require more disruptive technological changes. For these reasons, the GAA stacked-wires MOSFET architecture is today regarded as an attractive option to push CMOS scaling beyond 7/5nm nodes. Although the first 3D GAA transistors were demonstrated ten years ago [1-4], significant progress have been reported last year [5-6] with aggressive 44/48 CPP (Contacted Poly Pitch) ground rules [7]. In this paper we will discuss recent progress and the major roadblocks remaining to reach higher performances in such devices, in particular stress boosters and parasitic capacitances.

2. Design options of GAA stacked-wires devices

Two main options can be considered for GAA transistors (**Fig. 1**). As compared to FinFET, the conventional square (or round) NW has a lower effective width (W_{eff}) in a given layout footprint even if the Drain-Induced Barrier Lowering (DIBL) shown in **Fig. 2** is strongly reduced. However, wide and thin Nanosheets (NS) can significantly increase W_{eff} compared to conventional FinFETs (or stacked-NW) and therefore offer better current drivability. As shown in **Fig. 3**, stacked nanosheets show the best compromise to maximize W_{eff} while having similar and even lower DIBL. The capability to have a fine-tuning of the sheet width enables V_T flavors relevant for power-performance optimization [7,8,9].

3. Carrier mobility

The computed carrier mobilities in [110]-oriented GAA NS, NW and FinFET devices are shown in **Figs. 4-7**. The size-dependent carrier mobility in 3D multi-gate devices is mainly due to facet-dominated transport with high (resp. low) electron mobility in the (100) (resp. (110)) plane and high (resp. low) hole mobility in the (110) (resp. (100)) plane. Meanwhile, mobility in conventional NWs is often the worse due to additional quantum confinement effects resulting in mobility reduction. Horizontal GAA NS for n-FET and vertical GAA NS for p-FET turn out to be the best possible configuration to promote electron and hole transport.

4. Device integration and performance

Over the last year, vertically stacked-NW/NS MOSFETs were fabricated using a replacement metal gate process with specific technical requirements compared to FinFET [5-7]. The fabrication started with the epitaxial growth of ($Si_{0.7}Ge_{0.3}/Si$) multilayers. **Fig. 8a** shows a TEM image of (*SiGe/Si*) multilayers with three Si channels and two sacrificial SiGe layers. Then, individual and dense arrays of fins were patterned to fabricate stacked-wires FETs. Multiple patterning techniques were used in order to meet the density targets of advanced nodes. **Fig. 8b** shows TEM images in the transverse and longitudinal directions after the etching of *(SiGe/Si)*-fins. Our SIT-based patterning technique yielded 40 nm-pitch fins which were 60 nm high and roughly 20 nm wide. After that, dummy gates and spacers were defined prior to the anisotropic etching of the (*SiGe/Si*) multilayers. Then, the SiGe layers were partially etched selectively to the Si ones to form inner spacers well-aligned and correctly dimensioned as shown in **Fig. 8c**. The Si wires were released during the Replacement Metal Gate (RMG) module prior to conformal HfO_2/TiN/W gate deposition (**Fig. 8d**). If the fabrication of stacked-wires FETs including inner spacer is crucial to reduce parasitic capacitances, another major challenges is the strain engineering used to improve short-channel performances. Strain fields were imaged at different stages of our fabrication process. For example, SiGe(B) raised-Source/Drain were used to inject a significant amounts of compressive strain in Si channels (**Fig. 9b**). The level of in-plane deformation in Si *p*-channels became close to 1%. Meanwhile, no strain was generated with Si raised-S/Ds (**Fig. 9a**). A typical transfer and output characteristics of stacked-NWs *p*-FET with L_G=25 nm and W~30 nm is shown in **Fig. 10**.

5. Conclusion

Recent results in stacked Nanosheet transistors demonstrate the high competitiveness of this technology for future technology nodes. Thanks to the benefits of large W_{eff}, the Nanosheet architecture is a versatile design option for performance and power management.

Acknowledgements

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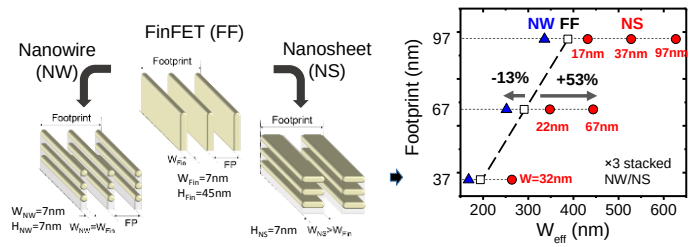

Fig. 1 : (Left) Two GAA transistor options in order to replace FinFET: NanoWire (W_{NW}=W_{Fin}) and NanoSheets (W_{NS}>W_{Fin}). (Right) In contrast to NW, a significant increase in effective width (W_{eff}) can be achieved with GAA NS transistors at constant footprint. W_{eff} is defined as the circumference of FF, NW, or NS.

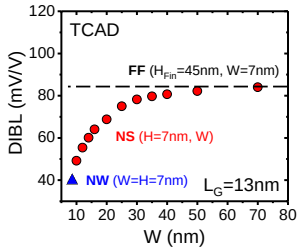

Fig. 2 : DIBL *vs* Width (W) at L_G=13nm. Immunity to SCE of GAA NS is between the NW and FinFET (FF) boundaries.

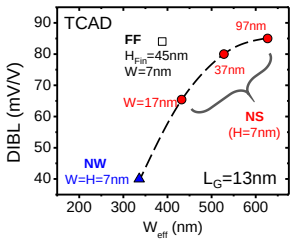

Fig. 3 : DIBL *vs* W_{eff} at L_G=13nm. Improvement in W_{eff} at constant DIBL for GAA NS compared to FinFET (FF) devices.

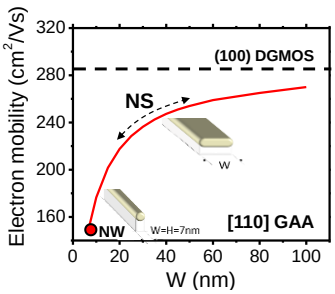

Fig. 4 : Electron mobility *vs* W for [110] GAA NW/NS FETs (H=7nm).

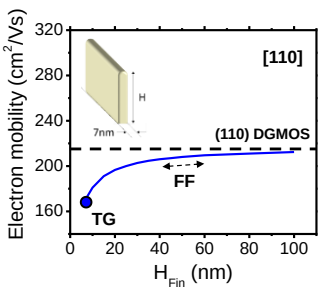

Fig. 5 : Electron mobility *vs* H_{Fin} for [110] FinFET transistors (W=7nm). TG stands for Triple Gate (W=H).

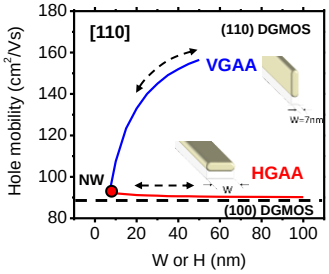

Fig. 6 : Hole mobility *vs* W or H for [110] horizontal (HGAA, H=7nm) and vertical (VGAA, W=7nm) FETs.

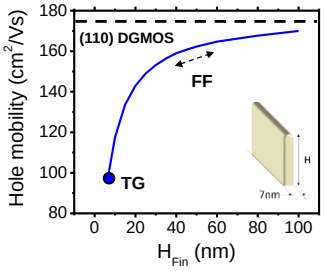

Fig. 7 : Hole mobility *vs* H_{Fin} for [110] FinFET (FF) transistors (W=7nm). TG stands for Triple Gate (W=H).

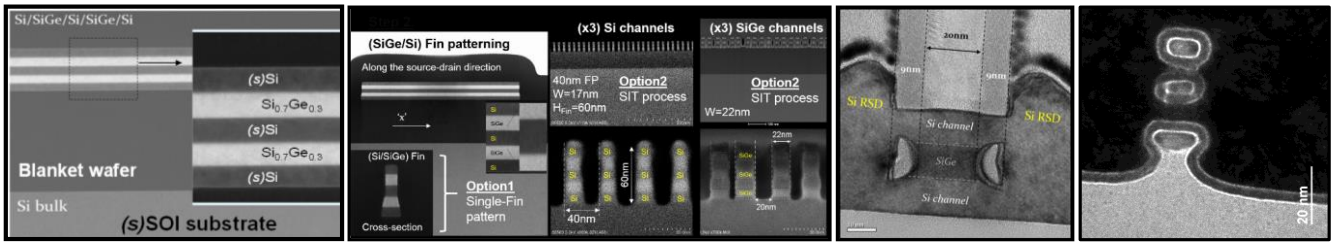

Fig. 8: Cross-sectional Transmission Electron Microscopy (TEM) images at various stages of the stacked-NW/NS fabrication process. (a) Formation of (Si/SiGe) superlattices with 3 levels of Si layers stacked upon one another. (b) Etching of (Si/SiGe) fins shown in the longitudinal and transverse directions of future Si (or SiGe) wires. Two fins patterning were used: (*left*) single-fin process and (*right*) dense array of fins with a Sidewall Image Transfer (SIT) process. (c) Stacked-wires FET after the integration of inner spacer. (d) Stacked-wires FET with a HfO_2/TiN/W gate stack.

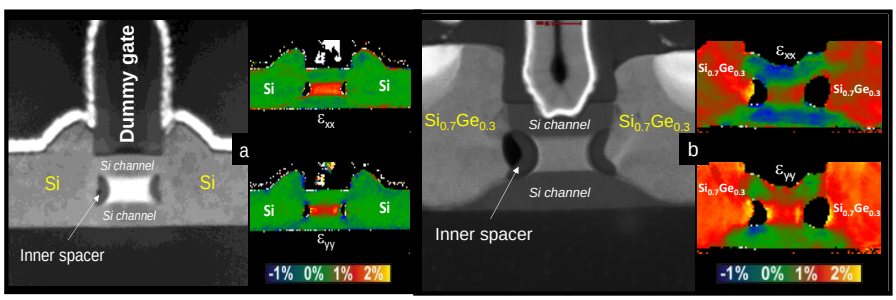

Fig. 9: HAADF STEM images of stacked-NWs *p*-FETs and Precession Electron Diffraction deformation maps in the (ε_{xx}) and (ε_{yy}) directions. Strain is measured after Si (a) and $Si_{0.7}Ge_{0.3}$:B (b) S/D epitaxy. No strain into Si *p*-channels for Si S/Ds. However, recessed and epitaxially regrown $Si_{0.7}Ge_{0.3}$:B S/Ds inject a compressive strain close to 1% (in blue) in the top and bottom Si *p*-channels.

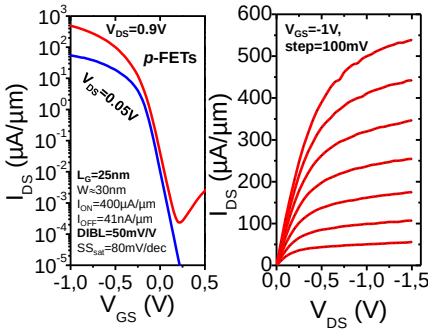

Fig. 10: (*Left*) I_{DS}-V_{GS} and (*right*) I_{DS}-V_{DS} characteristics of stacked-NS *p*-FETs with L_G=25nm. Here, the width W~30nm.