NSP: Physical compact model for stacked-planar and vertical Gate-All-Around MOSFETs

O. Rozeau[1], S. Martinie[1], T.Poiroux[1], F. Triozon[1], S. Barraud[1], J. Lacord[1], Y. M. Niquet[2], C. Tabone[1], R. Coquand[1], E. Augendre[1], M. Vinet[1], O. Faynot[1] and J.-Ch. Barbé[1]
[1]CEA-Leti, Minatec Campus, 38054 Grenoble, France, email: olivier.rozeau@cea.fr
[2]CEA-INAC, Grenoble, France

***Abstract*— In this work, a predictive and physical compact model for NanoWire/NanoSheet (NW/NS) Gate-All-Around (GAA) MOSFET is presented. Based on a novel methodology for the calculation of the surface potential including quantum confinement, this model is able to handle arbitrary NW/NS cross-section shape of stacked-planar and vertical GAA MOSFETs (circular, square, rectangular). This Nanowire Surface Potential (NSP) based model, validated both by numerical simulations and experimental data, is demonstrated to be very accurate in all operation regimes of GAA MOSFETs.**

I. INTRODUCTION

Due to its excellent immunity to the Short Channel Effects (SCE), undoped GAA MOSFET is one of the most promising candidate for sub-7nm CMOS technologies [1]. GAA quasi-cylindrical or square cross-section NanoWires (NW) can be used for an optimized gate control of the channel in order to minimize static power consumption. Meanwhile, GAA NanoSheet (NS) (e.g. *thin* and *wide* NW) MOSFETs can be proposed in order to increase the drive current for high performance applications. No compact model of GAA MOSFETs accounting for multiples shapes of NW/NS cross-section has been proposed yet. In this work, we present a novel and complete Surface Potential (SP) -based model for stacked-planar and vertical NW/NS GAA MOSFETs mandatory for the design of integrated circuits.

II. EFECTIVE SURFACE POTENTIALS

Typical undoped stacked-planar and vertical GAA MOSFETs are illustrated in Fig. 1. The number of NW/NS can be higher than two with different widths. The major modeling challenge is to account for the variation of SP along the NW/NS perimeter. To circumvent this mathematical challenge an effective SP is defined and calculated based on a decomposition of the structure cross-section into the sum of a Symmetrical Double-Gate (SDG) and a Cylindrical GAA MOSFET (C-GAA). Fig. 2 illustrates the asymptotic cases of a NS cross-section.

Using [2], the schematic of Fig. 3 and the notations in Table 1, Poisson's equation for C-GAA MOSFET is written as:

$$\frac{d^2x}{dr^2}+\frac{1}{r}\cdot\frac{dx}{dr}=\Delta\cdot exp(x-x_n) \quad \text{with} \quad \Delta=\frac{q\cdot n_i}{\varepsilon_{si}\cdot\phi_t} \qquad (1)$$

In [2], an ingenious transformation of variables is proposed:

$$\begin{cases}\alpha = r\cdot\frac{dx}{dr}\\ \beta = r^2\cdot exp(x-x_n)\end{cases} \qquad (2)$$

Several publications use this transformation of variables to solve Poisson's equation where the well-known solution is given by [3]:

$$x=ln\left(-\frac{8\cdot\delta}{\Delta\cdot(\delta\cdot R^2+1)^2}\right) \qquad (3)$$

δ is a new unknown variable defined by the boundary conditions. An analytical approximation is given in [4]. In this work, we propose a solution which consists in introducing the boundary conditions in (1) by using (2). The result is an equation written as,

$$(x_g-x)^2+B\cdot(x_g-x)=\Delta_f\cdot exp(x-x_n) \qquad (4)$$

with $B=\frac{4\cdot C'_{si}}{C'_{ox}}$, $C'_{si}=\frac{\varepsilon_{si}}{R}$, $C'_{ox}=\frac{\varepsilon_{ox}}{R\cdot\ln\left(1+\frac{T_{ox}}{R}\right)}$ and $\Delta_f=\frac{2\cdot q\cdot n_i\cdot\varepsilon_{si}}{\phi_T C'^{\,2}_{ox}}$

Then, (4) can be easily solved as described in [5]. SP calculation starts with an initial guess followed by two successive corrections based on Taylor's developments. This analytical calculation was validated on gate capacitance C_{gg} by TCAD simulations. An excellent agreement is achieved especially in moderate inversion which is the most challenging regime to describe (Fig. 3).

For SDG MOSFET, a similar approach can be used. In a Cartesian coordinate system (Fig. 4), Poisson's equation is written as:

$$\frac{d^2x}{dy^2}=\Delta\cdot exp(x-x_n) \qquad (5)$$

Similarly to cylindrical case, the transformation of variables is defined as,

$$\begin{cases}\alpha = \frac{dx}{dy}\\ \beta = y\cdot exp(x-x_n)\end{cases} \qquad (6)$$

The result is (4) but now with a new definition of capacitances: $C'_{si}=\frac{\varepsilon_{si}}{T_{si}}$ and $C'_{ox}=\frac{\varepsilon_{ox}}{T_{ox}}$.

The mathematical procedure to calculate SP 'x' is exactly the same as for C-GAA case. Fig. 4 shows a validation in the case of SDG MOSFET.

Equation (4) can be considered as an "universal" equation to describe asymptotical cases. The only differences between both are C'_{si} (where R is replaced by T_{si}) and C'_{ox}. Fig. 5 allows to easily understand the behavior of surface potential described

by (4). The strong inversion is controlled by C'_{ox} only while both capacitances C'_{si} and C'_{ox} are included in the weak inversion. In addition, the total inversion charge used for the charge and the current calculation is given by:

$$Q_i = W_{eff} \cdot C'_{ox} \cdot \phi_T \cdot q_i \quad (7)$$

W_{eff} denotes the NS/NW perimeter and can be easily calculated considering the geometrical parameters. Thus, using a rigorous description of W_{eff}, C'_{ox} and C'_{si}, all GAA MOSFET architectures can be modeled.

As shown by the schematic in Fig. 6, NS GAA MOSFET can be decomposed in three parts: two outer parts which represent the left (resp. right) half of the NW cross-section and an inner part equivalent to a SDG transistor. W_{eff}, C'_{ox} and C'_{si} are calculated using geometrical parameters described in Fig. 6. The outer part sections can be purely cylindrical or quasi-square with different corner radius R_c. The effective radius is analytically calculated and validated in Fig. 7. This partitioning approach and the calculation of all geometrical parameters are validated using TCAD simulations (Fig. 8). An excellent agreement is achieved between the model and simulations resulting in the validation of SP without any fitting parameter.

Using a similar approach, W_{eff}, C'_{ox} and C'_{si} can be calculated for stacked-NS (SNS) GAA MOSFETs (Fig. 8). The model is able to accurately model SNS GAA MOSFET with different widths between top and bottom channels (see Fig. 1) without any fitting parameter.

III. Quantum Confinement Modeling

In NSP model, the quantum confinement (QC) was introduced thanks to corrections on the oxide capacitance accounting for the effect of carrier effective mass on the charge centroid position (Fig. 9: DS for dark-space) and on the flat-band voltage due to structural quantum confinement. DS is calculated by considering a constant electrical field at the silicon-oxide interface similarly to [6] for both inner and outer parts. A clamped value DS_0 was introduced to physically describe the weak inversion regime. DS_0 has a significant impact on the model accuracy especially for small NS cross-sections and is rigorously calculated by considering the first order of the trial eigenfunction as described in [7]. To validate quantum confinement effects in our model, the software TB_SIM [8] has been used to solve the Poisson-Schrödinger equations in GAA MOSFETs. Fig. 10 and 11 show the validation of QC for a square cross-section with several corner radius and for single NS and SNS GAA MOSFETs. In this model, a single effective mass is defined as a function of device polarity, Si orientation and Ge concentration for pFET without any fitting parameter.

IV. Currents and Charges Including Parasitics

Similarly to [9-10], an analytical calculation of drain current is performed by considering SP at the drain and source sides. The model core was validated using TCAD simulations for long channel transistor with a constant mobility (see Fig. 12 and 13). The drain, source and gate charges are calculated as described in [9-10]. Fig. 14 illustrates the charge partitioning between the drain and the source. In the same way to [11], additional physical features like electrical field dependence on mobility, SCE, DIBL, channel length modulation effect, access resistances with bias dependence, velocity saturation, GIDL current gate tunneling current and parasitic capacitances were implemented in the model code for both stacked-planar and vertical GAA MOSFET architectures.

V. Model Validation

The model was validated using: (i) TCAD simulations of short channel MOSFET including electrical field dependent mobility, velocity saturation and access resistances (Fig. 15 to 18) and (ii) experimental data (case of short channel SNS GAA MOSFET: Fig. 19 to 21). The good agreement shown between the model and experimental data highlights that this compact model is accurate and provides a credible quantitative estimates of NW/NS GAA MOSFETs operation. NSP model is implemented in Verilog-A language respecting requirements related to simulation robustness [12] like symmetry tests as illustrated in Fig. 22. Finally, NSP model is now ready for the design of first circuits based on stacked-planar and vertical NW/NS GAA MOSFETs.

Acknowledgment

This work has been carried out in the frame of the IBM/LETI collaboration program and has been partially funded by the French Public Authorities through the NANO 2017 program and by SUPERAID7 (grant N° 688101) project.

References

[1] K. Tachi *et al.* "Experimental study on carrier transport limiting phenomena in 10 nm width nanowire CMOS transistors," in *Proc. 2010 IEEE International Electron Devices Meeting*, pp. 34.4.1 - 34.4.4.

[2] Y. Chen and J. Luo, "A comparative study of double-gate and surrounding-gate MOSFETs in strong inversion and accumulation using an analytical model," in *Proc. 2001 International Conference on Modeling and Simulation of Microsystems*, pp. 546-549.

[3] D. Jimenez *et al.* "Continuous analytic I–V model for surrounding-gate MOSFETs," IEEE Electron Device Letters, vol. 25, pp. 571–573, August 2004.

[4] B. Yu *et al.* "Explicit continuous models for double-gate and surrounding-gate MOSFETs," IEEE Trans. On Electron Devices, vol. 54, pp. 2715-2722, October 2007.

[5] T. L. Chen and G. Gildenblat, "Analytical approximation for the MOSFET surface potential," Solid-State Electronics, vol. 45, pp. 355–339, February 2001.

[6] F. Stern, "Self-consistent results for n-type Si inversion layers," Physical Review B, vol. 5, pp. 4891–4899, June 1972.

[7] L. Ge and J. G. Fossum. "Analytical modeling of quantization and volume inversion in thin Si-film DG MOSFET," IEEE Trans. On Electron Devices, vol. 49, pp. 287-294, February 2002.

[8] TB_SIM simulator: Site web: http://inac.cea.fr/L_Sim/TB_Sim/

[9] O. Rozeau *et al.* "Surface potential based model of ultra-thin fully depleted SOI MOSFET for IC simulations" in *Proc. 2011 IEEE International SOI Conference.*

[10] G. Gildenblat *et al.* "PSP: An Advanced Surface-Potential-Based MOSFET Model for Circuit Simulation," IEEE Trans. On Electron Devices, vol. 53, pp. 1979-1993, September 2006.

[11] T. Poiroux *et al.* "UTSOI2: A Complete Physical Compact Model for UTBB and Independent Double Gate MOSFETs," in *Proc. 2013 IEEE International Electron Devices Meeting*, pp. 12.4.1-12.4.4.

[12] C. C. McAndrew, "Validation of MSOFET model source-drain symmetry," IEEE Trans. On Electron Devices, vol. 53, pp. 2202-2206, September 2006.

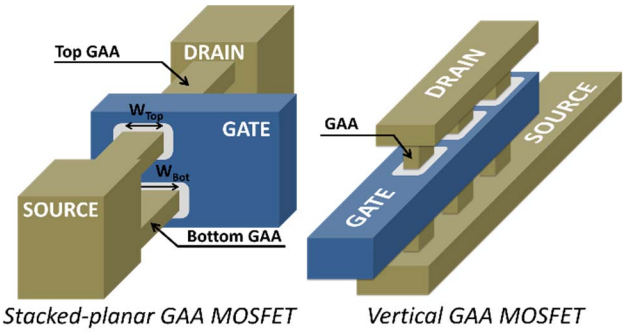


Fig. 1. Typical stacked-planar and vertical GAA NW/NS MOSFET architectures.

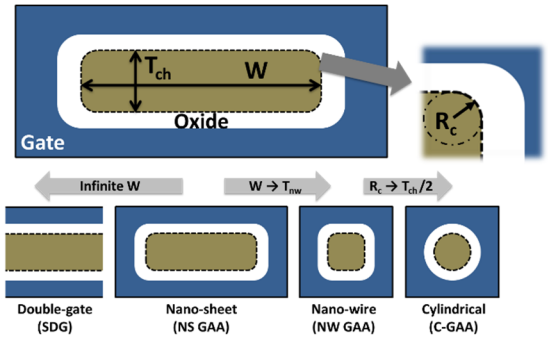


Fig. 2. Description of NS GAA MOSFET architecture and its asymptotic cases.

ϕ_T	Thermal voltage
T_{ox}	Gate oxide equivalent thickness
W	Nano-sheet width
L	Gate length
R_c	Radius of nano-sheet corners
T_{ch}	Nano-sheet silicon thickness
C'_{ox}	Gate oxide capacitance per area unit
C'_{si}	Body capacitance per area unit
x_g	Gate to source voltage normalized to ϕ_T
x_{nds}	Drain to source voltage normalized to ϕ_T
x_n	Quasi-Fermi level normalized to ϕ_T
x	Surface potential normalized to ϕ_T
q_i	$(= x_g - x)$ Gate charge density normalized to $C_{ox}\phi_T$

Table 1. Notations used in this work

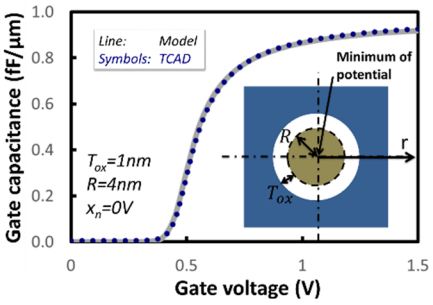


Fig.3. Gate capacitance vs gate voltage of C-GAA MOSFET: comparison between TCAD and analytical solution of (4).

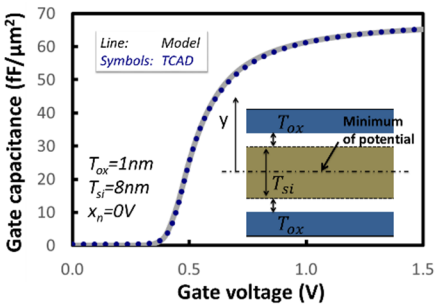


Fig.4 Gate capacitance vs gate voltage of SDG MOSFET: comparison between TCAD and analytical solution of (4).

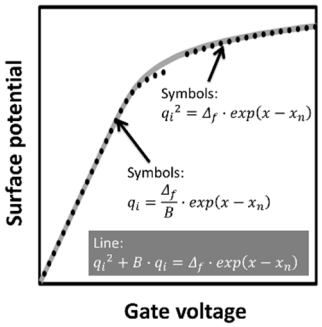


Fig. 5. Effective surface potential vs gate voltage for analysis of (4).

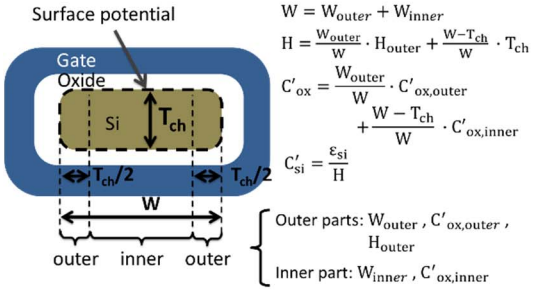


Fig. 6. Partitioning of NS GAA MOSFET and related geometrical parameters and variables.

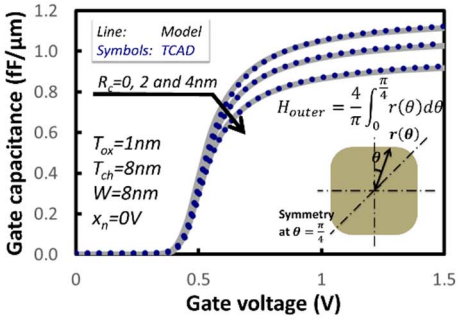


Fig. 7. Gate capacitance vs gate voltage of quasi-cylindrical GAA devices with several R_c.

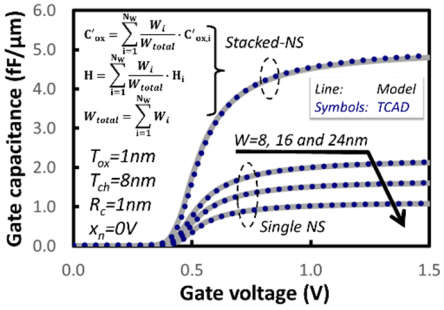


Fig. 8. Gate capacitance vs gate voltage of single and stacked NS GAA MOSFET with several W.

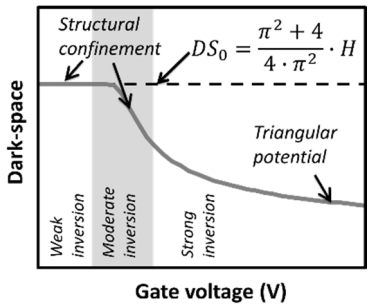


Fig. 9. Distance between charge centroid and oxide-silicon interface versus gate voltage for quantum confinement modeling.

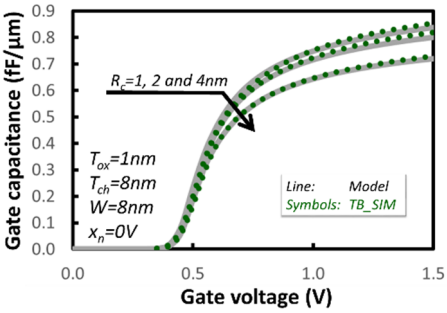


Fig. 10. Gate capacitance versus gate voltage of quasi-cylindrical GAA MOSFET with several R_c for the validation of quantum confinement correction.

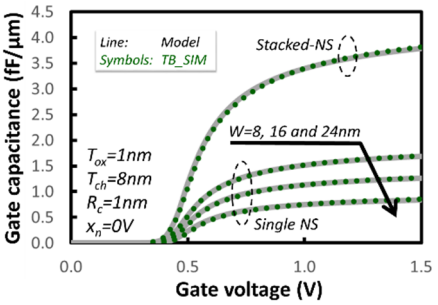


Fig. 11. Gate capacitance vs gate voltage of single and stacked NS GAA MOSFET with several W for the validation of quantum confinement correction.

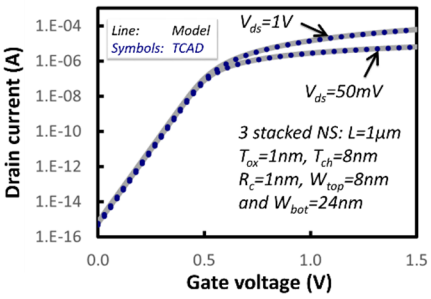


Fig. 12. Drain current vs gate voltage of SNS GAA MOSFET (no fitting parameter) for the validation of model's core.

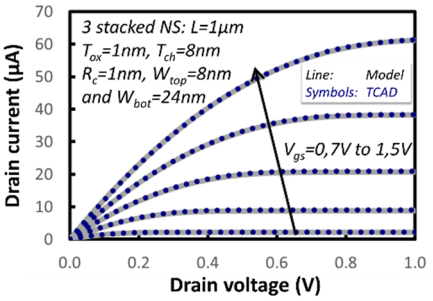


Fig. 13. Drain current vs drain voltage of SNS GAA MOSFET (no fitting parameter) for the validation of model's core.

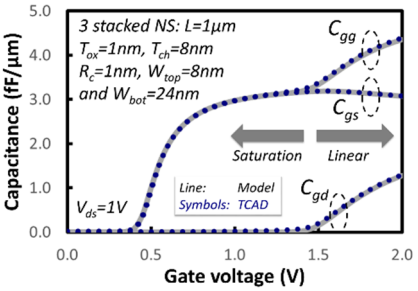


Fig. 14. Input capacitances vs gate voltage of SNS GAA MOSFET (no fitting parameter) in saturation regime for the validation of model's core.

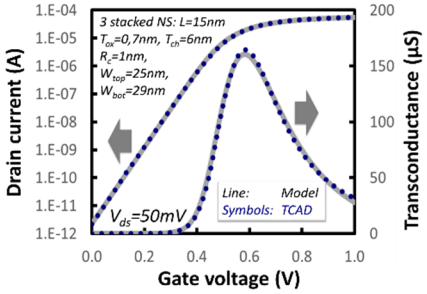


Fig. 15. Drain current and its derivative vs gate voltage of SNS GAA MOSFET in linear regime for the validation of model's core.

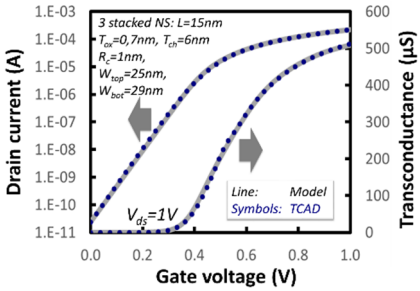


Fig. 16. Drain current and its derivative vs gate voltage of short channel SNS GAA MOSFET in saturation regime for the validation of model's core.

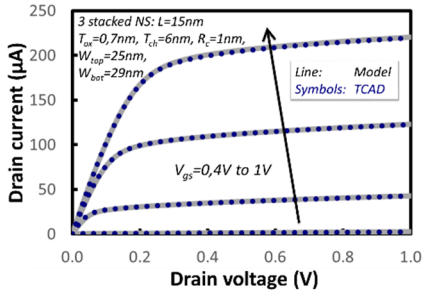


Fig. 17. Drain current vs drain voltage of SNS GAA MOSFET for the validation of model's core.

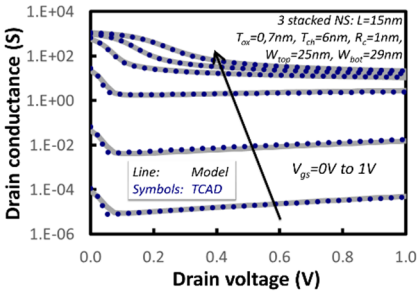


Fig. 18. Drain conductance vs drain voltage of short channel SNS GAA MOSFET for the validation of model's core.

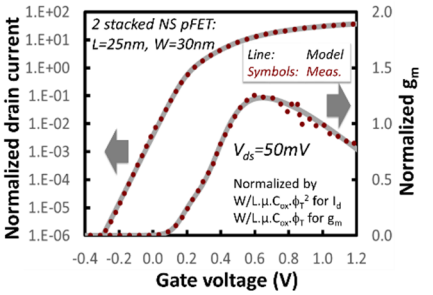


Fig. 19. Normalized drain current and its derivative vs gate voltage in linear regime: comparison between NSP model and experiments.

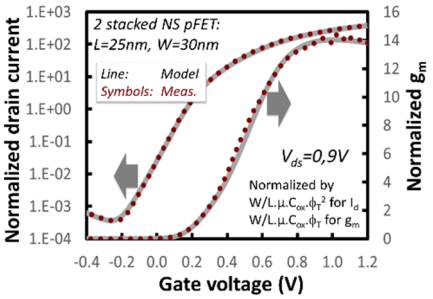


Fig. 20. Normalized drain current and its derivative vs gate voltage in saturation: comparison between NSP model and experiments.

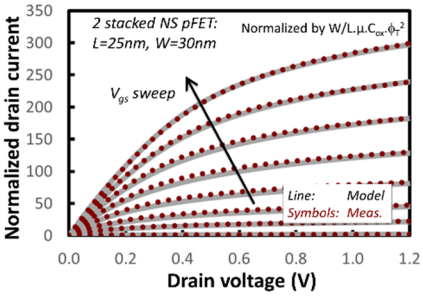


Fig. 21. Normalized drain current vs drain voltage: comparison between NSP model and experiments.

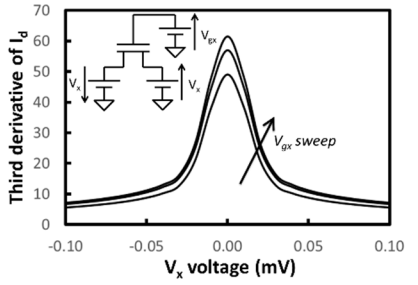


Fig. 22. Third derivative of the drain current for symmetry checking related to [12].