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***Abstract*—**We report on vertically stacked horizontal Si NanoWires (NW) *p*-MOSFETs fabricated with a replacement metal gate (RMG) process. For the first time, stacked-NWs transistors are integrated with inner spacers and SiGe source-drain (S/D) stressors. Recessed and epitaxially re-grown SiGe(B) S/D junctions are shown to be efficient to inject strain into Si *p*-channels. The Precession Electron Diffraction (PED) technique, with a nm-scale precision, is used to quantify the deformation and provide useful information about strain fields at different stages of the fabrication process. Finally, a significant compressive strain and excellent short-channel characteristics are demonstrated in stacked-NWs *p*-FETs.

I. Introduction

The vertically stacked wires MOSFET architecture pushes further the scaling limits of the CMOS technology [1-4]. Now deemed as a possible extension to FinFET, it offers multiple benefits. A low I_{OFF} current is indeed expected, thanks to multi-gate electrostatic control, with a high current drivability due to 3D vertically stacked channels [3-5]. Obviously, major roadblocks still remain to reach higher performances, in particular, stress boosters and parasitic capacitances. Gate-All-Around (GAA) MOSFETs based on Si NWs that call upon RMG FinFET process technology were recently reported [6-7]. Nevertheless, none of them demonstrated the integration of inner spacers which is key in order to reduce gate-source/drain capacitances in such a 3D integration process. In this work, we introduced, for the first time, inner spacers and SiGe S/D in a RMG stacked wires process. Wider, thinner and stacked wire structures have been proven to be efficient to match or exceed FinFETs performance due to higher W_{eff}/footprint ratio [8-9]. The strain engineering requires also dedicated optimization because of the opportunities brought to the channel to relax. The morphological strain evolution along the fabrication process will be presented thanks to PED technique [10] and then, we will quantify electrical performance of stacked-NWs *p*-FETs.

II. Device Fabrication

The RMG process flow for vertically stacked-NWs MOSFETs is presented in **Fig. 1**. The transistors are processed on 300 mm SOI substrates. GAA stacked-NWs FETs, which are close to the RMG FinFET technology, have nevertheless specific technical requirements. They are numbered "**1** to **5**" in **Fig. 1**. The fabrication starts with the epitaxial growth of (*$Si_{0.7}Ge_{0.3}$/Si*) multilayers on blanket SOI substrates. Growth pressure was 20 Torr, while the growth chemistry changed between SiGe (SiH_2Cl_2 + GeH_4) and Si (SiH_4), in order to have satisfying growth rates at 650°C [11]. Different Si/SiGe stacks have been investigated: (i) a ***(Si/SiGe/Si)***-stack for which the two Si channels and the sacrificial SiGe layer have thicknesses around 12 nm and (ii) a ***(Si/SiGe/Si/SiGe/Si)*** multilayer with lower layer thicknesses (7 nm for Si and 8 nm for the SiGe layers). They should yield two and three stacked Si channels, respectively. **Fig. 2a** (resp. **2b**) shows TEM images and Energy-Dispersive X-ray (EDX) spectroscopy maps of (*SiGe/Si*) multilayers grown on strained-SOI (resp. SiGeOI) substrates in order to have ×3 tensile strained Si channels for *n*-FETs (resp. ×3 compressive strained SiGe channels for *p*-FETs). X-ray reflectivity (XRR) measurements were performed on each multilayer in order to have a precise determination of individual layer thicknesses (**Fig. 3**). Then, individual and dense arrays of fins were patterned to fabricate stacked-NWs FETs. The Sidewall Image Transfer technique (SIT) was used in order to meet the density targets of advanced nodes. **Fig. 4** shows TEM images after etching of *(SiGe/Si)*-fins along transverse and longitudinal directions. Our SIT-based patterning technique yields 40 nm-pitch fins which are 60 nm high and roughly 20 nm wide. After that, dummy gates and spacers were defined prior to the anisotropic etching of the (*SiGe/Si*) multilayers. Then, the SiGe layers were partially etched selectively to the Si ones. Etching rates and selectivity of SiGe were studied on ***(Si/SiGe/Si/SiGe/Si)*** stacks with low layer thicknesses (7 nm for Si and 8 nm for SiGe) (**Fig. 5**). An excellent selectivity was achieved even for thin Si and SiGe layers. Then, the depth of the SiGe recess was adjusted to match the thickness of future inner spacers (**Fig. 6**). A nitride layer was deposited in the cavities with a thickness optimized for the spacer etch sequence that followed. **Fig. 7** shows TEM images of stacked-NWs FETs with inner spacers well-aligned and correctly dimensioned. The process then continued with the epitaxial growth of $Si_{0.7}Ge_{0.3}$:B raised-S/D [12]. The Si wires were released during the RMG fabrication module. This selective etch process was followed by a conformal HfO_2/TiN/W deposition (**Fig. 8**). An optimized Ω-shaped gate Si channel was used for bottom wire to maintain a good electrostatic integrity (**Fig. 8b**).

III. STRAIN CHARACTERIZATION AND MODELING

Of all the challenges that we face for GAA stacked-NWs FETs, one of the most important is the strain engineering which is used to improve short-channel performances. We have thus imaged strain fields at different stages of our fabrication process. Strain maps were obtained by TEM using the PED technique. Interpretation of the results in terms of elastic strains and stresses required some modeling. In TEM, it is indeed mandatory to consider the specimen thickness to account for elastic relaxation [13]. Hence, we developed 3D Finite Element Method (FEM) based models that include the anisotropy of the system and the materials. Stress relaxation is taken into account by building thin-foil geometries with free lateral faces. Strain values were taken as average values along the specimen thicknesses and projected in 2D as in the experiments [14]. Computations, as experiments, are presented with respect to a relaxed Si ref. In **Fig. 9**, we present strain maps for a blanket stack grown on a *s*SOI substrate. The measured deformation ε_{yy} and ε_{xx} are shown together with the TEM lamella calculations. The reconstruction of the bulk (before lamella relaxation) resulted from a validated TEM-specimen model. The vertical profiles extracted from the strain maps show that the Si layers are seen as being slightly compressed in the growth direction (by approx. -0.4%). This is due to the fact that the Si is in-plane (ε_{xx}) tensile-strained by around 0.8%. The Ge-content in the SiGe layers is adjusted in the TEM-specimen model, to fit the experiments, allowing therefore to extract Ge-content in the layers. We determined that the first layer contained 24% of Ge and the second 28%. In **Fig. 10**, we present ε_{xx} and ε_{zz} strain results after fin patterning. Strain relaxation effects are seen on the free edges of the structure. The ε_{xx} map shows that, as expected on a *s*SOI substrate, the *s*Si and the SiGe layers have larger in-plane lattice parameters than the Si ref.. Horizontal profiles from the three *s*Si channels have been extracted. In the center, the in-plane tensile strain is still around 0.8%, consistently with measurements on blanket wafers. However, the integration of inner spacers may induce a strain relaxation after the anisotropic etching of (*SiGe/Si*) superlattices (see Fig. 6). Then, SiGe(B) raised-S/Ds can be used to inject significant amounts of compressive strain in Si channels. This is well observed in **Fig. 11b**. The level of in-plane deformation in Si *p*-channels became close to 1%. Meanwhile, no strain was generated by using Si raised-S/Ds (**Fig. 11a**). Note in Fig. 11a, that the sacrificial SiGe layer between the two Si channels has larger lattice parameter than the Si ref. (ε_{xx} = 1.3%). This shows that the SiGe has partially relaxed during the integration of the inner spacers. Indeed, similar levels of deformation than those obtained on relaxed SiGe at free edge locations (see Fig. 10) are shown. This result suggests that an optimized engineering of process-induced stress techniques such as SiGe S/Ds (for *p*-FET) can be efficient in 3D stacked-NWs devices.

IV. ELECTRICAL CHARACTERISTICS

Before discussing the performances of stacked-NWs FETs, we show, in **Fig. 12**, the benefit of inner spacers in order to reduce parasitic capacitances. This is a particularly important point since thin and wide nanowires are expected to enhance drive current by increasing the effective width [8,9]. Gate capacitance vs V_{GS} of stacked wires *p*-FETs with W=25-45 nm and 500 nm gate length is shown in **Fig. 13**. The CV curves, obtained from a multi-fingers gate and an array (#120) of stacked wires, show a consistent dependence on the top view wire width, W. In **Fig. 14**, a linearity is well observed between the saturation threshold voltage $V_{T,sat}$ and the I_{ON} current (normalized by the channel perimeter). This indicates that the increase of I_{ON} current (for 25nm<L_G<70nm) takes place under SCE. The impact of top view channel-width on $V_{T,sat}$ is shown in **Fig. 15**. An increase of confinement potential as W is reduced leads to higher $V_{T,sat}$. Low values of $V_{T,sat}$ are explained by the compressive strain induced by the SiGe S/D. The I_{ON} vs I_{OFF} current is plotted in **Fig. 16** for [100] and [110] Si channels. The latest results of GAA stacked-NWs are reported [3, 7]. Improved performance of *p*-FETs devices is achieved along the [110] direction. This is explained by the compressive strain induced by the SiGe S/Ds which strengthens the light holes of the highest valence bands by pushing heavy holes subbands down. The subthreshold slope SS_{sat} and the impact of W and L_G on the DIBL are shown in **Figs. 17, 18** and **19**. These results indicate that well-controlled SCE are achieved down to L_G=25 nm. Finally, **Fig. 20** show the transfer and output characteristics of stacked-NWs *p*-FET with L_G=25 nm and W~30 nm. The device shows high performance in terms of SS_{sat} (80 mV/dec), DIBL (50 mV/V) and I_{ON} current (400 µA/µm at V_{DD}=0.9 V). The devices outperform the previous *p*-FET stacked-NW [3] due to the introduction of compressive strain.

V. CONCLUSION

Vertically stacked wires MOSFETs with inner spacers and SiGe:B S/D have been successfully fabricated for the first time with a RMG process. Precession electron diffraction has been used to provide accurate deformation maps at different process steps. The benefits of epitaxially regrown SiGe:B S/D junctions is clearly evidenced, with a significant compressive strain (~1%) injected in top and bottom Si *p*-channels. Finally, short-channel performances of devices are discussed for different widths, gate lengths, and transport orientations. Through this work, two major challenges facing the development of stacked wires technology are addressed: inner spacers and strain engineering in 3D integration processes.

ACKNOWLEDGMENT

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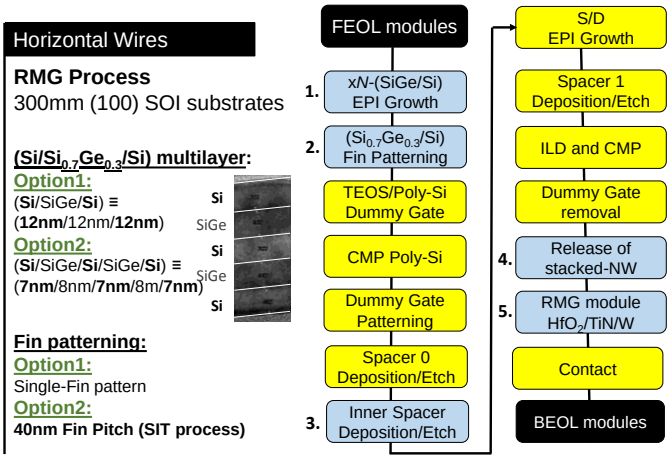

Fig. 1. Process flow of stacked wires FETs. Inner spacers and SiGe:B raised-S/D are used. The Ge concentration in the SiGe layers is around 30%. High density Fin patterning (FP=40nm) is obtained by a SIT process. The steps numbered '**1**' to '**5**' are specific technical requirements for stacked wires FETs (as compared to FinFET devices).

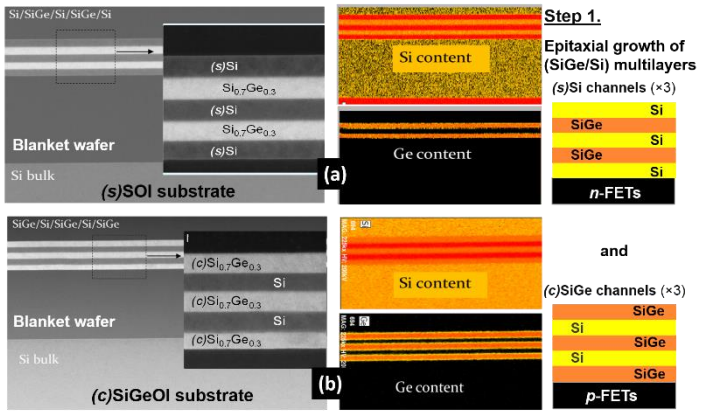

Fig. 2. TEM images and EDX spectroscopy maps of (Si/SiGe) superlattices with **(a)** ×3 levels of tensile strained Si layers (for *n*-FETs) and **(b)** ×3 levels of compressive strained SiGe layers (for *p*-FETs) stacked upon one another.

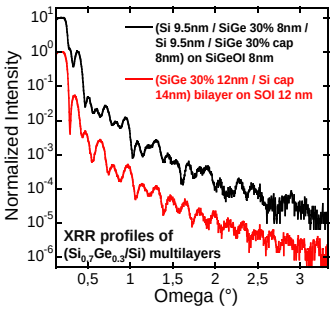

Fig. 3. XRR profiles of ($Si/Si_{0.7}Ge_{0.3}$) multilayers. Well-defined thickness fringes are present up to high incidence angles, showing a smooth surface interfaces and allowing thicknesses measurements.

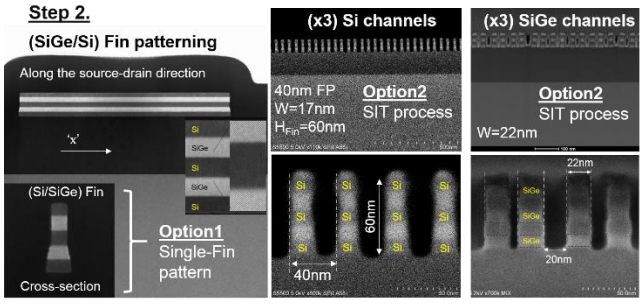

Fig. 4. Cross-sectional TEM images after etching of (Si/SiGe) fins in the longitudinal and transverse directions of futures Si (or SiGe) wires). Two types of fins patterning were used: **(Left)** single-Fin process and **(Right)** dense arrays of fins with a SIT process. Our SIT-based patterning technique yields 40 nm-pitch fins which are 60 nm high and 20 nm wide for both Si and SiGe channels.

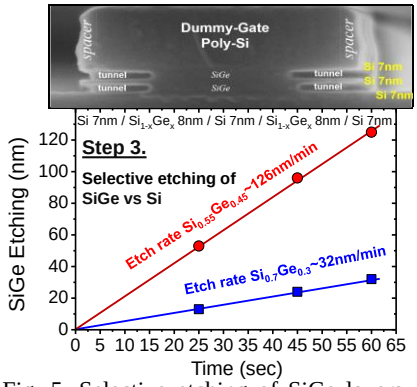

Fig. 5. Selective etching of SiGe layers. The Si and SiGe thicknesses are 7 nm and 8 nm, respectively. **(Top)** Cross-sectional SEM image showing the etch depth profile realized before the integration of inner spacers. **(Bottom)** SiGe etch depth *versus* time for 30% and 45% of Ge.

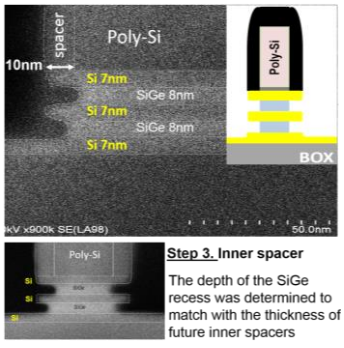

Fig. 6. Cross-sectional SEM images of stacked-NWs FETs prior to SiN inner spacers integration. The Si and SiGe thicknesses are 7 nm and 8 nm, respectively. The etching of SiGe layers stops at the same 'x' position than the spacer/poly-Si dummy gate interface.

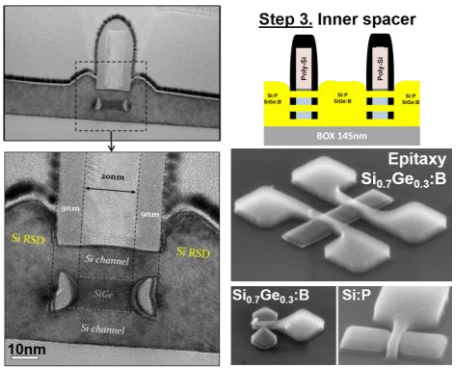

Fig. 7. **(Left)** Cross-sectional TEM images of stacked-NWs FET after the integration of inner spacers. The Si and SiGe thicknesses are 12 nm. **(Right)** 3D SEM images of stacked-NWs FETs after the source-drain epitaxy ($Si_{0.7}Ge_{0.3}$:B for *p*-FETs and Si:P for *n*-FETs). Inner spacers are well-aligned and correctly dimensioned.

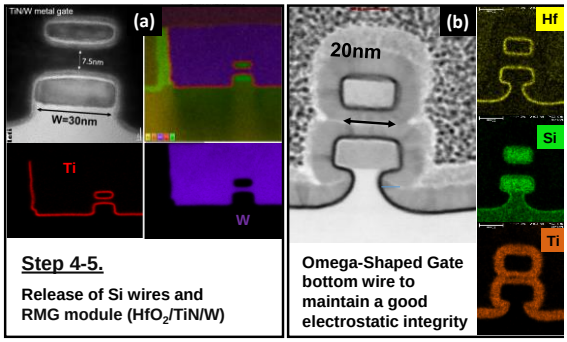

Fig. 8. **(a)** Cross-sectional TEM images and EDX maps of stacked wires FETs (HfO_2, TiN and W gate stack). Wire widths above 20 nm are used to improve the effective width W_{eff} and then enhance the drive current. An Ω-Gate Si channel is used for the bottom wire **(b)** to maintain a good electrostatic integrity. The deposition of high-k dielectrics (HfO_2) and metals (TiN/W) is conformal.

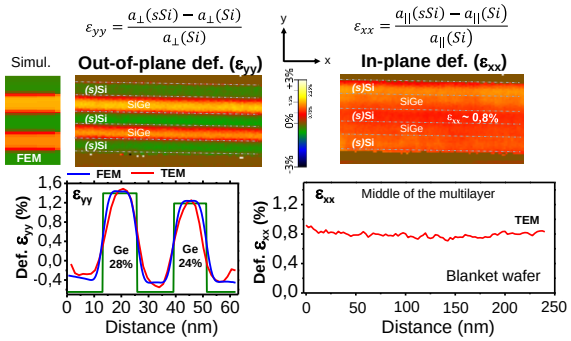

Fig. 9. **(Top)** Out-of-plane (ε_{yy}) and in-plane (ε_{xx}) PED deformation maps of (*SiGe/Si*) superlattices (**on blanket wafers**). Here, the growth was made on a *s*SOI (~1.4-GPa biaxial stress) substrate in order to have ×3 tensile strained Si channels for *n*-FETs. **(Bottom)** ε_{yy} and ε_{xx} profiles extracted in our sample from experiment (TEM) and simulations (FEM).

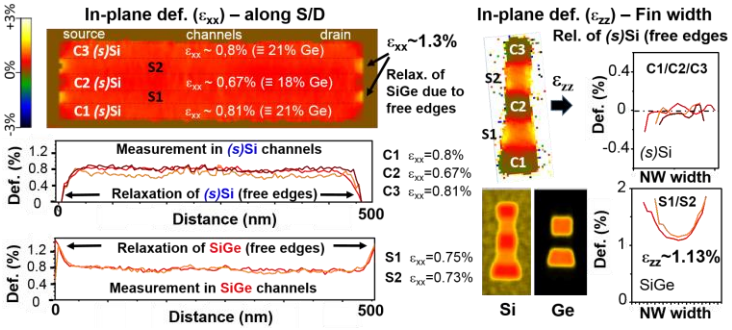

Fig. 10. **(Left)** In-plane (ε_{xx}) PED deformation maps of a (*SiGe/Si*) superlattices (**after Fin patterning**). The (*SiGe/Si*) stack is similar to that in Fig. 9. A deformation of around 0.8% in the *s*Si layers (×3) is kept corresponding to a stress of 1.4GPa after Fins patterning. **(Right)** Deformation map and profiles for ε_{zz}. Strain relaxation effects are observed in this direction due to free edges.

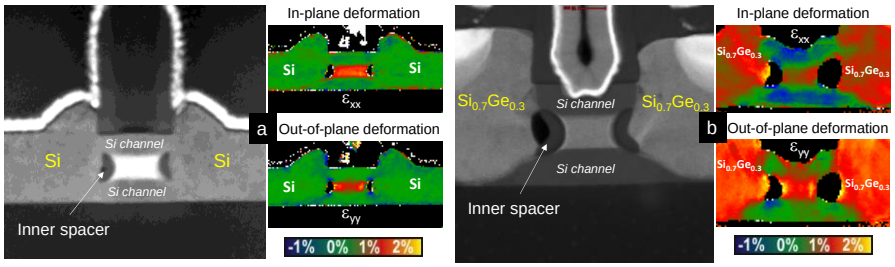

Fig. 11. HAADF STEM images of stacked-NWs *p*-FETs and deformation maps acquired by PED in the (ε_{xx}) and (ε_{yy}) directions. A spatial resolution of about 1.5 nm is achieved. Strain is measured **after Si (a)** and **$Si_{0.7}Ge_{0.3}$:B (b) S/D epitaxy**. For Si S/D, no strain is generated into Si *p*-channels. However, recessed and epitaxially regrown $Si_{0.7}Ge_{0.3}$:B S/D junctions clearly inject a significant amount of compressive strain in top and bottom Si *p*-channels. A compressive strain close to 1% (in blue color) is clearly visible.

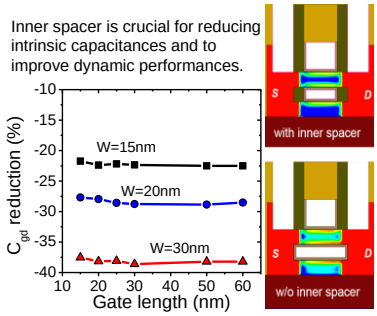

Fig. 12. TCAD simulations showing the reduction of parasitic gate-source/drain capacitances with inner spacers.

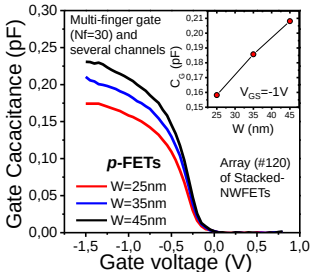

Fig. 13. Gate capacitance *vs* V_{GS} for stacked-NWs *p*-FETs with W=25-45nm. Here, L_G=500nm.

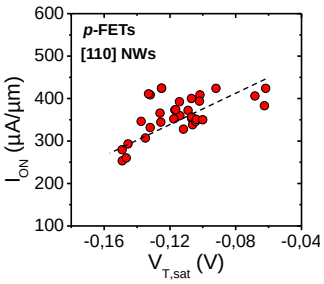

Fig. 14. I_{ON} *vs* $V_{T,sat}$ for stacked-NWs *p*-FETs with W=25-35nm at V_{DD}=0.9V. 25nm<L_G<70nm.

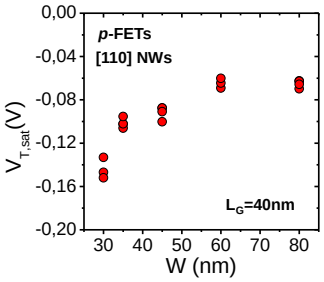

Fig. 15. $V_{T,sat}$ *vs* W for stacked-NWs *p*-FETs with L_G=40nm at V_{DD}=0.9V.

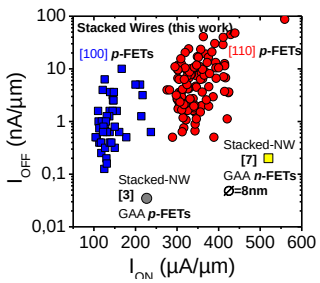

Fig. 16. I_{ON}/I_{OFF} plot of [100] and [110] stacked-NWs *p*-FETs with W=20nm-30nm at V_{DD}=0.9V.

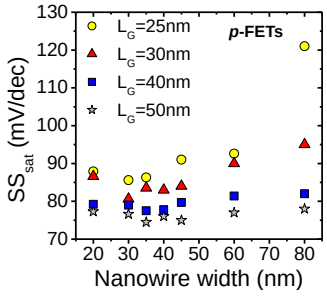

Fig. 17. Subthreshold slope *vs* wire width (W) for stacked-NWs *p*-FETs with 25nm≤L_G≤50nm.

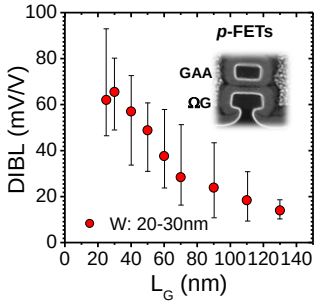

Fig. 18. Median DIBL *vs* gate length (L_G) for stacked-NWs *p*-FETs with W=20nm-30nm.

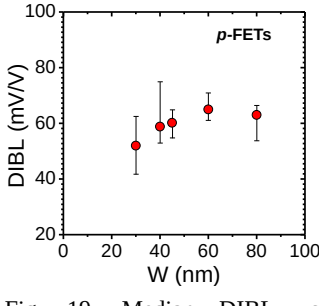

Fig. 19. Median DIBL *vs* nanowire width (W) for stacked-NWs *p*-FETs with L_G=40nm.

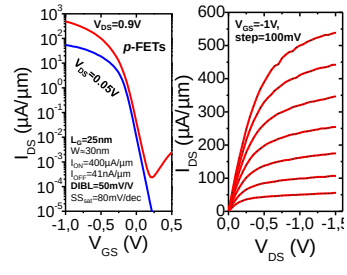

Fig. 20. I_{DS}-V_{GS} and I_{DS}-V_{DS} characteristics of stacked-NWs *p*-FETs with L_G=25nm. Here, W~30nm.