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High Gain and Fast Detection of Warfare Agents Using Back-Gated Silicon-Nanowired MOSFETs

Vikram Passi, Florent Ravaux, Emmanuel Dubois, Simon Clavaguera, Alexandre Carella, Caroline Celle, Jean-Pierre Simonato, Luca Silvestri, Susanna Reggiani, Dominique Vuillaume, and Jean-Pierre Raskin

Abstract—The top-down fabrication of doped p-type silicon-nanowired (NW) arrays and their application as gas detectors is presented. After surface functionalization with 3-(4-ethynylbenzyl)-1, 5, 7-trimethyl-3-azabicyclo [3.3.1] nonane-7-methanol molecules, the wires were subjected to an organophosphorous simulant, and both static and dynamic measurements were performed. A current gain of 4×10^6 is obtained upon the detection of the subpart-per-million concentration of a nerve-agent simulant. This represents a four-decade improvement over previous demonstration based on nanoribbons, proving better sensing capabilities of NWs. Technology-computer-aided-design simulations before and after gas detection have been performed to gain insight into the physical mechanisms involved in the gas detection and to investigate the impact of the surface-to-volume ratio on sensor sensitivity.

Index Terms—Gas detection, metal-oxide-semiconductor field-effect transistors (MOSFETs), silicon nanowires (NWs), silicon surface functionalization.

I. INTRODUCTION

BENEFITING from properties such as a large surface-to-volume ratio, extreme sensitivity to gas sensing, and finite charge-carrier concentration, which can be significantly influenced by surface states, the fabrication of nanowires

(NWs) for sensing applications is gaining increased attention in research. The exposed surface of NWs can be modified to act as both an electron-transfer mediator and an immobilizing matrix for biological or chemical molecules [1]. Taking advantage of the above properties, NW-based devices are the best candidates for gas detection [2]–[4], bioanalytical applications [5], [6], and deoxyribonucleic acid detection [7], [8]. Recently, the use of silicon nanoribbons (NRs) as nerve agents/organophosphorous (OP) detectors has been reported [5], where the NRs are grafted with 3-(4-ethynylbenzyl)-1, 5, 7-trimethyl-3-azabicyclo [3.3.1] nonane-7-methanol (TABINOL) and exposed to diphenyl chlorophosphate (DPCP), which is used as a simulant of nerve agents, thus forming aza-adamantane quaternary ammonium salt [5]. Due to their strong similarities with NRs, devices realized with arrays of silicon NWs are particularly fascinating for sensing applications as they increase the surface-to-volume ratio of the detector. The NW-based sensors are expected to show a stronger dependence of the carrier concentration on surface-charge modification, thus inducing a significant change in the device conductance. In this letter, we propose a top-down fabrication process for an array of ten p-doped NWs starting from a silicon-on-insulator (SOI) substrate. After surface functionalization with TABINOL, whose high selectivity to DPCP has been demonstrated already [5], the wires are exposed to the vapors, and electrical measurements are performed. An increase larger than six orders of magnitude in the current level after the DPCP exposure is observed, improving the performance of the device compared with the NR structures. In addition, numerical simulations have been carried out, which clearly show the impact of surface-charge modifications in the detection phase for varying NW widths.

II. DEVICE FABRICATION AND DESCRIPTION

The detailed processing of the NWs can be found in [9]. The starting material is a lightly positive-doped ($10 \Omega \cdot \text{cm}$) SOI layer of 50 nm in thickness. Fig. 1(a) shows the scanning-electron-microscopic (SEM) image of NWs after resist development. The top silicon is etched using chlorine chemistry, and the resist is removed by immersing the wafer in 1% HF. Platinum contacts are subsequently structured in the source/drain (S/D) regions after boron ion implantation and the activation anneal. The channel region was masked during this step. After inspecting the wafer by SEM [see Fig. 1(b)], the annealing of the metal is completed to produce a 40-nm-thick PtSi layer. An

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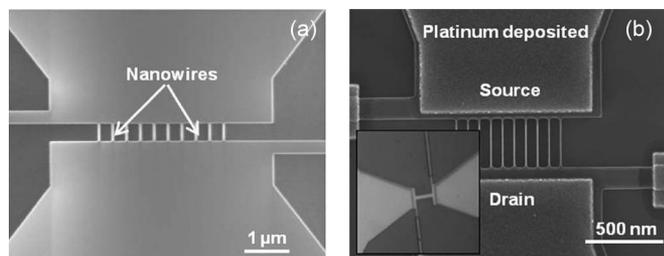


Fig. 1. Top-view SEM image of silicon NWs. (a) After resist development. (b) After the lift-off process of platinum on the source and drain pads. The inset in (b) shows an NR with metal contacts. The width of the NWs is 25 nm, whereas the NR is 1- μ m wide.

array of ten NWs of width $W = 25$ nm, length $L = 300$ nm, and a spacing of 300 nm and an NR [see the inset in Fig. 1(b)] of $W = 1 \mu\text{m}$ and $L = 5 \mu\text{m}$ are fabricated on the same wafer, which is functionalized and measured. Considering the 1- μ m NR footprint width along with its two 50-nm-high sidewalls, an effective NR width of 1.1 μm is obtained. The same type of calculation gives an effective width of 1.25 μm for 10×25 -nm-wide NWs associated in parallel. A detailed description of surface functionalization and electrical characterization procedures can be found in [5].

III. RESULTS AND DISCUSSION

Fig. 2(a) shows the measured drain current as a function of the back-gate voltage (V_{BG}) characteristics for the array of NWs and the NR before and after the DPCP exposure. In a typical experiment, two drops of DPCP were deposited carefully on a glass substrate (e.g., a watch glass) in the vicinity of sensors, so that the chip was not in direct contact with the OP simulant but only exposed to the vapors. It has been shown that the DPCP vapor pressure was estimated in the 500–800-part-per-billion range, as reported in [10]. The NW-based device clearly shows both an enhanced shift of the characteristic toward more positive V_{BG} and a higher maximum current increase with respect to the NR, when exposed to the gas. This represents an improvement of approximately four decades over the previous demonstration of OP detection based on NR devices published in [5]. Devices developed in this letter feature highly doped S/D regions and PtSi contacts that produce an extremely low extrinsic contact resistivity. This explains the large improvement in detection gain because the device architecture used in [5], which is based on Ti/Au Schottky S/D contacts on lightly doped silicon, suffers from very large metal/silicon-interface resistance. Table I provides a direct comparison of NW-based sensors to their NR counterpart fabricated with the same technological process. When compared with the NR counterpart, the NW sensors feature both the enhanced threshold-voltage shift ΔV_T and the larger relative change in current $(\Delta I/I)_{\text{peak}}$ upon exposure to DPCP, resulting in much larger detection margins, as outlined in Table I.

The observed current change after the DPCP exposure could be mainly due to: 1) the creation of a net charge in the molecules that act as an effective top gate [11], 2) the change in the density of silicon surface states [12], [13], and 3) the charge transfer between silicon and surface molecules, leading

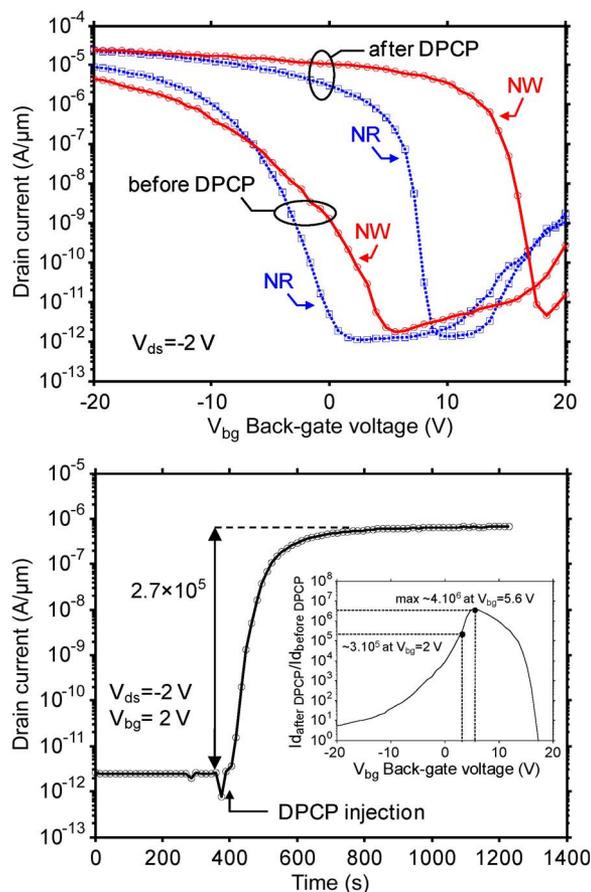


Fig. 2. (a) Measured I_{DS} - V_{BG} characteristics of NW- and NR-based devices before and after the DPCP exposure. (b) Measured time-dependent step increase in current in NWs during the injection of DPCP with an amplification factor larger than 3×10^6 . The static current gain after exposure to DPCP presented in the inset shows that the $V_{BG} = 2$ V bias condition for time-dependent measurement is slightly below the maximum gain of 4×10^6 obtained at $V_{BG} = 5.6$ V.

TABLE I
COMPARISON OF NR- AND NW-BASED SENSORS
FABRICATED IN THIS LETTER

Parameter	Nanoribbon (NR)	Nanowires (NWs)	Ratio NWs/NR
$V_{T \text{ before DPCP}}$ (V)	-8.8	-8.3	N/A
$V_{T \text{ after DPCP}}$ (V)	7.5	16.7	N/A
ΔV_T (V)	16.3	25	$\times 1.53$
$(\Delta I/I)_{\text{peak}}$	1.60×10^6	4×10^6	$\times 2.46$
$V_{bg \text{ peak}}$ (V)*	2.2	5.6	N/A

* Back-gate voltage at which $(\Delta I/I)_{\text{peak}}$ is extracted.

to interface dipoles and change in the silicon surface potential [14]. Following [5], the first two effects aforementioned can be precluded, and the charge transfer from the silicon substrate to the molecular layer upon gas exposure is considered as the main effect playing a role. In order to understand the physical mechanisms that are dominant in the NWs and the NR when exposed to DPCP vapors, 2-D and 3-D technology-computer-aided-design (TCAD) simulations of the NR and of the arrays of NWs, respectively, have been performed with the Sentaurus Device by Synopsys. Poisson's equation coupled with the drift-diffusion transport model has been solved to obtain the drain current with the varying back-gate voltage V_{BG} .

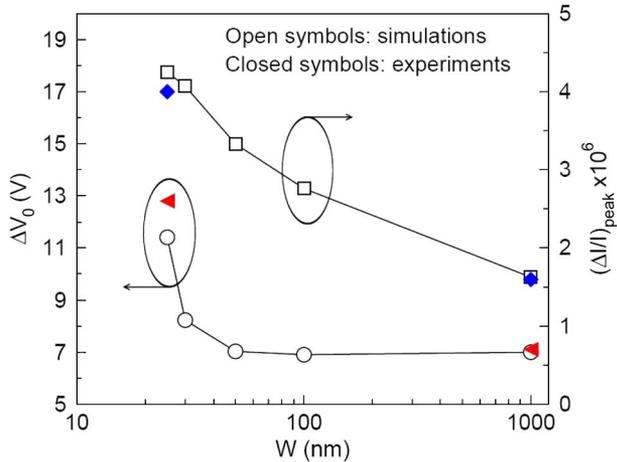


Fig. 3. Simulated maximum drain-current variation and back-gate voltage shift after the DPCP exposure as a function of device width.

In Fig. 3, the effect of the surface-to-volume ratio on sensor sensitivity in terms of the current curves shifts toward positive V_{BG} (ΔV_0), and $(\Delta I/I)_{peak}$ is shown as a function of the NW width. In [5], V_0 was defined as the V_{BG} value corresponding to the minimum current. Since here, the minimum current is not always well defined as in the NR case [see Fig. 2(a)], and V_0 is extracted by imposing $I_{ON}/I_{OFF} = 6 \times 10^6$, where I_{ON} is taken at $V_{BG} = -20$ V. Assuming that electrons are transferred from the silicon substrate to the molecular layer after the DPCP molecules have reacted with the TABINOL monolayer [5], [13], fixed negative charges at the silicon/molecular-layer interface are introduced in the simulations in order to emulate their effect. The negative interface charge sustains a corresponding accumulation of holes in the device, leading to the positive shift of the threshold voltage. The concentration of negative charges has been fixed to reproduce the experiments relative to the NR (see Fig. 3), and it is found to be $1.93 \times 10^{12} \text{ cm}^{-2}$, in agreement with values from the literature [5], [13]. Keeping the interface configuration unchanged, the simulations of devices with different widths have been carried out. ΔV_0 is increased when considering small widths as 2-D effects play a significant role in modulating the electrostatic control of the device. In addition, a degradation of the subthreshold slope is observed, which is induced by the additional coupling between the back-gate field and the NW sidewalls. The $(\Delta I/I)_{peak}$ curve shows a dependence approximately $\propto (1/H + 1/W)$, where H and W are the height and the footprint width of the NWs, respectively. The latter is due to the relative variation of charges within the device (from a subthreshold to an accumulation condition), accounting for the effect of the fixed charge at the exposed interfaces. Although a slight mismatch between simulation and experimental results is observed, which is likely due to variations of the silicon/surface-interface characteristics, Fig. 3 clearly shows that the sensor performance can be improved by reducing the NW width, particularly when W is shrunk below 50 nm.

IV. CONCLUSION

Single-crystal doped silicon NWs are fabricated on a SOI substrate by a top-down approach using electron beam lithography. The functionalization of NRs and NWs with TABINOL is performed, and after functionalization, the wires are exposed to DPCP. Change in the characteristics with a sharp detection of gas is observed. Better sensitivity is obtained for the NW structure together with an important area saving. The 3-D TCAD simulations of NWs with different widths before and after gas exposure have been performed, and the impact of the surface-to-volume ratio on sensor characteristics is demonstrated. By reducing the wire width from 1 μm down to 25 nm, the sensitivity of the silicon-based gas sensor is slightly improved, but more importantly, the V_{BG} window in which this extremely high sensitivity is reached is significantly enlarged.

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