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Self-optimisation using runtime code generation for Wireless Sensor Networks

Internet-of-Things Symposium
ESWeek Amsterdam

Caroline Quéva    Damien Couroussé
Henri-Pierre Charles

Univ. Grenoble Alpes, F-38000 Grenoble, France
CEA, LIST, MINATEC Campus, F-38054 Grenoble, France
### Classical Compiler architecture: GCC, LLVM, Java JIT

- Driven by performance only
- Mono architecture
- Not energy aware
- Not data dependent

### “Compilation time” typology

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<th>Execution</th>
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</tbody>
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#### Transformations Phases

- Loop Unrolling
- Address computation
- Strength reduction
- Register Allocation
- Code generation

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Intro Compilers

Future Compilers Architecture

- Multi objective (execution time, power, thermal constraints)
- Multi-target (Heterogeneous multi SoC)
- Data driven (dynamically)

Using “Compilation time”

Designers, programmers, optimizers, and users are involved in the compilation process. The diagram illustrates the various phases of code generation and optimization, including loop unrolling, strength reduction, register allocation, and address computation.

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Definitions

Static compilation  “classical” binary code generation (gcc, icc, clang, ...)

Dynamic Compilation  binary code generated at run-time (DBT)

  JIT  run-time dynamic compilation based on complex Intermediate representation (Java, LLVM)

Innovations

  Compilette  : small binary code generator embedded into application able to optimize code depending on data sets

  deGoal : a tool which help to generate Compilettes
## Supported architectures

<table>
<thead>
<tr>
<th>Architecture</th>
<th>Stat.</th>
<th>Features</th>
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<tbody>
<tr>
<td>ARM Cortex-A &amp; M, [T2, VFP, NEON]</td>
<td>✔</td>
<td>SIMD, [IO/OoO]</td>
</tr>
<tr>
<td>STxP70 (STHORM / P2012)</td>
<td>✔</td>
<td>SIMD, VLIW (2-way)</td>
</tr>
<tr>
<td>K1 (Kalray MPPA)</td>
<td>✔</td>
<td>SIMD, VLIW (5-way)</td>
</tr>
<tr>
<td>PTX (CUDA Asm language)</td>
<td>✔</td>
<td></td>
</tr>
<tr>
<td>ARM32</td>
<td></td>
<td>32 bits</td>
</tr>
<tr>
<td>MIPS</td>
<td>✔</td>
<td>Up to &lt; 1kB ram</td>
</tr>
<tr>
<td>MPS430 (TI)</td>
<td>✔</td>
<td></td>
</tr>
</tbody>
</table>

- Cross code generation supported (generate code for STxP70 from ARM Cortex-A)
- IO / OoO: different insn scheduling for both mode
Simple program example:

```c
void gen_vector_add(void *buffer, int vec_len, int val)
{

    // Begin buffer Prelude vec_addr
    Type int_t int 32 #(vec_len)
    Alloc int_t v
    lw v, vec_addr
    add v, v, #(val)
    sw vec_addr, v

}
```

Source to source converted to standard C code

Standard C code
Writing a compilette with deGoal

Simple program example:

```c
void gen_vector_add(void *buffer, int vec_len, int val) {
    // Begin buffer Prelude vec_addr
    Type int_t int 32 #(vec_len)
    Alloc int_t v

    lw v, vec_addr
    add v, v, #(val)
    sw vec_addr, v
}

Memory:

ldr r1, [r0]
add r1, #1
str r1, [r0]
add r0, #4
ldr r2, [r0]
add r2, #1
str r2, [r0]
add r0, #4
```

When executed
Simple program example:

```c
void gen_vector_add(void *buffer, int vec_len, int val)
{
    #[
    Begin buffer Prelude vec_addr

    Type int_t int 32 #(vec_len)
    Alloc int_t v

    lw v, vec_addr
    add v, v, #(val)
    sw vec_addr, v
    ]#
}
```
Intro Architectures examples

Example MSP430

- LaunchPad Development Kit
- TI Micro controller
- 16-bit Ultra-Low-Power Microcontroller,
- 1KB Flash
- 128B RAM

Example STM32

- ST Micro microcontroller
- ARM Cortex-M 32 processor

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Code specialisation for arithmetic

- Micro-controllers lack dedicated HW support for arithmetic computing
  - No FP unit
  - Sometimes, even no integer multiplier!
- Illustration on floating-point multiplication,
  - But applicable to many other operations!

Example: simple float multiplication, compiled for TI’s MSP430

```c
float fmul (float a, float b) {
    return (a*b);
}
```

```
1  c630: mov r8, r12
2  c632: mov r9, r13
3  c634: mov r6, r14
4  c636: mov r7, r15
5  c638: call #0xc9d6 ; <__mulsf3>
6  c63c: mov r14, r12
7  c63e: mov r15, r13
8  c640: mov r10, r14
9  c642: mov r11, r15
```

- `__mulsf3` costs \(~1000\) cycles per invocation
**Experiment**

**Reference**

- gcc’s generic version of the float multiplication routine
- Precision $p = 24$

```c
/* tgcc */
float fmul (float M, float X) {
    return (M*X);
}
```

**Our approach**

- Runtime specialization of the float multiplication routine
- Precision $p \leq 24$

```c
1 /* tgen: code generation */
2 float (*) (float) fmulM;
3 fmulM = generate_fmul_code(M, p);
4
5 /* tdyn: run the generated routine */
6 float fmul (float X) {
7    return fmulM(X);
8 }
```

$t_{gcc}$ : execution time of gcc’s multiplication routine

$t_{gen}$ : execution time of code generation

$t_{dyn}$ : execution time of the generated $fmulM$ function
Performance indicators

t_{gcc} : execution time of gcc’s multiplication routine

t_{gen} : execution time of code generation

t_{dyn} : execution time of the generated fmulM function

Speedup :

\[ s = \frac{t_{dyn}}{t_{gcc}} \]  \hspace{1cm} (1)

Overhead recovering :

\[ n = \frac{t_{gen}}{t_{gcc} - t_{dyn}} \]  \hspace{1cm} so that \( t_{gen} + n.t_{dyn} \leq n.t_{gcc} \)  \hspace{1cm} (2)
FP Multiplication algorithm (X, Y)

- Special case handling (denormal, zero, NaN)
- Unpack X, Y
- Mantissa multiplication
- Renormalize
- Repacking
- Rounding

Optimization potential

- Skip unnecessary steps
- Value specialization
ALGORITHM 1: Floating-Point Multiplication with Horner scheme

Input: Floating-point operands $M$ and $X$ to be multiplied ($M$ is known, $X$ is unknown).

Output: The result $M \times X$ of the multiplication.

\[
\begin{align*}
i &\leftarrow 0; \\
detection &\leftarrow 1; \\
result &\leftarrow X; \\
\textbf{while not} \ (\text{mantissa}(M) \ \&\& \ (1 \ll i)) \ \textbf{do} \\
| \quad i &\leftarrow i + 1; \\
\textbf{end} \\
\textbf{for} \ i &\leftarrow i + 1 \ \textbf{to} \ \text{len(mantissa}(M)) \ \textbf{do} \\
| \quad \textbf{if} \ \text{mantissa}(M) \ \&\& \ (1 \ll i) \ \textbf{then} \\
| \quad| \quad \quad \text{result} &\leftarrow (\text{result} \ll detection) + X; \\
| \quad| \quad \quad \text{detection} &\leftarrow 1; \\
| \quad \textbf{end} \\
| \quad \textbf{else} \\
| \quad| \quad \quad \text{detection} &\leftarrow \text{detection} + 1; \\
| \quad \textbf{end} \\
\text{end} \\
\text{result} &\leftarrow (\text{result} \ll \text{detection}); \\
\textbf{return} \ \text{result}
\end{align*}
\]
Results

Speedup

Overhead recovering
Conclusion for multiplication

- Demonstration that runtime code generation is a realistic goal
  - on a 16-bit micro-controller
  - with only 512 bytes of RAM
- Efficiency: $10 \times$ faster floating-point multiplication (when one of the two operands is a runtime constant)
- Greater genericity: extra flexibility on precision
- 50% increase performance on an IIR application (7 coeff.)
- Further work: automatic runtime code generation embedded in libm
Future works

In IoT
- Generalize the arithmetic library
  - Other operators (trigonometry, ...)
  - Network stacks

Other domains
- High Performance Computing
- Power Consumption driven
- Code polymorphism
  - Online optimization
  - Cryptography