Radiation Hardened MRAM-Based FPGA

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Field-programmable gate arrays (FPGAs) are mainly composed of memory cells which store the configuration data defining the implemented functionality of the circuit. Today, advanced memories are facing a number of issues such as increased static power consumption and radiation sensitivity. These can be solved by the use of a new memory technology: magnetic random access memory (MRAM) [1]. It combines the reliability against radiation induced soft errors, the non-volatility of Flash memory, fast writing cycle, and the endurance of static random access memory (SRAM). MRAMs therefore appear as a good candidate for replacing today's memories in FPGAs [2]. To take advantage of all of its assets, a new FPGA architecture has been designed by taking into account all the specificities of MRAMs. This paper presents a silicon proven innovative MRAM-based look-up table (LUT) intended for space applications. It has been designed to validate the concept and measure the performance. It combines MRAM and dynamic logic for lower power consumption while increasing density and reliability to soft errors.

***Index Terms*—Dynamic random access memory (DRAM), field-programmable gate array (FPGA), look-up table, magnetic random access memory (MRAM), magnetic tunnel junction, radiation hardening, scrubbing, soft error.**

I. Introduction

ONE of the main issues in current static random access memory (SRAM)-based field-programmable gate arrays (FPGAs) is the radiation sensitivity of SRAM cells in advanced technology nodes. To solve this, one of the solutions is to check and write periodically the configuration memory to correct soft errors that may have occurred; it is called scrubbing. Then, SRAM FPGAs need an external non-volatile memory to store the configuration data which increases the area of boards. A domain where these constraints are critical is space domain. The use of magnetic random access memory (MRAM) memory cells can be a solution to overcome these specific constraints in space applications. This paper presents an innovative look-up table (LUT) composed of MRAMs and intended for space applications. It combines MRAM and dynamic random access memory (DRAM) memories to make a non-volatile, radiation hardened and dense FPGA.

The paper is organized as follows. Section II describes MRAM memory cells. Section III describes classical architecture of an FPGA and particularly the role of its memory cells. Section IV describes the innovative FPGA architecture. Section V shows some results of the silicon demonstrator. Then, we conclude on the use of MRAM cells for FPGAs.

II. MRAM Description

The basic element of MRAM is the magnetic tunnel junction (MTJ, Fig. 1), a nanostructure basically composed of two ferromagnetic (FM) layers separated by an insulating layer. The magnetization of one layer is fixed while that of the other layer (storage layer, SL) can be switched between two stable positions depending on the data to be written. The digital information stored in the MTJ is represented by its resistance level,

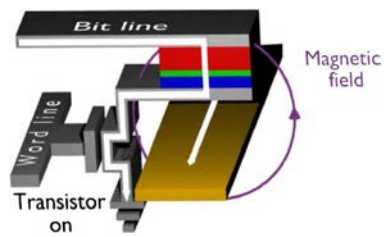

Fig. 1. TAS writing scheme.

which changes according to the relative magnetization of the two layers. Reading the memory state consists in measuring this resistance, typically by comparing the current through the MTJ to a reference current. Writing the information consists in switching the magnetization orientation of the SL, using a pulse of magnetic field or spin polarized current through the junction [3]. The demonstrator has been designed with thermally assisted switching (TAS) MRAMs [4]. In this technology, the MTJ is temporarily heated during write by a pulse of current flowing through the MTJ. This heating releases the SL magnetization, thus enabling writing at a lower field. This approach significantly lowers the write power consumption in comparison to the toggle MRAM. The TAS MRAM has been developed by Spintec and Crocus Technology. It is very suited for space applications thanks to its thermal stability and radiation hardness.

III. FPGA Description

A. FPGA

An FPGA is a programmable digital component. It can implement any digital function if it is complex enough. It is composed of a matrix of LUTs. An LUT is a simple circuit that can compute any simple digital function. For example, Fig. 2 shows a 3-input LUT. It is composed of a multiplexer (MUX) and memory cells connected to it. The 3 inputs , , and select the memory cell whose content is routed to the output S. In the example, if the input code is "001", the memory cell at the address "001" is selected and the output S is in the 0 logic state. If the input code is "111", then the output is in the 1 logic

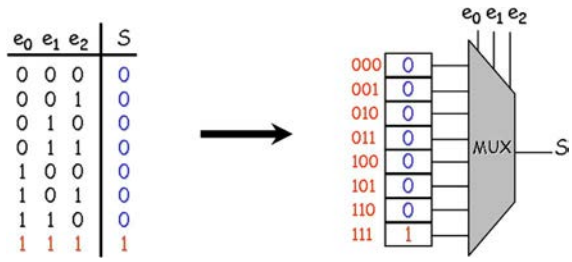

Fig. 2. 3-inputs look-up table example implementing an AND logic function.

state. To implement a function, the truth table has to be directly written in the memory cells at the correct addresses.

To make a complex function, such as an adder or a multiplier, several LUTs are connected together with programmable interconnects. A programmable interconnect is simply made of a transistor connected to two lines, which is controlled by a memory cell connected to its gate, and that can be activated or not whether the two lines has to be connected or not.

In an FPGA, between 50% and 80% of silicon area is constituted by the interconnection network [5] and it contributes to dynamic power consumption between 60% and 80% [6]. That is why the choice of the configuration memory technology is important. Indeed, SRAM cells are composed of at least 5 transistors, so most of the surface of an FPGA is composed of memory cells.

B. Radiation Induced Errors in FPGAs

Circuits used in space systems are influenced by particles such as high energy protons, electrons, gamma, and X-rays. These particles, when they go through a circuit, hit the silicon and generate electron-hole pairs. When these pairs are under an electric field, at the drain of a deactivated transistor, the electrons and holes are separated and a current is generated. The pulse of current, in the order of hundred of picoseconds, can change the state of a transistor and create an error in the circuit and in the end a malfunction at the system level, that can be dangerous according to the circuit's functionality. The errors do not damage physically the circuit and disappear quickly, so they are called soft errors.

Memory cells are particularly sensitive to soft errors because a particle can change their content and hence lead to permanent error of the memory unless it is corrected. This is a problem, particularly in the case of FPGAs because if the content of a configuration memory is changed, the functionality of the FPGA is modified and can cause an error at the system level. To avoid this, SRAM-based FPGA can use a technique called scrubbing which consists in reading and checking the configuration memory periodically to detect and correct configuration errors that may have occurred. This technique avoids the accumulation of errors in the circuit.

IV. New Architecture

The LUT we propose combines MRAM and DRAM memories (Fig. 3). The configuration memories connected to the multiplexer are made of a capacitance that stores the configuration data and a selection transistor. It is the active part of the circuit as it is computing when the FPGA is in operation. The data

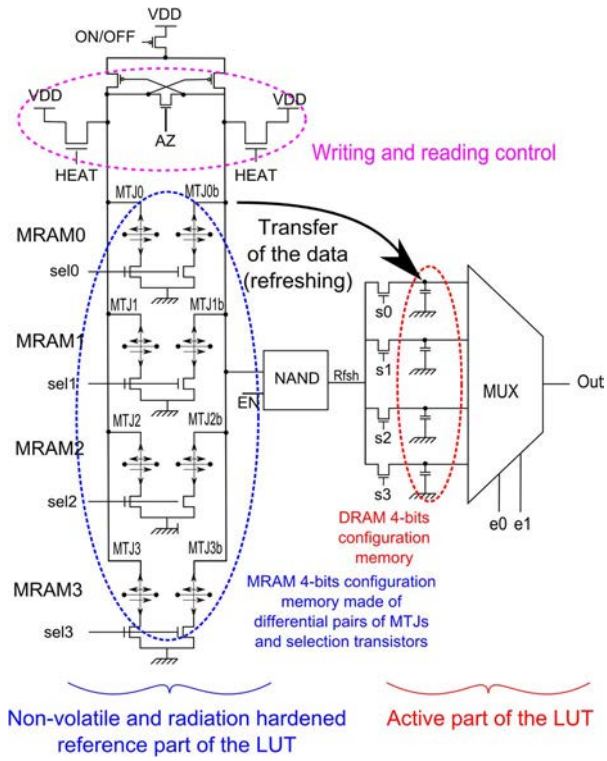

Fig. 3. Schematic of the proposed LUT architecture.

are refreshed periodically thanks to an MRAM block in which each cell is composed of two MTJs operating in differential mode. The configuration is stored permanently since MRAM are non-volatile and reliable because MTJs are immune to radiation. That is why this part is called reference part. Moreover, the power supply of the MRAM block can be switched off between two refreshing phases to decrease power consumption. Thanks to the refreshing phase, every possible error in the configuration memories is corrected. The refresh phase replaces the scrubbing technique in SRAM-based FPGA so it does not add power consumption to the circuit compared to the same circuit implemented in an SRAM-based FPGA.

A pending patent [7] describes an FPGA based on DRAM memory cell refreshed by an external ROM memory component. In our case, the use of MRAM allows a local implementation of the non-volatile memory. The power consumption is reduced as it is a local memory and there is the possibility to switch off LUT and interconnection circuits that are not used. So we can optimize the power consumption of the circuit.

V. Demonstrator

The demonstrator was fabricated using an industrial hybrid CMOS/magnetic manufacturing process developed by TowerJazz and Crocus Technology. The circuit implemented is a 2-input LUT as illustrated in Fig. 3. It comprises 4 configuration memory cells. Each memory cell is composed of a capacitance made of the parasitic capacitance of a transistor. The corresponding MRAM memory cell is composed of two MTJs in opposite states. In this way, the reading phase is differential and more reliable. Figs. 4 and 5 show, respectively, a picture of the test chip and the layout of the circuit with its different parts. Its

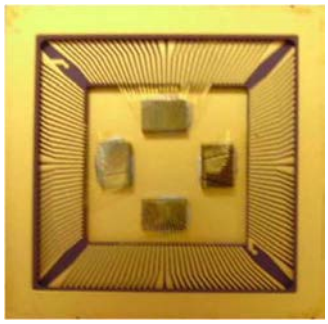

Fig. 4. Picture of the silicon demonstrator.

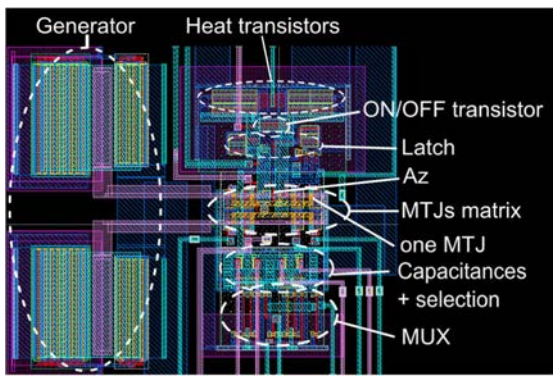

Fig. 5. Layout of the demonstrator.

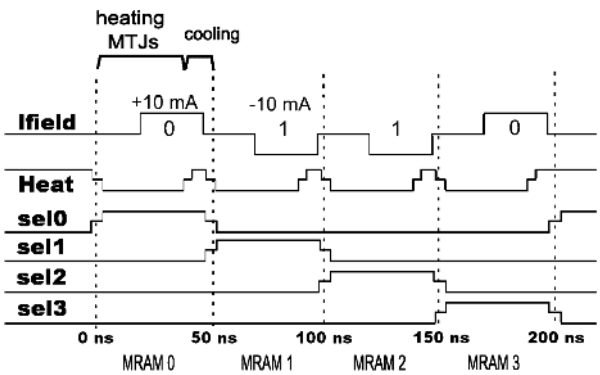

Fig. 6. Programming phase.

area is 1520 μm^2. Most of the area is composed of the current generator and the reading circuit. However, their surface can be neglected for bigger LUT because they are shared between several MTJs.

An XOR function was first implemented. The corresponding truth table was first written in the MTJs. The capacitances were then refreshed and eventually the LUT was tested by applying all its input codes. The tests showed that these different steps are successfully achieved. First, the programming phase (Fig. 6) has been tested. The XOR function is written in the MRAM block. Each MRAM is selected sequentially (signals "sel0" to "sel3"). For each MTJs selected, the "Heat" signal is set to "0" to heat them. Then, it is set to "1" to stop the heating. The current to produce the magnetic field "Ifield" is applied at the end of the heating period for about 15 ns corresponding to the duration of the cooling phase.

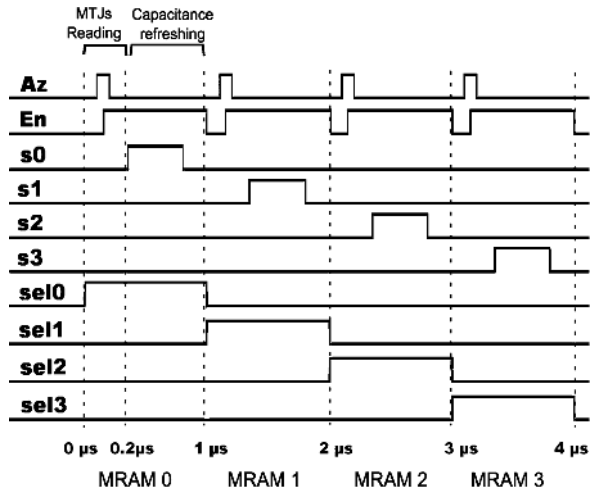

Fig. 7. Refreshing phase.

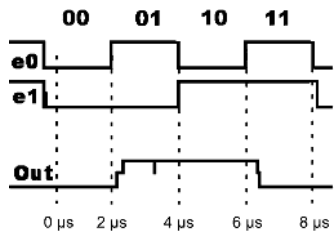

Fig. 8. LUT in operation.

Then, the refreshing phase is tested (Fig. 7). Each MRAM cell and each capacitance is selected sequentially (signals "sel0" to "sel3" and "s0" to "s3" successively). Each time, the latch is updated to read the MRAM selected. The "EN" signal is activated to enable refreshing the capacitance with the data read, while the "AZ" signal is used to convert the convert the magnetic state of the MTJs into electrical information.

The next step is to test that the LUT is implementing the correct function. The test vectors of this test and the result are presented in Fig. 8. All the inputs ("e0", "e1") codes are displayed. We see that the function XOR is successfully executed.

Fig. 9 shows a dynamic reconfiguration of the LUT. It means that the function implemented by the LUT is changed when the circuit is in operation. The old function was "0010" and is reconfigured into the XOR function. All the possible functions have been implemented during the tests, meaning that 16 functions were tested successfully. It shows that the MRAM were written correctly. To test the non-volatility, the power has been shut down and then powered on again. After the refresh phase, the XOR function was still implemented demonstrating that the configuration memory is non-volatile. Fig. 10 shows a parametric test in which the pulse width and magnetic fields (by varying the power supply of the magnetic field driver) are changed. Four zones can be identified. In zone 1, the magnetic field and MTJ temperature are too low to correctly write the MTJ. In zone 2, the temperature is high enough but the field is too low. In zone 3, the field is large enough but the temperature is too low. In zone 4, the field and temperature are high enough to write correctly the MTJs. It shows that the test is successful when the pulse width is longer than 40 ns and the supply voltage

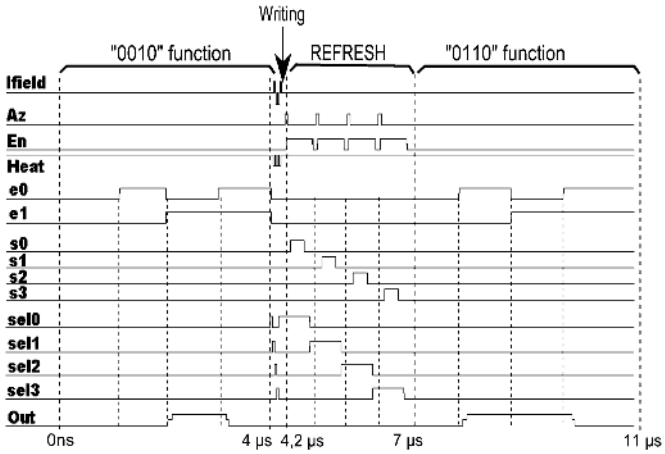

Fig. 9. Dynamic reconfiguration.

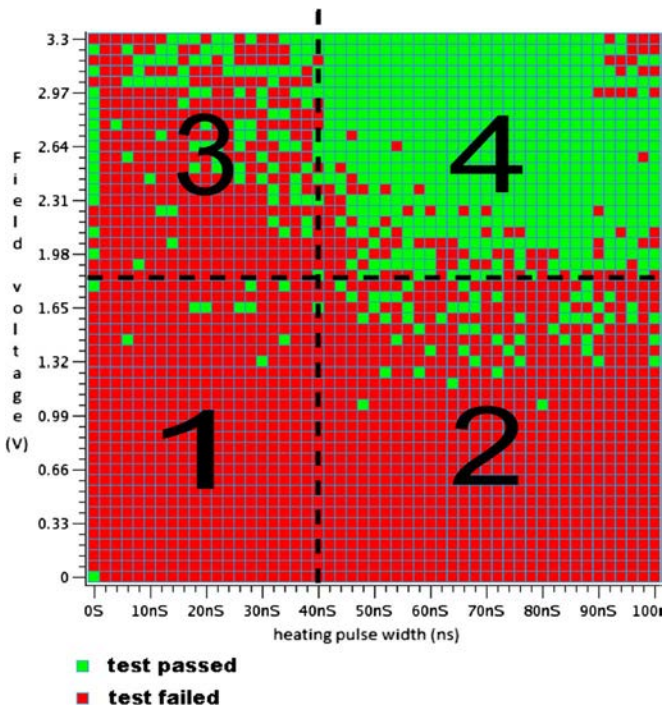

Fig. 10. Parametric passed/failed as a function of the supply voltage of the magnetic field driver and the heating pulse duration.

over 2.1 V. So, the minimum writing time is 55 ns (15 ns for the cooling phase) for one MRAM configuration memory. The writing power is 1.1 nJ for two MTJs.

Compared to Flash memories used in most of FPGA for space applications, MRAMs have a lower power consumption, are faster, and have a higher endurance [1]. In addition, MTJs have a high tolerance to total ionizing dose radiation [8] compared to Flash memories [9]. In comparison to SRAM FPGA, the scrubbing period is faster and can be applied more frequently. In addition, the circuit benefits from the radiation immunity of MTJs to correct every configuration soft error. The MRAMs are placed locally in the FPGA, whereas SRAM FPGAs need an external radiation hardened non-volatile memory. Hence, this new MRAM FPGA architecture is more reliable and has lower power consumption than Flash and SRAM-based FPGAs.

VI. Conclusion

An MRAM-based FPGA has been designed. It combines MRAM and DRAM to make a high density, low power, and radiation hardened FPGA. A 2-input LUT demonstrator has been designed with the Tower 130 nm technology for the CMOS layers and Crocus TAS MRAM technology for the magnetic layer. The test of the demonstrator has validated the concept of configuration circuit presented in this paper.

Acknowledgment

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