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ABSTRACT

This work presents the performance degradation of a 32-bit DSP fabricated with 28nm FDSOI technology subjected to different levels of gamma radiation. A new mixed hardening methodology based on electrical compensation and thermal regeneration is applied to the irradiated devices to recover the degraded electrical characteristics induced by the total ionizing dose. The application of this new methodology seeks to extend the lifetime of FDSOI integrated circuits under high radiation conditions while keeping good reliability.

1. Introduction

Fully-Depleted-Silicon-On-Insulator (FDSOI) technology has many advantages over conventional bulk ones such as an improvement in the operating frequency, low power consumption, low sensitivity to single event effects (SEE) and short channel effects (SCE) [1]. Several studies have focused on radiation-induced effects on FDSOI devices [2]. Physically, the total ionizing dose (TID) induces a buildup of charges likely to be trapped in the oxide layers of FDSOI transistors, namely the gate oxide, the buried oxide (BOX), and the shallow trench isolation (STI) oxide. This results in a negative threshold voltage shift, a subthreshold slope degradation and an increased leakage currents [3]. As a consequence, the TID impacts negatively the performance of the circuit resulting in a degradation of the operating frequency and more power consumption. Different hardening methods have been developed and applied to integrated circuits (ICs) over the years, such as shielding and radiation hardening by design (RHBD). These methods are applicable for FDSOI technology as well as bulk ones. They focus on preventing the effects of radiation. However, they do not recover the degraded electrical characteristics of the devices after being subjected to radiation.

In [4], we have proposed a new hardening methodology based on an electrical compensation and a thermal regeneration of FDSOI devices. The method applied to elementary FDSOI transistors has shown great results in the recovery of their electrical characteristics degraded by TID. In this work, we continue to prove the efficiency of this proposed mixed hardening strategy. We analyze the degradation induced by gamma radiation of a 32-bit DSP chip and we apply the mitigation strategy to restore its performance.

The paper is organized as follows: In Section 2, we briefly explain the principle of electrical compensation based on the electrostatic coupling effect inherent to FDSOI technology and the thermal regeneration method allowing the recovery of radiation-induced degradation. In addition, the concepts related to the operating frequency and power consumption of an IC will be explained. Then, the architecture of the circuit under test is presented. The experimental details are given in Section III. In Section IV, we present the radiation impact on the performance of the irradiated test-chip, the results of the applied mitigation strategy on the restoration of the device's performance in addition to a brief discussion regarding the possible applications of this methodology. Finally, concluding remarks are drawn in Section V.

2. Background

2.1. Mixed Thermal-Electrical hardening method

The method that we proposed in [4] is based on the regeneration-compensation principle intended to mitigate the TID effects on FDSOI devices. First, back-gate biasing is used to compensate threshold voltage shift and then thermal annealing is applied to recover the degradation of both threshold voltage and subthreshold slope. Back-gate biasing is an important feature of FDSOI technology that allows the modulation of the threshold voltage through electrostatic coupling between its two channel-oxide interfaces [5]. The threshold voltage of the front transistor V_{tf} changes when a back-gate voltage V_{bg} is applied according to the equation $V_{tf} = V_{t0} - nV_{bg}$ [6], where n is the coupling coefficient depending on the transistor capacitances and V_{t0} is the intrinsic threshold voltage of the device. This advantage has been exploited by the IC designers to improve the operating frequency at the expense of an increase in power consumption [6].

Depending on the type of substrate used, the FDSOI transistor can be either Low Vt (LVT) or Regular Vt (RVT). The LVT variant, depicted in Figure 1, is the subject of the current study. It is built in a flip well which means that NMOS transistors are seated on an N-well and that PMOS ones are seated on a P-well. This variant of transistors allows a great

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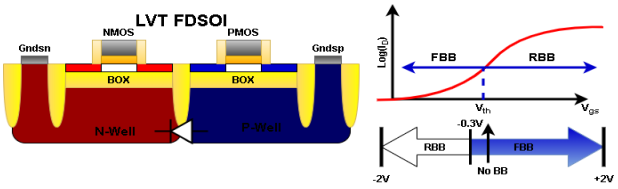

Figure 1: Cross-section of LVT FDSOI transistor.

range of negative threshold voltage shift through a strong forward body bias (FBB) but a short range of positive threshold tuning using reverse body bias (RBB).

Furthermore, the use of high temperatures for regenerating the electrical characteristics of irradiated devices has been previously studied in several works [7, 8]. In fact, the radiation-induced-trapped charge in the oxides can be evacuated very slowly at room temperature. Since this process is thermally activated, an increase in temperature accelerates the evacuation of charges. This phenomenon is commonly modeled by an Arrhenius law [9]. Hence, to reach certain activation energy, there is an equivalence between the time and the temperature of the annealing process. For instance, we will need a longer time at low temperature to reach the same activation energy as when annealing at high temperature during a short time. As high temperature accelerates aging mechanisms in semiconductors, appropriate annealing parameters, namely the couple (temperature, time) have to be chosen carefully to preserve the reliability of the devices.

2.2. *Description of the devices*

The device used for these experiments is a 32-bit DSP dedicated to Telecom applications [6]. It has been fabricated with STMicroelectronics 28nm FDSOI technology. The device includes the DSP and an automatic test harness as depicted in Figure 2. The DSP is designed with a Very Long Instruction Word (VLIW) architecture, which is well suited to Telecom applications. It is able to perform scalar and complex arithmetic operations and it embeds cordic/divide and compare/select functions. The architecture presents a pipeline depth of 10 stages in order to achieve more than 1.5 GHz at nominal voltage without using body bias. Two SRAM memories are used to feed the DSP core, one for the Program and the other for data interfaces. Each SRAM is organized in 1024 words of 32 bits.

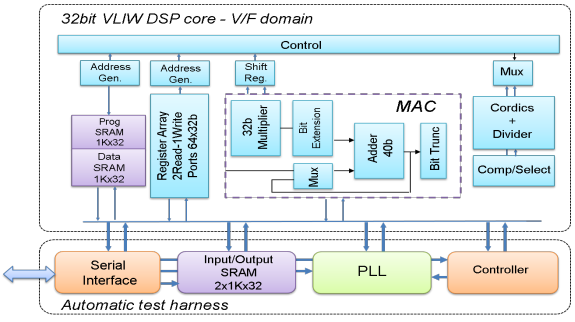

Figure 2: Block diagram of 32-bit DSP.

The automatic test harness is designed to drive the DSP core and to verify the correct result of every operation. Therefore, it is possible to detect the failure of the core and thus to measure the maximum clock frequency of the DSP in function of the applied voltage. The harness is composed of a Phase Locked Loop (PLL) clock generator, SRAM memories, a local controller, and an interface. The interface is used to drive the test harness from a PC. It uses multiple commands to configure the DSP, the PLL, and to read/write the SRAM memories. The PLL is used to generate the clock frequency to the DSP core. The PLL uses a dedicated different power supply pin to minimize the clock jitter, noise and to guarantee normal operation even when the core is at low voltage. The SRAM memories on the harness contain the expected result of each DSP operation. Therefore, if during the execution of the DSP, the computed result differs from the expected result, an external signal is risen signaling the detection of an error. The measurements of the circuit follow this sequence: 1) all SRAM memories are written, 2) the PLL is configured with the target frequency, 3) the voltage of the core is regulated to the target voltage, 4) the execution of the core is started, 5) the internal core results are collected. If the current test succeeds, the test is restarted with an increased frequency of 1 MHz. When the test fails, the frequency used for the previous test is considered as the maximum frequency of the circuit for the current applied voltage. A new frequency exploration campaign can be executed for different applied voltages where the PLL frequency is initialized to its minimum frequency. The circuit has been designed with LVT cells in order to achieve 2.6 GHz at 1.3 V when body bias is used. It contains multiple power domains to supply power and to measure the circuit consumption. The test board is equipped with stabilized voltage regulators and measurement capabilities to measure the internal voltage of the circuit and the power consumption. The measurement of the power consumption is automatically triggered by the board when the test is started.

3. Experimental details

Twenty-four 32-bit DSP fabricated with 28nm FDSOI LVT technology made by STMicroelectronics and the CEA-LETI were irradiated in the IRMA facility at Saclay, France, with a $^{60}Co\ \gamma - ray$ source. The devices were divided into four groups and placed at different dose-rate locations in the irradiation chamber to observe the degradation of their electrical characteristics. The dose was deposited in several steps to reach 128 kGy, 12.8 kGy, 19.8 kGy, and 3.5 kGy in groups 1 to 4, respectively (see Table 1). Three isochronous annealing cycles were applied to all devices for the regeneration of their characteristics, using temperatures of $T_1 = 200$ °C, $T_2 = 250$ °C and $T_3 = 300$ °C with a common duration Δt of 23 minutes. To observe the effect of radiation and temperature separately, this experiment was performed in radiation then annealing.

All devices were unbiased during irradiation and were measured at room temperature immediately after each radiation step and after each annealing cycle to observe their

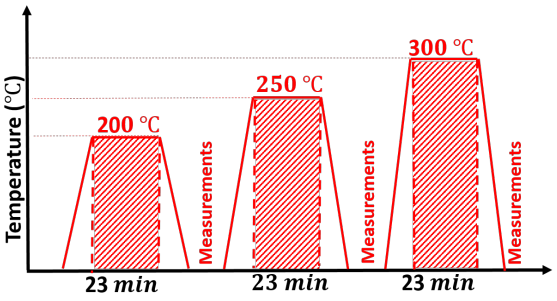

Figure 3: Annealing procedure.

progressive regeneration on the degraded performances of the devices. Radiation responses of integrated circuits differ depending on the biasing configuration during the radiation process. It has been reported in previous works [10, 11] that the worst response for FDSOI devices is when they are biased during irradiation. This can be explained by the fact that the applied electric field act to separate the electron-hole pairs created by ionizing radiation, preventing their prompt recombination. The most favorable case is the one carried out during our experiments where the devices are not subject to influence of a gate oxide electric field keeping the electron-hole pairs created by ionizing radiation relatively close, which is a favorable case for their prompt recombination. Even though, the goal of this work is to validate the proposed hardening methodology on the degraded DUTs.

The main measured parameters were the maximum operating frequency of the device f_{max} and the power consumption P both available on the test bench display shown in Figure 4. This test bench is able to make measurements by varying the supply voltage V_{dd} from 0.5 V to 1.3 V with a 0.05 V step and applying an absolute value to the back-gate between 0 to 2 V with a step of 0.5 V.

Figure 4: Test bench machine.

Table 1
Irradiation conditions

Devices	Dose-rate (Gy/h)	Duration (h)	TID(kGy)
Group 1 (G1)	800	160	128
Group 2 (G2)	80	160	12.8
Group 3 (G3)	120	145	19.8
Group 4 (G4)	21	145	3.5

4. Results and discussions

After exposition of the test chips to ionizing radiation, a degradation of their performance was observed, and in some cases, a total failure of the device. This latter is assumed when a loss of communication between the test chip and the device in charge of collecting the information is observed. Just before the total failure, we were able to determine the maximum TID level that this technology can tolerate. In the case of this test chip, the intrinsic resistance to ionizing radiation is around 5 kGy without applying any hardening technique. This means that a V_{bg} may eventually compensate for the performance degradation of the device only if the TID does not exceed this critical dose. Beyond a dose of 5 kGy, a thermal annealing becomes necessary. For values lower than 5 kGy, we observe degradation in power consumption and operating frequency. A common TID level was established at 1.4 kGy, in order to measure the impact of the dose rate.

Figure 6 shows the degradation at different TID levels of the transfer function between supply voltage (V_{dd}) and operating frequency for group 4 irradiated at the lower dose rate for a total TID of 3.5 kGy. For the groups G2 and G3, the same dynamics has been observed, namely a degradation of the operating frequency until a certain dose level, then an increase of the frequency. However, for Group 1 (G1), irradiated at a high dose level, we were able to perform just one point of measurement around 5 kGy, due to the failure of the device at this dose level. We observe a slowdown of the device's frequency for a TID below 1.4 kGy while an increase of the frequency is noticed for higher radiation levels. The slowdown of the device frequency can be explained by the degradation of the switching speed of the FDSOI transistors used in the device, due particularly to their increased output conductance. This kind of degradation has been actually observed in our previous work [4], where a series of 28nm FDSOI NMOS and PMOS transistors with different dimensions, oxide thicknesses and different substrate (RVT and LVT), were tested at high dose levels. The irradiated transistors showed the typical degradation of their electrical characteristics such as a negative shift of the threshold voltage, a subthreshold slope degradation ΔSS, in addition to an increase in the leakage currents. As an example of the expected degradation, Figure 5 shows the negative threshold voltage shift of elementary FDSOI-LVT NMOS and PMOS transistors used for the design of the tested device chip, for different dose levels. TID-induced degradation at transistor level increase the rise and fall time of logic gates or inducing an increase in the operating frequency and switching output errors. More irradiation tests should be applied to this component for a better understanding of the impact of radiation on the PLL. On the other hand, we assume that the increase of the device frequency beyond 1.4 kGy is due to a failure in the PLL block that generates a raised operating frequency due to the degradation of its elementary blocks. This can be the consequence of the degradation of the phase comparator which provides wrong information about the phases of the signals to be compared, in addition to the local oscillator of

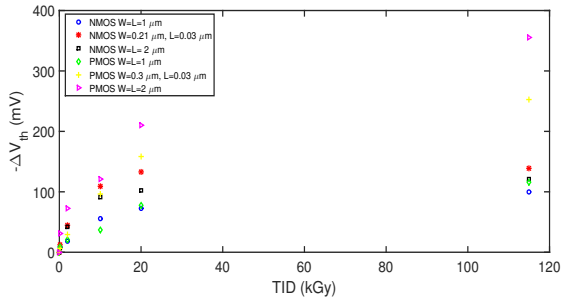

Figure 5: Threshold voltage degradation for 28nm FDSOI-LVT single transistors.

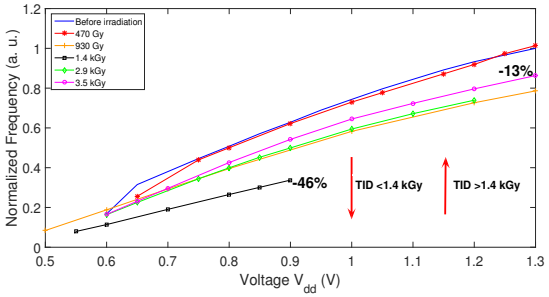

Figure 6: Frequency degradation at different TID levels.

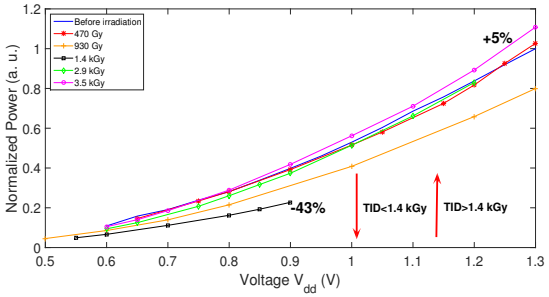

Figure 7: Power degradation at different TID levels.

the PLL whose elementary transistors are degraded affecting its operating frequency.

Figure 7 shows the power consumption of the test-chip at different TID levels. We notice that below 1.4 kGy, the power consumption of the device shows a decreasing trend with the dose level, which can be explained by the decrease of the operating frequency, as the dynamic power consumption depends directly on the switching activity.

Above 1.4 kGy, we observe that the power consumption of the device augments (green and pink lines). This is mainly due to the raised frequency after the failure in the PLL block that produces a severe increase in the dynamic power consumption and consequently, in the general power consumption. Besides, another contribution to the rise of power consumption is the increase in the leakage currents induced by the charges trapped in STI oxides.

4.1. Recovery of the performances

As described in section 2, thermal annealing can promote the detrapping of charges in the oxides generated by high levels of TID. The higher the temperature, the greater the recovery of electrical characteristics. In contrast, a high temperature applied to an electronic device can induce a significant degradation in the carrier mobility in the conduction channel and can accelerate aging mechanisms such as negative bias temperature instability , Hot Carrier Injection (HCI) and electromigration. [12]. Other mechanical effects related to the thermal expansion of the materials are potential issues when applying numerous thermal cycles at high temperatures [13]. For this reason, we propose to apply the mixed regeneration-compensation method that we have elaborated in [4]. This method reduces the annealing temperature using the inherent coupling effect proper to the FDSOI technology. This method has shown great results when applied to elementary NMOS and PMOS FDSOI transistors. The flow diagram of this strategy is depicted in Figure 8 and includes first a pre-characterization of the electrical parameters of elementary FDSOI transistors with different dimensions. Then, the devices are irradiated showing degradation, mainly in threshold voltage and in the subthreshold slope. A back-gate voltage, proportional to the degradation of the irradiated device, is applied in order to compensate for the threshold voltage shift induced by the TID. The application of the electrical method is a priority because it does not significantly affect the reliability of the component. The annealing process is started only when the compensation by the electrical technique is no longer efficient to cancel the TID-induced degradation. Once the thermal annealing cycle has finished, the compensation method is activated again, calculating and compensating the residual ΔV_{th}. Thus, we determine a set of pairs (T, V_{bg}) for which the remaining degradation of the threshold voltage and that of the subthreshold slope are less than a certain values that depend on the application and the authorized frequency degradation (For our case study, we take 5% of threshold voltage shift and 10% of subthreshold slope degradation). We determine the optimal (T, V_{bg}) pair with an annealing temperature as low as possible.

This mixed method was previously implemented experimentally on elementary 28nm FDSOI transistors, where a pair (200 °C, -0.8 V) is necessary to cancel almost the total electrical degradation in both NMOS and PMOS transistors after 115 kGy [4]. Figure 9 shows the recovery of the operating frequency when applying the proposed regeneration-compensation strategy to the test-chips belonging to group 2. First, a total failure was noticed after the devices received 12.8 kGy. Applying a temperature of 200 °C with a back-bias of 0.5 V can partially recover the frequency degradation after the failure of the test chip. Applying a V_{bg} of 1 V and an annealing temperature of 200 °C ensures the good functioning of the test-chip. Annealing at 250 °C and 300 °C is also effective with a V_{bg} of 0.5 V, but increasing the temperature may reduce the reliability of the device.

Figure 10 shows the normalized power consumption, measured after applying the regeneration-compensation strategy.

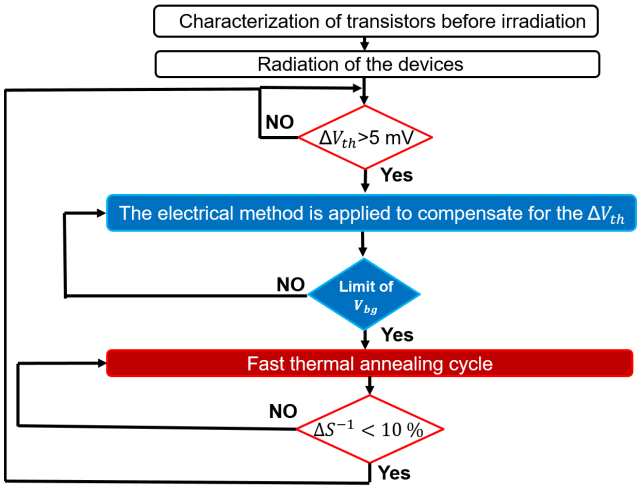

Figure 8: Flow diagram of the mixed hardening methodology.

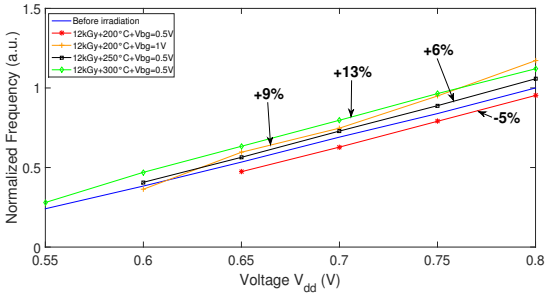

Figure 9: Frequency recovery after applying the T-V_{bg} method.

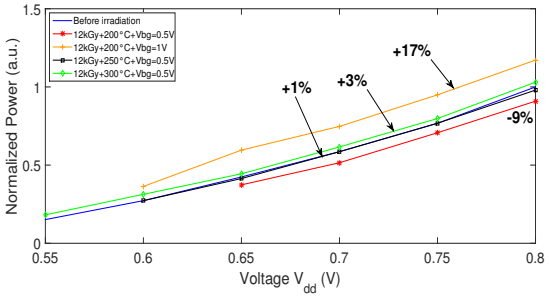

Figure 10: Power recovery after applying the T-V_{bg} method.

As expected, the method mitigates noticeably the effect of ionizing radiation on power consumption. This is due mainly to the annealing that enhances the evacuation of the trapped charges in the oxides and decreases, therefore, the radiation-induced leakage currents.

4.1.1. Pairs (T, V_{bg})

Table 2 summarizes the pairs (T-V_{bg}) required to regenerate and compensate for the degradation produced by the TID after each irradiation step. To minimize the effect of temperature on the reliability of the test chip, we have chosen the pairs with the lowest annealing temperature capable to restart the test chip after its failure. In the case of test chips from Group 4 (G4), when the TID is lower than 5 kGy, an annealing temperature of 200 °C is sufficient to cure the device without applying a V_{bg}, however, an applied V_{bg} of 0.5 V has the same effect with no impact on the device reliability. Due to the high level of ionizing radiation applied to devices of G1, a temperature above 200 °C should be applied. In fact, the trapped charges in the oxides remain at deeper energy levels, so they need a higher temperature to be re-emitted. For these chips, the annealing at 200 °C is not sufficient to revive the test chip. These values are similar to the pairs found in [4] for elementary transistors, which confirms the effectiveness of this method.

Table 2
Recovery pairs

Group/TID	Temperature (°C)	V_{bg} (V)
G1-128 kGy	250	0.5
G2-12.8 kGy	200	0.5-1
G3-19.8 kGy	200	0.5-1
G4-3.5 kGy	25	0.5

4.2. Dose-rate effects on the performance

In order to analyze the impact of dose-rate on the DSP performance, we set a common TID level at 1.4 kGy for devices of all groups. It is well known that the response to radiation of a semiconductor device is a phenomenon dependent on the exposure time. This can be verified in Figures 11 and 12, where the devices of the 4 groups show a different response in the degradation of their operating frequency and power consumption at the same TID level. In Figure 11, the operating frequency shows a decreasing degradation. G1 devices show 16% degradation compared to a pristine device. This degradation is because these devices were under the influence of radiation for a short period (1h45). The G2 and G3 devices show similar degradation because they were irradiated at a medium dose rate and an exposure of 18h and 12h respectively. However, the devices that showed the most degradation were the G4 chips that were irradiated at a low dose rate. This is because these DSPs were exposed to radiation for much longer (66h30), this allowed the charges in the volume of the oxides to move towards the interfaces $Si - SiO_2$ and $Si - BOX$ producing degradation in the slopes of the transistors and consequently a more delay in their switching response.

Likewise, Figure 12 shows the power consumed by the devices corresponding to the different groups. The G1 devices show a 15% degradation in their power consumption, due to their low exposure time to radiation. Furthermore, the chips of groups G2 and G3 show degradation of 24% and 25% respectively. Finally, the G4 devices were the most degraded with 43% degradation due to their long exposure to radiation.

The direct relation between the operating frequency and the power consumption is confirmed, where a similar behavior in the characteristics shown in Figures 11 and 12 is reported. In this case, if the operating frequency decreases,

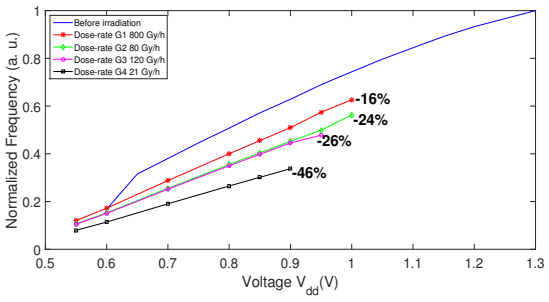

Figure 11: Frequency degradation at different dose-rates.

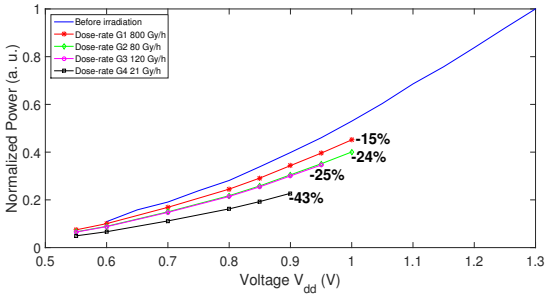

Figure 12: Power degradation at different dose-rates.

the power consumption will tend to decrease. This is true for low levels of TID, where the degradation of V_{th} is not so severe, and the leakage currents are not yet very significant. However, for higher levels of TID, the leakage currents I_{OFF} will increase, this will produce a rise in the static power consumption and consequently an increase in the overall power consumption of the IC.

4.3. Discussion

Like any hardening method, this method has advantages and drawbacks that must be taken into account. The first benefit of this methodology is the improvement of the resistance of FDSOI devices and dynamically correcting the effects due to ionizing radiation. Compared with other methods that use heat treatment, the regeneration-compensation method has the advantage of using relatively low temperatures, and only when necessary. The electrical method, using back-gate bias, allows to compensate for the negative shift of V_{th} degradation, without affecting the component reliability when applied in the allowable range. In [4], we propose an architecture that implements this mixed hardening method and that allows a real time correction of the degradation induced by the TID by prioritizing the electrical compensation. Only when the electrical method is no longer sufficient, the thermal regeneration method is triggered with a fast annealing cycle for a short period of time. In this way, the reliability of the system is less affected, prolonging its lifetime in a mission under high radiation conditions. This mixed method was experimentally tested showing great effectiveness in recovering degraded electrical parameters in single transistors and complex circuits. However, the regeneration method can be difficult to implement in embedded applications, because it requires adding heating resistors or metal heating plates in addition to circuits that limit the duration of the annealing cycle. During our annealing experiments carried out to observe the regeneration of the devices, an external heating source was used. This external source consisted of an oven, so the internal temperature of the device could be slightly lower due to heat dissipation. Having a localized source of heat could improve de-trapping performance at a lower temperature, so new solutions should be explored to implement the regeneration method. Thermally insulated devices, such as SOI Devices, have been found to have a significant increase in temperature due to limited heat dissipation through the substrate. This effect, called Self-heating effect, is one of the issues to avoid when studying the scaling of a new SOI structure [14]. However, a significant increase in temperature in an irradiated device could be beneficial to recover its electrical characteristics degraded by radiation. The electrical compensation involves the application of V_{bg} in NMOS and PMOS transistors. However, the high density and the diversity of transistors in an IC is a factor to take into account when implementing this method.

5. Conclusions

The FDSOI-LVT technology is used for low power consumption and high-frequency performance applications. The body biasing can be exploited to improve the performance of integrated circuits and to compensate for the threshold voltage shift induced by the ionizing dose. During our study, we observed that the effects of TID degraded the operating frequency and power consumption of the 32-bit DSP fabricated with 28nm FDSOI-LVT technology. At a relative low TID level, i.e. below 5 kGy for this test chip, the sole application of a back-gate voltage was sufficient to compensate for degradation. For higher doses, high temperature annealing was necessary to regenerate the component. The use of a mixed hardening method, based on the regeneration-compensation method, is promising for an implementation in embedded systems. This method reduces the negative impact of radiation and high temperatures on the reliability of a device made with FDSOI technology, while simultaneously allowing an extension of its life-time during a mission in a radioactive environment.

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