Contactless four-terminal MEMS Variable Capacitor for Capacitive Adiabatic Logic

Ayrat Galisultanov, Yann Perrin, Hatem Samaali, Hervé Fanet, Philippe Basset, Gaël Pillonnet

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A Galisultanov[1], Y Perrin[1], H Samaali[2], H Fanet[1], P Basset[2] and G Pillonnet[1]

[1] Univ. Grenoble Alpes, CEA, LETI, F-38000 Grenoble, France
[2] Université Paris-Est, ESYCOM, ESIEE Paris, France

ayrat.galisultanov@cea.fr

Abstract. This paper reports the design, energy recovery and logical functionality modelling of four-terminal MEMS comb-drive devices for capacitive adiabatic logic (CAL). The proposed electromechanical element consists of the moving mass with two insulated electrodes and two fixed electrodes. The two pairs of fixed and moving electrodes form an input and an output comb-drive capacitive transducers. The voltage across the input port allows us to control the capacitance of the output port. The developed contactless four-terminal design is simulated in Coventor MEMS+® software. In order to speed-up transient simulation of numerous devices in an electrical Spice simulator, the obtained electrical and mechanical characteristics are used to fit our Verilog-A analytical compact model. Spice-simulation results demonstrate CAL logical functionalities using cascadable power clock scheme, i.e. logic states differentiation and cascadability. Also we show that MEMS-based calculation is energy efficient, for example, in a chain of four buffers, 99.1% of the energy transferred to the device is recovered for later use when devices operate at 25 Hz. The non-recoverable energy is mainly dissipated by mechanical damping during the logic state transition from high to low level and can be removed by using retractable power clocks. For this mm-scale device the energy dissipated per operation is in the order of one pJ. This is still far from the energy dissipated by a nm-scale FET transistor, which is of the order of 10's aJ. However, for the contactless design constant electric field scaling is possible and the energy dissipation decreases proportionally to the cube of the size. Finally, the difference between the signal energy and the distinguish energy in MEMS-based adiabatic logic is discussed.

1. Introduction

Despite the nanoscale size of the modern transistors, the dissipation per logic operation in digital circuits is of order of 10's aJ [1]. It is four orders of magnitude higher than the theoretical limit introduced by Landauer (3 zJ at 300 K) [2]. In a static CMOS circuit, the energy provided by the voltage source E_{prov} is dissipated in each switching event. The amount of the dissipated energy E_{diss} equals to the signal energy $E_{sig} = CV_{DD}^2 / 2$, where C is the capacitor at the output gate(s) and V_{DD} is the voltage supply. This effect is represented in Figure 1a for the CMOS buffer. The ramping time T here is much greater than the RC time constant, where R is the resistance of the charging path. In order to characterize energy loss in the calculation, we can introduce a fractional energy efficiency parameter η (where $0 \leq \eta \leq 1$) for the charging-discharging "0"→"1"→"0" loop:

$$\eta = 1 - E_{diss} / E_{prov}. \quad (1)$$

The energy efficiency of the static CMOS circuit is zero, as all provided energy is dissipated to heat. However, there is no fundamental limitation to dissipate less than signal energy E_{sig}.

Adiabatic (smooth) switching between logic states is the basis for many approaches to energy recovery [3]. In other hand, it leads to a decrease in the operating frequency by smoothing logic state transition. As presented in Figure 1b, this approach allow us to recover the signal energy and suppress dynamic dissipation CV_{DD}^2. On CMOS-based irreversible adiabatic logic, the dissipation per logic operation decreases by a factor of ten as shown in [4]. Further improvement is limited by an inherent trade-off between the dynamic and leakage losses caused by the internal properties of the FET transistor, i.e. the subthreshold slope [5].

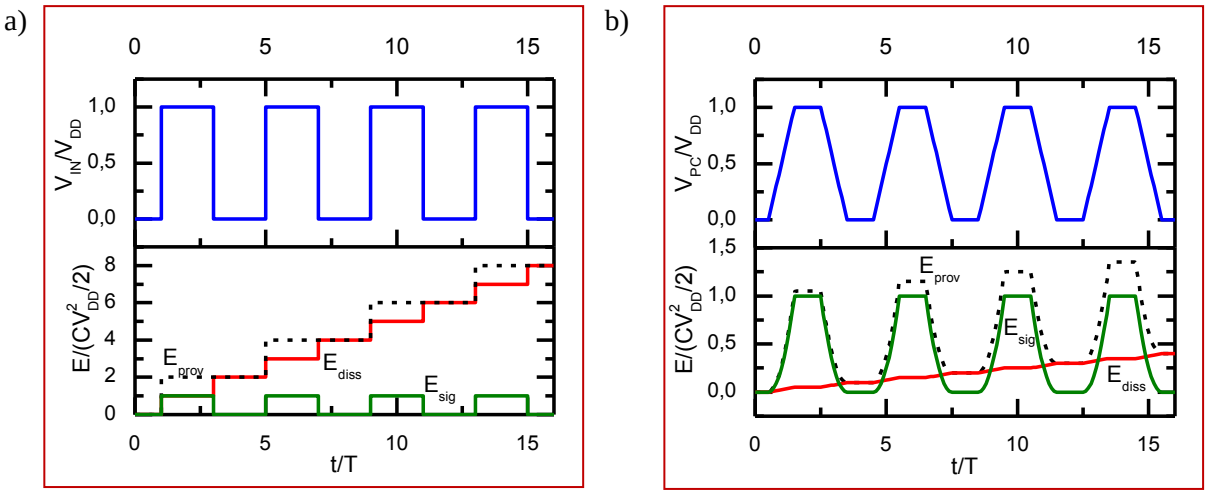


Figure 1. a) Static CMOS logic ($RC << T$). Normalized input voltage V_{IN}/V_{DD} (first graph), normalized provided E_{prov}, dissipated E_{diss}, and signal energy E_{sig} (second graph). b) Adiabatic CMOS logic. Normalized power supply voltage V_{PC}/V_{DD} (first graph), normalized provided E_{prov}, dissipated E_{diss}, and signal energy E_{sig} (second graph).

To suppress this inherent trade-off, electromechanical relays have been introduced in the literature [6]. As they are based on metal-metal contact instead of a semiconductor junction, the leakage becomes almost negligible except in the case of nm-scale electrostatic gap [4]. Unfortunately, the main bottleneck of the relay-based adiabatic logic is the mechanical reliability and performance limit of the scaled switches, due to adhesion force of contact interface [7]. To overcome this limitation, we recently proposed a new logic family called Capacitive Adiabatic Logic (CAL) [8, 9]. Due to smooth switching process in adiabatic logic, the resistive elements (transistors, relays) in a voltage divider circuit can be replaced by capacitive ones.

Let us consider four-terminal voltage-controlled capacitance $C_{DS}(V_G)$. In this paper, we keep the FET transistor notations, i.e. the input control voltage is applied between the gate (G) and the ground (GND). These two terminals are isolated from the drain (D) and source (S) terminals, which form an output with a capacitance C_{DS}. There are two possible behaviors of capacitance as a function of the input voltage. The curve $C_{DS}(V_G)$ can have a positive or negative slope, as presented in Figure 2a. The former case is called positive variable capacitance (PVC) and the latter, negative variable capacitance (NVC). PVC and NVC voltage-controlled capacitors could play the same role in CAL as NMOS and PMOS in FET-based logic, respectively.

Based on these two elements, we can easily construct a CAL inverter, which is shown in Figure 1b. All other basic logic gates are presented and discussed in [8-9]. The output voltage is defined by the capacitance ratio and the power supply voltage $V_{PC}(t)$ such that:

$$V_{OUT}(t) = \frac{C_{NVC}(V_{IN})}{C_{PVC}(V_{IN}) + C_{NVC}(V_{IN})} V_{PC}(t). \qquad (2)$$

Two cases emerge, which are:
– when the input voltage is lower than the low logic level $V_{IN}<V_L$, the proper C_L, C_H, and $V_{PC}(t)$ selection can guarantee that the output voltage is higher than the high logic level $V_{OUT}>V_H$;
– when the input voltage is higher than the high logic level $V_{IN}>V_H$, the proper C_L, C_H, and $V_{PC}(t)$ selection can guarantee that the output voltage is lower than the low logic level $V_{OUT}<V_L$.

The basic device of CAL consists of two electrically isolated and mechanically coupled capacitors. The gap-closing MEMS variable capacitor could be a good candidate for this purpose as it offers large capacitance variation if the actuation voltage is higher than pull-in voltage [10]. However, a mechanical contact is required in order to have a high capacitance variation. Consequently, this solution suffers from high non-adiabatic loss, which is independent of the operating frequency and cannot be suppressed by the ramping time increasing [11]. On the contrary, the comb-drive MEMS variable capacitor avoids electrical and mechanical contacts [12].

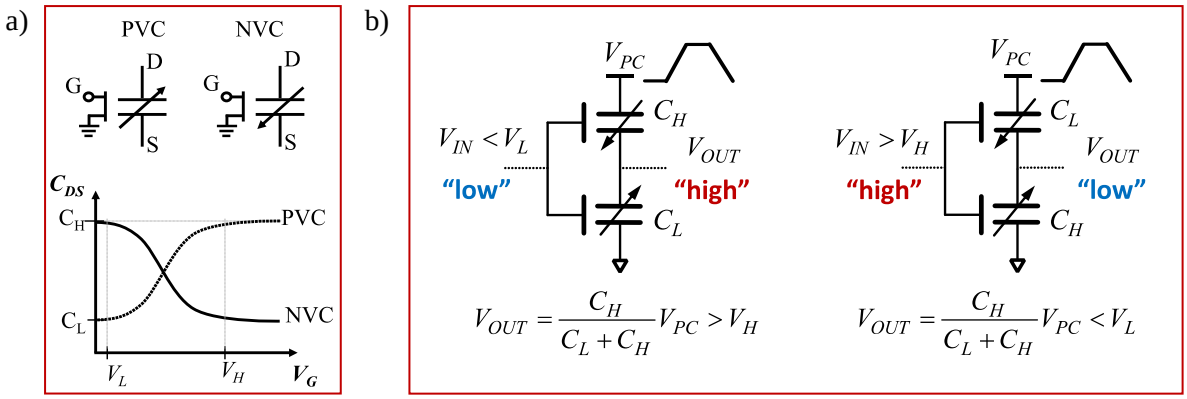
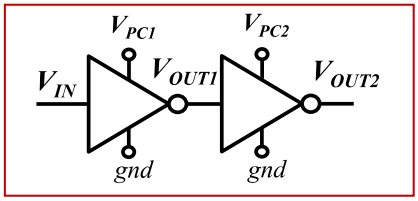


Figure 2. a) Capacitance–voltage (CV) characteristics and symbols for positive variable (PVC, dotted line) and negative variable (NVC, solid line) capacitors. The low and high voltage levels are denoted as V_L and V_H, respectively. The same notation (C_L and C_H) is used for capacitance levels. b) Electrical schematics of simple CAL inverter circuit and cascadability conditions.

CMOS-based adiabatic logic circuits basically operate with two types of architecture: Bennett clocking, called also retractable, and four-phase quasi-adiabatic pipeline [13]. The power supplies, called power clocks (PC's), are quite different for these two architectures. The common thing is that these two types of power supply can provide and recover energy, i.e. realize charge recovery. In this work, we use both type of power clocks. Retractable logic can be seen as asymptotically reversible logic, but it requires N different PC's for a N-deep logic chain. Additionally, retractable PC is more slow, as during byte transfer through a chain of inverters (c.f. Figure 3a), the chain is blocked for other information, as presented in figure 3b. On the contrary, quasi-adiabatic pipeline PC requires only four different PC's with a $\pi/2$ phase shift and can change input each $4T$ (cf. Figure 3c). PC's synchronize the speed of transfer and processing of information. The energy losses in the reversible PC's are out of the scope of this paper, but can be found in [14-17].

a)



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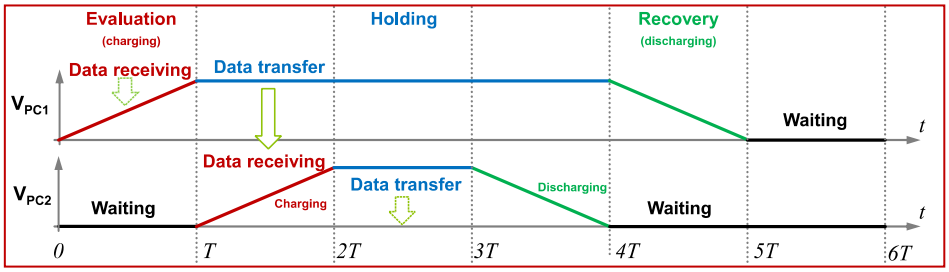

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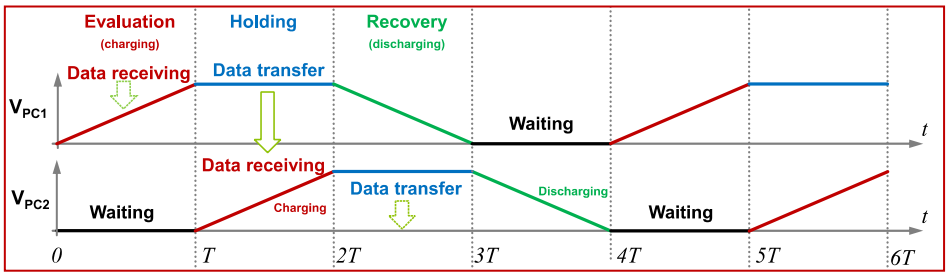

Figure 3. a) Cascade of two inverters. b) Data and energy transfer in Bennett (retractable) power clock. c) Data and energy transfer in four-phase quasi-adiabatic pipeline power clock.

The design of the MEMS variable capacitor must be optimized for energy efficient charging and discharging processes. On the other hand, a logic gate based on this element must be capable to differentiate "0" and "1" logic states. Furthermore, as shown in Figure 2b, the logic gate must be able to receive the logic state from the previous gate, process it and transmit the result to the next gate, i.e. to be cascadable. In other words, input and output states have to be capable to plug the gates in series.

The aim of this work is to demonstrate energy recovery capability of comb-drive MEMS device and discuss its fundamental limitations. In the next section, we introduce our MEMS topology to implement four-terminal PVC and describe analytical and numerical simulation approaches.

2. Methods

The proposed microelectromechanical element consists of the two electrically isolated and mechanically coupled capacitors. In order to avoid any contact between the electrodes, we use contactless interdigitated comb transducers for both capacitors. This paper extends the proposal of [12].

2.1. Design of the MEMS variable capacitors

The MEMS realization of voltage controlled capacitor C_{DS} is based on two comb-drive transducers, as shown in Figure 4a. The proposed electromechanical element consists of the moving mass with two insulated electrodes and two fixed electrodes. The two pairs of fixed and moving electrodes form an input and an output comb-drive capacitive transducers. The input (left) transducer has an initial overlap L_{in} between the fixed and the moving electrodes. The output transducer (right) is symmetrical and does not have an initial overlap. An initial gap L_{gap} is present between the fingers of the output transducer. The input capacitor C_G forms an actuator and is used for control of value of the output capacitor C_{DS} as function of input voltage V_G. The capacitance value C_{DS} also depends on voltage across it V_{DS}. In order to avoid self-actuating the capacitance C_{DS} is symmetric and is not affected by V_{DS}, when input voltage V_G is low.

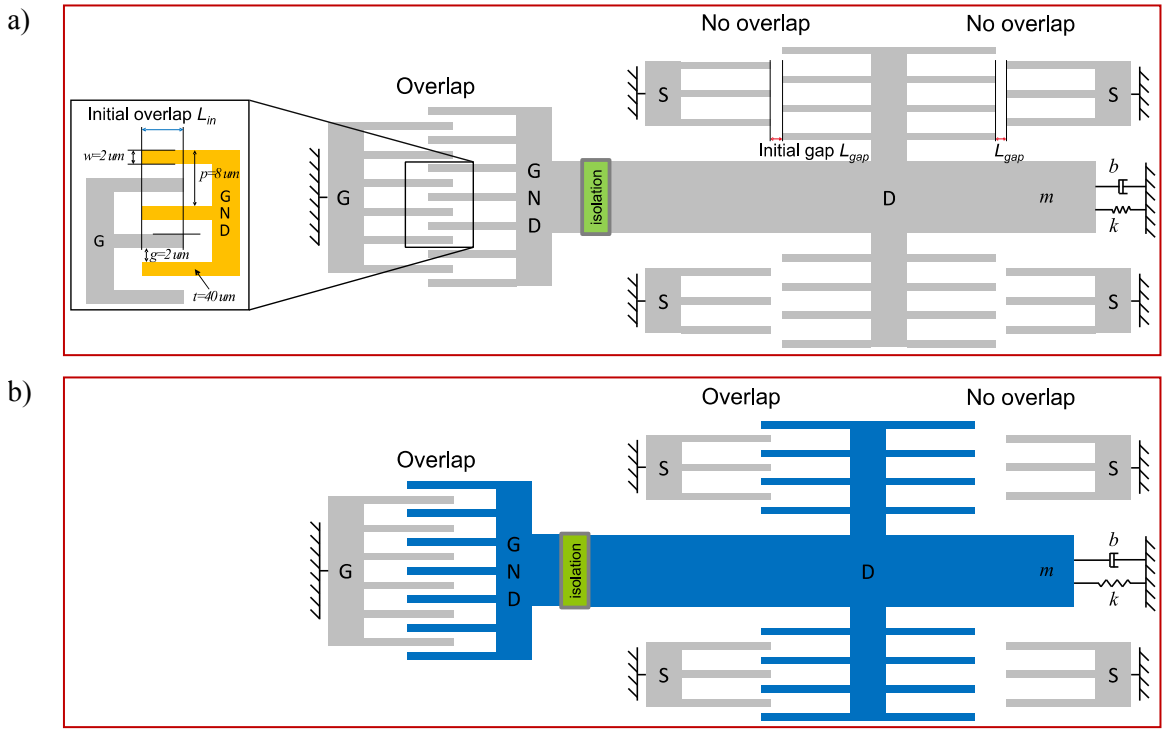

Figure 4. Two states of MEMS element as function of the moving mass displacement *x*. a) Low state: $-L_{gap} \le x \le L_{gap}$. Parameters of the comb-drive actuator are presented in the insert. b) High state: $x < -L_{gap}$.

We assume that the device is made of SOI wafer, with Si (100) structural layer having a thickness *t* equal to 40 μm. The buried oxide with 2 μm thickness provides insulation and rigid mechanical connection between GND and D electrodes of the moving part. The parameters of the comb actuators are shown in Figure 4a. The gap space *g* between comb-drive fingers is 2 um, the width of the finger *w* is 2 um, and the finger pitch *p* is 8 um. The gap space *g* and the width of the finger *w* values are established on the basis of the typical optical lithography capabilities.

The Coventor MEMS+® contactless comb-drive model of variable capacitance is presented in Figure 5. The left comb-drive actuator corresponds to the input, and the right comb-drive actuator forms the output. Input and output transducers form input C_G and output C_{DS} capacitances, respectively. The moving mass is suspended by four identical springs.

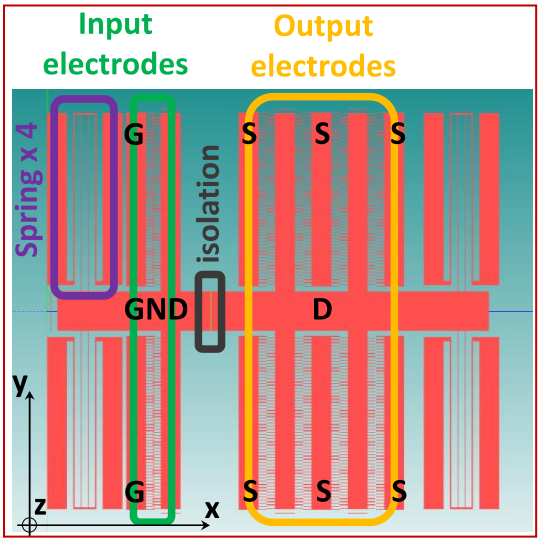

Figure 5. Top view of the contactless four-terminal MEMS element. Length of the structure is 1.2 mm, width is 1 mm, number of input fingers N_{in} is 110, number of output fingers N_{out} is 220.

2.2. MEMS+® results

The mechanical parameters extracted from MEMS+® simulations are presented in Table 1. The resonant frequency of the device is around 1.2 kHz.

Table 1. Extracted from MEMS+ simulation mechanical characteristics of MEMS element.

Parameter	Value
Mass m, kg	$4.41 \cdot 10^{-8}$
Spring constant k, N/m	2.39
Resonant frequency f_{res}, Hz	1173
Damping coefficient b, kg/s	$1.16 \cdot 10^{-5}$
Quality factor, Q	28

The received displacement and the capacitance CV curves are shown in Figure 6. The initial overlap of input transducer L_{in} = 15 um and the initial gap between the fingers of the output transducer L_{gap} is 1 um. L_{in} and L_{gap} values are selected in order to have initial capacitance ratio between the input and the output capacitances of about 1.4. Due to different number of input N_{in} and output N_{out} fingers, this ratio decreases during actuation and reaches unity when $V_G \approx 30$ V. This variation allows us to define low and high states.

In this design, low and high states can be distinguished by the moving mass displacement x as compared with the the initial gap L_{gap}. If the input voltage V_G is lower than the threshold input voltage V_{TH} = 10 V, as represented in Figure 6, there is no overlap in the output transducer ($-L_{gap} \leq x \leq L_{gap}$) and, consequently, the voltage V_{DS} does not affect the position nor the capacitance ratio, as the output combs are symmetrical (c.f. Figure 4a). For V_G higher than the threshold input voltage V_{TH}, an overlap appears in the left part of the output ($x < -L_{gap}$.), as shown in Figure 4b. In that case, an increase of V_{DS} moves the mass to the left, and changes the capacitance ratio in the voltage divider circuit.

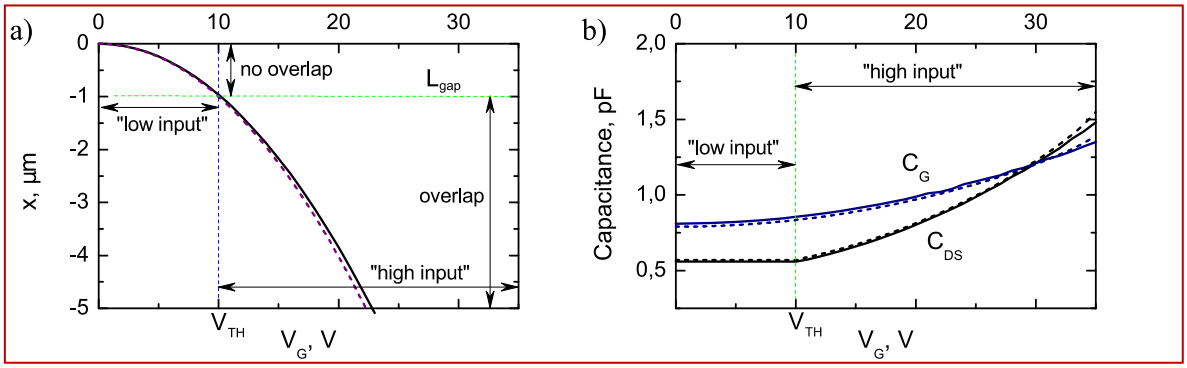

Figure 6. a) Moving mass displacement as a function of the input voltage V_G. b) Input C_G and output C_{DS} capacitances as a function of the input voltage V_G. Verilog-A model and MEMS+® simulation results are drawn as solid and dashed lines, respectively.

2.3. Analytical compact model

This electromechanical system has two electrical ports and one mechanical port. The developed model includes both electrical and mechanical parts of the system. The electrical part consists of four electrical terminals described in Figure 4 (G, GND, D, S). The mechanical part is a simple mass-spring-damper system and can be described by the following equation of motion:

$$m\ddot{x}=-b\dot{x}-kx+F_{eG}+F_{eDS}, \tag{3}$$

where input F_{eG} and output F_{eDS} electrostatic attractive forces are calculated from:

$$F_{eG}=\begin{cases}-\alpha_1 V_G^2 N_{in}\varepsilon_0 t/g, & \text{if } x\le L_{in}\\ 0, & \text{if } x>L_{in}\end{cases}, \tag{4}$$

$$F_{eDS}=\begin{cases}-\alpha_2 V_{DS}^2 N_{out}\varepsilon_0 t/g, & \text{if } x\le -L_{gap}\\ 0, & \text{if } |x|<L_{gap}\\ \alpha_2 V_{DS}^2 N_{out}\varepsilon_0 t/g, & \text{if } x\ge L_{gap}\end{cases}, \tag{5}$$

where α_1 = 1.18 and α_2 = 1.09 are the fitting parameters extracted from MEMS+® results, and $\varepsilon_0 = 8.854\cdot10^{-12}$ F/m is the vacuum permittivity. According to Equation 6 [18], the charging and discharging current through the MEMS variable capacitor is a sum of two components. The first one is the familiar capacitive current. The second one is the motional current, which describes the transfer of energy from the electrical to the mechanical domain and vice versa.

$$i(t)=C(x)\frac{dV(t)}{dt}+\frac{dC(x)}{dx}V\frac{dx}{dt} \tag{6}$$

The input C_G and output C_{DS} capacitances are calculated from:

$$C_G=\begin{cases}C_{Gp}+2\alpha_1 N_{in}\varepsilon_0 t(L_{in}-x)/g, & \text{if } x\le L_{in}\\ C_{Gp}, & \text{if } x>L_{in}\end{cases}, \tag{7}$$

$$C_{DS}=\begin{cases}C_{DSp}+2\alpha_2 N_{out}\varepsilon_0 t(-L_{gap}-x)/g, & \text{if } x\le -L_{gap}\\ C_{DSp}, & \text{if } |x|<L_{gap}\\ C_{DSp}+2\alpha_2 N_{out}\varepsilon_0 t(x-L_{gap})/g, & \text{if } x\ge L_{gap}\end{cases}. \tag{8}$$

The input C_{Gp} and output C_{DSp} parasitic capacitances are extracted from MEMS+® simulations and equal 0.12 and 0.56 pF, respectively. The C_G definition (7) is not entirely accurate in the region without overlap ($x\ge L_{in}$). However, this displacement range is out of normal operation regime. Consequently, this definition does not affect the accuracy of the model.

We use a Verilog-A hardware description language to realize this analytical compact model of MEMS device. The simulated CV and mechanical characteristics obtained from MEMS+ are used to fit a Verilog-A analytical compact model. The comparison between Verilog-A compact model and MEMS+® simulations is presented in Figure 6. This approach allows us to include the MEMS device compact model in the electrical simulator and speed-up the transient simulation of cascaded gates.

3. Results

In an electromechanical system such as CAL, the total dissipation is the sum of the losses in the electrical and mechanical domains [18].The smooth transition needed in any adiabatic logic family reduces the operating frequency. To suppress the power dissipation, the ramping time T should be more than both the electrical RC and mechanical relaxation time $Q/(\pi f_{res})$ constants.

3.1. Energy analysis in the four-terminal device

In order to study the dynamical behavior of the four-terminal variable capacitor, we performed transient electromechanical simulation using the aforementioned compact model of the circuit depicted in Figure 7a. Only the case of high state displacement ($x < -L_{gap}$) is discussed. During the simulation, all energy components are calculated and the conservation of energy is checked. The energy components in this electromechanical system are:

- Energy delivered by Nth power clock (energy source) $$E_{EL_N} = \int_0^{t_0} V_{PC_N}(t) i_N(t) dt$$
- Electrostatic energy stored in the input capacitance C_G (recoverable) $$E_{C_G} = \frac{1}{2} C_G V_G^2$$
- Electrostatic energy stored in output capacitance C_{DS} (recoverable) $$E_{C_{DS}} = \frac{1}{2} C_{DS} V_{DS}^2$$
- Energy dissipated in the Nth resistor (irreversible loss) $$E_{R_N} = R \int_0^{t_0} i_N^2(t) dt$$
- Mechanical spring energy (recoverable) $$E_M = \frac{1}{2} k x^2$$
- Kinetic energy (recoverable) $$E_{KIN} = \frac{1}{2} m v^2$$
- Damping loss (irreversible loss) $$E_D = b \int_0^{t_0} v^2(t) dt$$

where we assume that the resistance R is equal for all charging paths, v is velocity of the moving mass, V_{PCN} and i_N are the output voltage and current of the Nth PC, respectively.

For this simulation and model verification, we selected PC's with a ramping time T = 10 ms higher than that of the mechanical relaxation time $\tau_M = Q/(\pi f_{res})$ = 7.58 ms and with $V_{PC1max} = V_{PC2max}$ = 20 V > V_{TH} = 10 V. The maximum PC voltage V_{PC1max} is selected higher than the input threshold voltage V_{TH} in order to create overlap in the output and to induce the significant displacement of the moving mass.

The simulation results during charging and discharging process are presented in Figure 7b. We use four-phase PC here. According to Equation 6, a part of the electrical energy is converted into mechanical energy during the charging process of C_G and C_{DS}. During the discharge phase, most of the electrical and the mechanical energy stored in the system are recovered in the PC's. The difference between provided and recovered energy is determined by damping and resistive losses. However, mechanical loss dominates here, as the mechanical time constant is six orders of magnitudes higher

than the electrical one (the mechanical relaxation time equals τ_M = 7.58 ms, the RC time constant equals $\tau = RC_{DS}$~1 ns). This means that mechanical motion is adiabatic in the electrical domain.

The fractional energy efficiency η, i.e. ratio between the recycled energy and the energy provided by PC's, is 99.8 %. The maximal energy provided by PC's is 685 pJ. The irreversible losses are caused by the damping (1.56 pJ) and resistive (0.3 fJ) losses. The energy saving law is satisfied. The main part of mechanical loss dissipation arises from the loss of the electromechanical coupling in the output transducer during the discharging phase of the output capacitance C_{DS}. In the second graph of Figure 7b, it can be observed as free vibration from $t \geq 3.8T$.

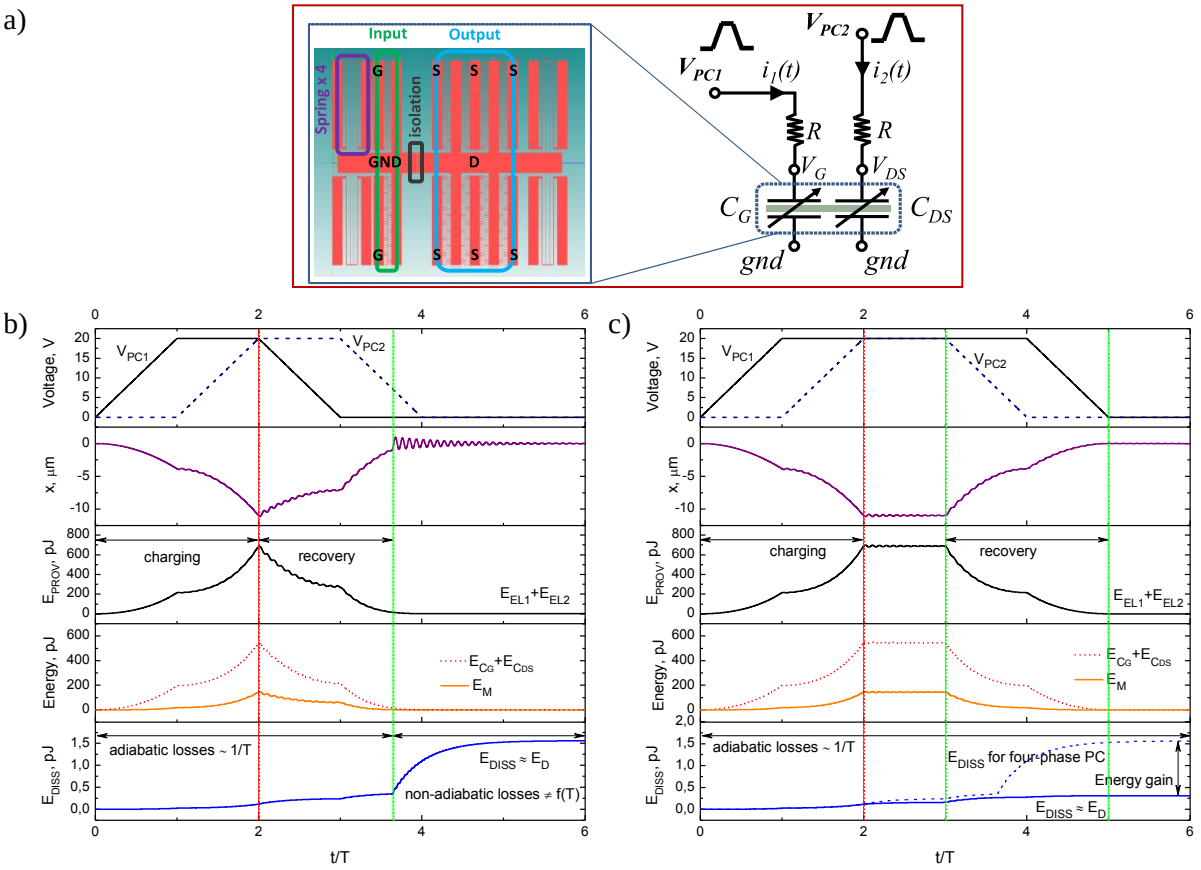

Figure 7. a) Test circuit. b-c) Evolution of voltages applied to the four-terminal MEMS element (first graph), moving mass displacement (second graph), electrical energy provided by PC's (third graph), electrical energy stored in capacitances and mechanical spring energy (fourth graph), and dissipated energy (fifth graph) over time for test circuit operated with b) four-phase and c) Bennett clocking PC's. We used the following parameters: T = 10 ms, R = 1 kΩ, V_{PCmax} = 20 V.

The simulation results with the same parameters, but for Bennett clocking PC, are shown in Figure 7c. The fractional energy efficiency η is 99.96 %. The maximal energy provided by PC's is the same as in the case of four-phase PC's (685 pJ). The irreversible losses are caused by the damping (0.3 pJ) and resistive (0.3 fJ) losses. Retractable PC's are more energy efficient here, since there is no loss of the electromechanical coupling in the output transducer during operation. For both cases the maximal electrostatic energy is 3.8 times higher than the maximal mechanical spring energy. In the ideal electromechanical actuator these energies should be equal [18], but in our realistic device model, the electrostatic energy dominates due to presence of parasitic capacitances.

In Figure 8, we present the effect of ramping time T on the dissipated energy E_{diss} during one cycle for device actuated with four phase and Bennett clocking PC's. All other parameters are the same as in

the previous calculations. The increasing ramping time decreases the dissipation for retractable PC's. This demonstrates the absence of any non-adiabatic losses in Bennett clocking PC's for the proposed design. However, for four-phase PC's we observe presence of the non-adiabatic losses, i.e. the losses, which do not depend on the ramping time T and cannot be recovered by PC's. These losses are caused by the loss of the electromechanical coupling in the output transducer during the discharging phase of the output capacitance C_{DS}. The coupling disappears when $x = -L_{gap}$, and, consequently, the system losses the following mechanical energy stored at this moment:

$$E_{NA} = kL_{gap}^2 / 2 . \quad (9)$$

L_{gap} in current MEMS-based CAL device is analog to V_T in metal–oxide–semiconductor technology. The energy dissipated during one cycle tends to this value when the ramping time T tends to infinity. For our device, the non-adiabatic part of dissipated energy equals 1.2 pJ.

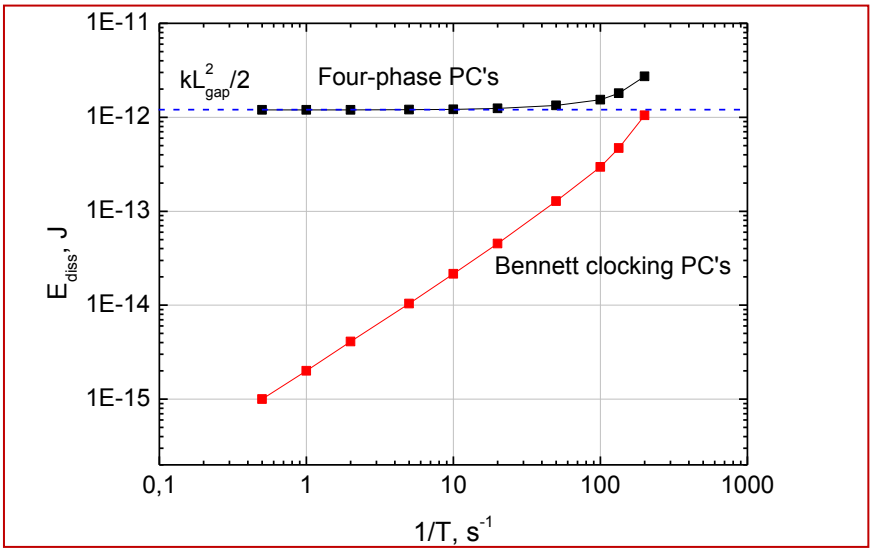

Figure 8. Simulated dissipated energy E_{diss} according to inversed ramping time T^{-1} for device operated with four-phase and Bennett clocking PC's.

3.2. Cascadability

The cascadability of the proposed four-terminal device is demonstrated using an array of buffer elements. In CAL we can use the input capacitance of the next gate as an element of voltage divider circuit, as presented in Figure 9a. The additional complementary NVC is not needed, unlike to CMOS circuits. The buffer chain circuit is presented in Figure 9b. The output voltage is measured across constant capacitance C_0 = 0.86 pF, which mimics the input capacitance of the next gate. The threshold voltage V_{TH} for simulated design is 10 V. The input voltage amplitude is 8 V and 12 V for low and high input levels, respectively. The binary input logic word "1010" is transferred through the buffer chain, as demonstrated in Figure 9c for quasi-adiabatic pipeline PC's. The logic state in further gates is coded by the moving mass displacement x, induced by the input voltage. If the amplitude of displacement is less than L_{gap} value, there is no overlap and, consequently, the output capacitance C_{DS} is not affected by the voltage V_{DS} around it (c.f. the second graph of Figure 9c). Due to the output symmetry wrong "1" is avoided. It causes low signal level in the next gate, i.e. V_{GN} is below V_{TH} and is considered by $(N+1)^{th}$ gate as a low state. On the contrary, if the input is high ($V_{GN} > V_{TH}$), the amplitude of displacement $|x|$ is higher than L_{gap} value. Consequently, the rise of the output voltage is able to trigger a displacement of the moving mass, transferring the high input signal to the $(N+1)^{th}$ gate of the buffer chain. The logic state is maintaining during holding phase (input decreasing) thanks

to the output electrostatic force F_{eDS} of the next gate. This inherent memory effect simplifies CAL circuit. The effect is shown in the fourth graph of Figure 9b. The energy efficiency parameter η equals 99.1 % for the selected PC's voltage level when devices operate at 25 Hz. The "0" and "1" states can be distinguished, even if the voltage difference between them is a few volts. In the third graph of Figure 9c we can observe the absence of voltage degradation during signal transfer throw the buffer chain due to power clock, which provides energy in the same level along the chain. For this design the length of the buffer chain is not limited. The system demonstrates cascadability for the maximal PC amplitude V_{PCmax} ranging from 22 to 25 V.

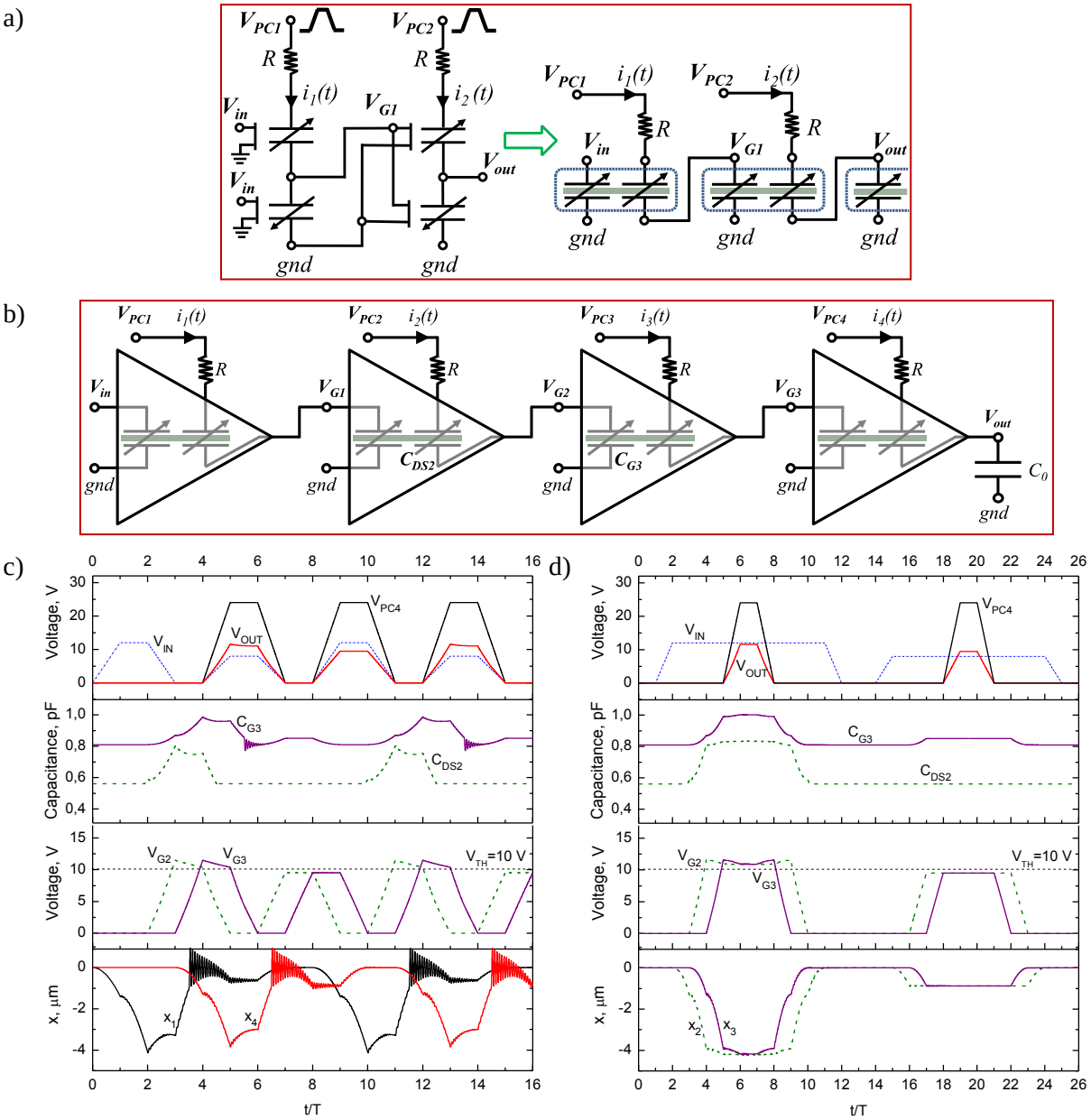

Figure 9. a) Electrical circuit simplification due to using the input capacitance of the next gate as an element of voltage divider circuit. b) Electrical diagram of the cascade of four buffers. c) Spice simulation results: input voltage V_{IN}, V_{PC1}, output of the first buffer V_{OUT} (first graph), C_{DS2} and C_{G3} (second graph), V_{G2} and V_{G3} (third graph), displacement of the first x_1 and the fourth x_4 MEMS elements over time for four-phase PC's. d) Spice simulation results: input voltage V_{IN}, V_{PC1}, output

of the first buffer V_{OUT} (first graph), C_{DS2} and C_{G3} (second graph), V_{G2} and V_{G3} (third graph), displacement of the second x_2 and the third x_3 MEMS elements over time for retractable PC's. We used the following parameters: T = 10 ms, R = 1 kΩ, V_{PCmax} = 24 V, C_0 = 0.86 pF.

The non-recoverable energy is mainly dissipated by mechanical damping during the changing of state from high to low (i. e. byte erasing) and can be removed by using retractable PC's, as presented in Figure 9d. The signal is transferred due to controlled capacitance variation, as for former case with four-phase PC's, however retractable PC's form an asymptotically reversible logic. Due to this the non-adiabatic loss (9) is suppressed as clearly seen in the fourth graph of the Figure 9c. The energy efficiency parameter η increases from 99.1% to 99.97 %.

3.3. Scalability trend

For this mm-scale device the energy dissipated during one cycle is of the order of one pJ per operation. This is still far from the energy dissipated by a nm-scale FET transistor, which is of the order of 10's aJ. However, constant field scaling scenario is available, as there is no adhesion force limitation, unlike to nanorelay [7]. The energy dissipation for the contactless design decreases proportionally to the cube of the size. As presented in Figure 10, the "optimistic" scalability trend is limited by the two factors. First factor is the Landauer limit for irreversible logic $k_B T \ln 2$ (3zJ@300K) [2]. The second is the tunnelling current, which cannot be neglected for nm-scale electrostatic gap [19]. For the scaled design, the level of dissipation in the electromechanical MEMS device can be decreased up to 100's of zJ. It should be noted that the total dissipated energy is affected by the energy losses within the reversible power supplies, which are not taken into account here.

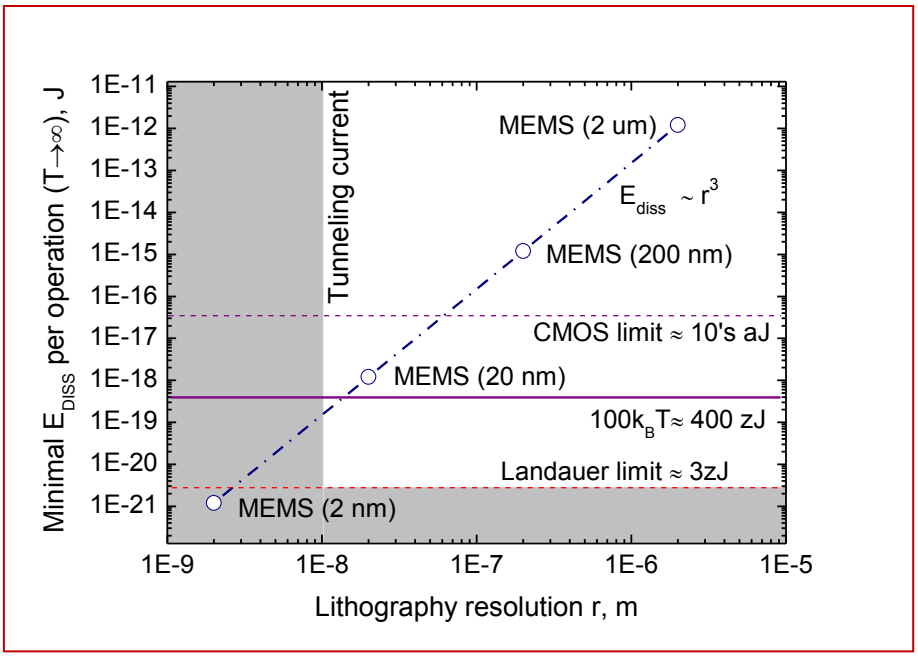

Figure 10. Simulated minimal dissipated energy trend E_{diss} for the ramping time tends to infinity according to lithography resolution r for device operated with four-phase PC's. Here we assume that $L_{gap} = r/2$.

4. Discussion

As we mentioned in the introduction, the energy efficiency η of the static CMOS circuit is zero, as all provided energy is dissipated to heat [3-4]. The part of the provided energy E_{prov} can be reused due to

smooth changing between logic states and special type of power supply that can recover the signal energy E_{sig}. However, the main drawback of this approach is the decrease in the operating frequency. The second problem is the energy recovery in a circuit operating with four-phase PC's. As a memory is needed in holding phase, the provided energy is not fully recoverable. The energy of the signal is divided into two parts. First part of the energy is recoverable and equals ($E_{sig} - E_{dist}$), the second part being the distinguish energy E_{dist}, which separates low and high logical states. In presented contactless electromechanical device it equals $kL_{gap}^2 / 2$. The distinguish energy also exists in CMOS and equals $CV_T^2 / 2$. This energy cannot be recovered in irreversible logic and causes non-adiabatic energy loss. In other word, the maximal energy efficiency of irreversible quasi-adiabatic logic is limited by ratio:

$$\eta \to 1 - E_{dist} / E_{prov}, \text{ for } T \to \infty . \quad (10)$$

The distinguish energy E_{dist} is limited below by the Landauer limit $k_B T \ln 2$ [2]. Additionally, E_{dist} must be significantly higher than $k_B T$ to be robust in thermal environment in order to prevent spontaneous change of state. The noise margin needs to be at least higher than 100 $k_B T$ [20], this level is shown in Figure 10. Once again, we would like to note that E_{sig} is not the energy which separates logic states. This principle demonstrates the limits of irreversible adiabatic logic and the interest to reversible calculation. We will build reversible MEMS CAL gates in the near future.

5. Conclusion

A contactless design of a variable MEMS capacitor for CAL has been successfully developed, tested, and verified. Our design avoids leakage losses, in contrast to CMOS-based adiabatic logic, and resolves the contact reliability problem of a nanorelay solution. An analytical compact model of the electrostatically-actuated four-terminal variable capacitor has been developed. The analysis of loss mechanisms have been done for a single device and for a cascade of buffer chain. The binary input logic word "1010" is successfully transferred through chain of buffers. The energy efficiency η equals 99.1 % when devices operate at 25 Hz with quasi-adiabatic pipeline PC's. For this type of architecture the non-adiabatic dissipation has been demonstrated for the presented MEMS device. This energy can be recovered by using retractable PC's.

For this mm-scale device the energy dissipated during one cycle is of the order of one pJ per operation for four-phase PC's. This is still far from the energy dissipated by a nm-scale FET transistor, which is of the order of 10's aJ. However, scalability has been studied and the energy dissipation for the contactless design decreases proportionally to the cube of the lithography resolution until nanoscale parasitic effects. MEMS-based CAL could be of interest as energy efficient alternatives to CMOS transistors for low-power adiabatic circuit applications.

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