Electromigration assessment in power grids with account of redundancy and non-uniform temperature distribution

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ABSTRACT

A recently proposed methodology for electromigration (EM) assessment in on-chip power/ground grid of integrated circuits has been validated by means of measurements, performed on dedicated test grids. IR drop degradation in the grid is used for defining the EM failure criteria. Physics-based models are involved for simulation of EM-induced stress evolution in interconnect structures, void formation and evolution, resistance increase of the voided segments, and consequent re-distribution of electric current in the redundant grid paths. A grid-like test structure, fabricated with a 65 nm technology and consisting of two metal layers, allowed to calibrate the voiding models by tracking voltage evolution in all grid nodes in experiment and in simulation. Good fit of the measured and simulated time-to-failure (TTF) probability distribution was obtained in both cases of uniform and non-uniform temperature distribution across the grid. The second test grid was fabricated with a 28 nm technology, consisted of 4 metal layers, and contained power and ground nets connected to "quasi-cells" with poly-resistors, which were specially designed for operating at elevated temperatures ~350°C. The existing current distributions resulted in different behavior of EM-induced failures in these nets: a gradual voltage evolution in power net, and sharp changes in ground net were observed in experiment, and successfully reproduced in simulations.

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CCS CONCEPTS

• **Hardware** → Electronic design automation → Methodologies for EDA → Software tools for EDA

KEYWORDS

Reliability theory, failure analysis, power grids, stress

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1 INTRODUCTION

For designing a reliable chip, the power/ground (p/g) grid resilience to EM failure should be addressed. The conventional approach to EM assessment is based on design rules, which specify the limiting current densities in each interconnect

segment. The rule violation in any segment is considered as a possibility of EM-induced damage, which causes failure of the whole chip. Common practice employed in industry for fixing this problem is to iteratively widen metal lines that are close to a location of void nucleation or voltage drop violation. However, this trial-and-error approach might iterate forever as it "blindly" tries to fix the grid and can lead to overdesign. A growing understanding that the existing constraints are too conservative and cannot describe properly the essential features of EM in the grid was developed in EDA community recently. In order to address this concern, a novel physics-based methodology of p/g EM assessment and fixing the induced voltage violations was developed [1]. Employment of the voltage degradation measurements performed on real silicon for validation and calibration of this methodology is described in this paper.

The important characteristic of the grid is the number of redundant paths for voltage delivery to the underneath circuits (cells). Despite of the total increase in the grid resistance caused by EM failure of some wires or vias, the redundancy ensures that a required voltage still can be delivered to the circuits. Thus, the proposed EM assessment methodology is based on analysis of IR drop evolution in the interconnect [2]. The grid TTF is defined as an instance in time when voltage drop degradation caused by resistance increase of several voided interconnect segments is reached a specified threshold. To be able to predict the grid mean-time-to-failure (MTTF), the correct physics-based simulation of metal voiding should be performed, with the accounted stochasticity of EM processes.

Another essential drawback of the rule-based approach is that it cannot correctly describe EM processes in the connected metal line structures, which are referred as interconnect trees (ITs). Current-driven atoms can freely migrate through different segments (branches) of the IT. Diffusion barriers represented by Ta/TaN liners block the atomic flux at the terminal nodes and prevent atom exchange between different layers of metallization. The flux divergence results in hydrostatic stress generation in the encapsulated metal. Physics-based simulations, based on the analysis of Korhonen's equation [3] for EM-induced evolution of hydrostatic stress in the tree, allows to get the stress distribution for any configuration of electric currents in the branches, and to detect the locations where the developed tensile stress transforms the existing micro-defects into growing voids.

A detailed simulation of kinetics of void shape and size evolution, which is crucial for the correct prediction of the resistance change of the voided structures, can be performed only on small interconnect structures. Therefore, the proposed approach for grid analysis was based on linking the numerical integration of Korhonen's equation with compact analytical models for voiding-induced resistance changes [4]. The compact models, validated by Finite Element Analysis (FEA) simulations, captured the behavior of void growth and drift in different via-metal structures [5].

Also, an important advantage of the physics-based simulations over the rule-base analysis is the possibility of proper accounting the temperature variations across the power grid. Linking the EM simulations with thermal analysis of the studied chip is very important, due to the exponential dependency of the TTF on temperature caused by thermal activation mechanism of atomic diffusion. Non-uniform temperature distribution affects the stress distributions in ITs and can cause voiding in the locations of large thermal gradients, where the essential divergence of atomic flux is developed [5].

Due to the complexity of the EM degradation of power grids, a careful experimental validation of the assessment methodology is required. A grid-like multi branch test structure studied in [6] has been used for validation of voiding models and calibration of model parameters. This grid, fabricated with a 65 nm technology, consists of two metal layers running in orthogonal directions and connected by vias in each intersection. Such grid design provides many redundant paths for current flow between cathode terminals located in two opposite corners of the grid and the anode terminal located in the grid center. Voltage tapping technique applied to all of 162 nodes of this grid allowed to deduce voiding kinetics from the measured nodal voltage evolution. Implemented on-chip poly-heaters generated either uniform or non-uniform temperature distributions for analysis of effects of temperature gradients on the rate of voltage degradation.

More relevant to real chip validation of the proposed EM assessment methodology should be done on a large grid fabricated with standard routing techniques, which can reveal the realistic current and voltage redistribution and gradual grid degradation due to cumulative effect of multiple voided wires and vias. Toward this target, a custom test-grid was designed with 28 nm CMOS technology. In order to cope with unavoidable transistor leakage happening at elevated temperatures of and above 350 ^{0}C, which is needed for conducting an accelerated EM testing, the standard cells were replaced by high-resistance poly-resistors. The comparison of measured and simulated behaviors of EM-induced voltage evolution in this test grid is presented in this paper.

2 EM ASSESSMENT METHODOLOGY

The EM analysis flow, which was developed for EM MTTF estimation, is shown in Fig.1. Here, a parasitic resistance extraction tool is applied to generate a resistor netlist of power and ground nets. The ports where p/g nets are connected to the cells are considered as constant current sources (I_s), with values defined by the cell power. Power analysis is performed for extracting initial voltages in all nodes of the fresh grid. The aim of the presented analysis is do detect the instance in time when resistance increase of the grid, caused by EM voiding of some segments, results in a critical increase of voltage drop, so that the required voltage can't be further delivered to the devices.

For obtaining correct temperature distribution in the grid, a thermal analysis of the studied chip is performed, using the heat dissipation map generated by power integrity tool. This map includes self-heating of the grid, as well as heat generation by the switching transistors and self-heating of signal lines. Then, the generated resistors netlist and node voltages, as well as average temperature for each resistor, are used for the EM assessment according to the flowchart of Fig.1, as it is described below in more details.

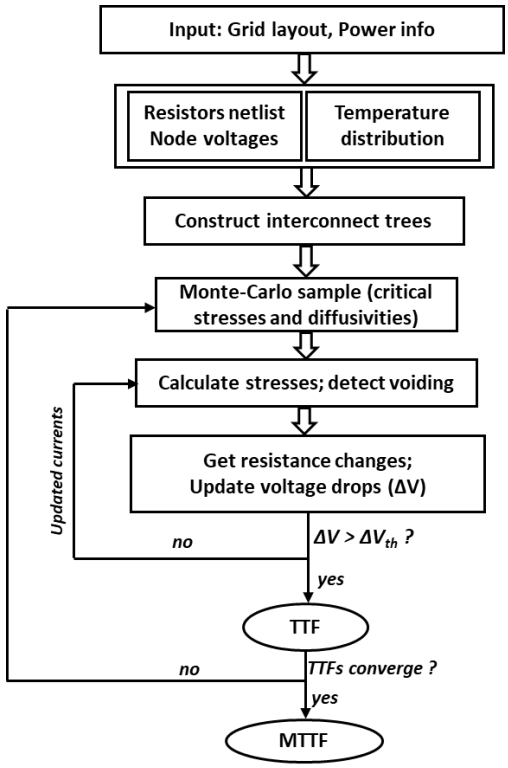

Figure 1: Schematics of EM assessment flow

2.1 IT construction and creation of the Monte-Carlo (MC) samples

Continuously connected metal segments in interconnect represent an IT, which is considered as an "elemental unit" for EM analysis. In dual-damascene technology, the tree consists of wires and underneath vias, since EM-induced atomic flux flow within one tree is blocked by the diffusion barrier at the via bottom. However, due to small lengths of vias, only metal layer segments (referred as "branches" of ITs) are usually considered for simulation of the matter re-distribution, while vias are considered as "junctions" in the trees, which are responsible for voltage/current supply. Formally, the IT is described as a directed graph, with edges corresponding to the branches, and vertices corresponding to the junctions. Reference directions of the graph are required for prescribing electric current direction in branches, as well as for determining inflow and outflow of atomic flux in each junction [2]. A common rail in a power grid is described by IT with just one or two branches connected to each junction (Fig.2a). The trees in the lowest metal layer can have more complicated structure, where junctions connected to 3 or 4 branches can appear due to existence of the segments linking the rail to the cell ports (Fig.2b).

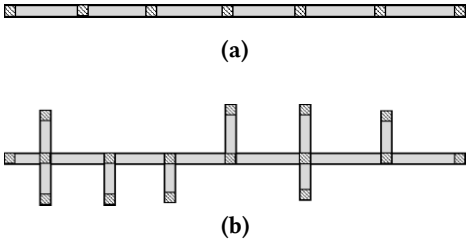

Figure 2: Examples of ITs: branches - gray rectangles; junctions – dashed squares

Using the extracted resistor netlist, the whole power grid is represented by a set of ITs. Known node voltages and the assigned reference directions of the branches allow to calculate electric currents and current directions for each branch. Also, the temperature T of each branch can be obtained using the distribution extracted from the thermal simulation. This temperature is used for assigning atomic diffusivity for the branch as $D_a=D_0 exp(-Q/k_BT)$, where Q is the activation energy, and k_B is the Boltzmann's constant.

Due to the polycrystal morphology of interconnect metals, the grain boundaries (GB) and interfaces represent the main venues of atom migration. Since the effective activation energy Q depends on the metal microstructure as well as on adhesion strength of copper interfaces with liner and capping dielectric, the diffusivity is considered as a random variable across the grid. This is one of the main reasons of stochasticity of EM processes. The diffusion activation energy is described by the normal distribution, with the following probability density function (PDF)

$$f(Q)=\frac{1}{\bar{\sigma}\sqrt{2\pi}}\exp\left[-\frac{1}{2}\left(\frac{Q-\bar{Q}}{\bar{\sigma}}\right)^2\right] \quad (1)$$

Mean value $\bar{Q}$ and standard deviation $\bar{\sigma}$ must be defined based on experimental data, as it is discussed in Sections 3 and 4.

The critical stress required for void nucleation is another random parameter in the EM model. According to the accepted models [7], void formation from a pre-existing micro-defect exposed to a critical hydrostatic tensile stress is possible, if the resulting stress energy decrease compensates the energy increase caused by creation of void surfaces. Therefore, the critical stress value is reverse proportional to the defect size. Randomly distributed defect sizes define the distribution function of critical stress. It is assumed that this distribution should be non-symmetric, because existence of a large defect is less probable. In this work, we use the lognormal distribution of critical stress (similar results can be obtained with the Weibull distribution [6]):

$$f(\sigma_{crit})=\frac{1}{\sigma_{crit}\eta\sqrt{2\pi}}\exp\left[-\frac{1}{2}\left(\frac{\ln(\sigma_{crit})-\mu}{\eta}\right)^2\right] \quad (2)$$

Thus, one MC sample is generated by populating all branches and junctions of the constructed interconnect trees with random values of diffusion activation energy and critical stress according to (1) and (2). Obtaining the EM TTF for this particular sample is based on physical model of EM-induced voiding.

2.2 EM Modeling and Assessment of IR-Drop Degradation

2.2.1 Stress evolution in ITs. EM model involves two main driving forces for atom migration: momentum exchange with electrons and hydrostatic stress gradient. Atomic flux is described by the following equation

$$\Gamma = \frac{D_a}{\Omega k_B T}\left(\Omega\frac{\partial\sigma}{\partial x} - q^*\rho j\right) \tag{3}$$

Here, q^* is the effective charge of migrating atoms, Ω is the atomic volume, ρ is the metal resistivity, j is the current density, and σ is the hydrostatic stress.

A divergence of the flux (3) results in local change of atoms concentration and, as sequence, a volumetric strain, which ultimately creates stress in the metal due to interaction with rigid confinement. In one-dimensional approximation, Korhonen's model [2] can be used, and the stress evolution along the metal line can be described by the following partial differential equation (PDE):

$$\frac{\partial\sigma}{\partial t} = \frac{\partial\sigma}{\partial x}\kappa\left(\frac{q^*\rho j}{\Omega} - \frac{\partial\sigma}{\partial x}\right) \tag{4}$$

where the notation $\kappa = D_a B\Omega / k_B T$ is used; B is the effective bulk modulus describing mechanical properties of the structure. In the case of a single wire of length L, the equation (4) is solved using the zero flux conditions in two edges $\Gamma(x=0)=\Gamma(x=L)=0$, which yields in the following expression for stress gradients at blocking boundaries:

$$\left.\frac{\partial\sigma_{ik}}{\partial x}\right|_{\substack{x=0\\x=L}} = \frac{q^*\rho j_{ik}}{\Omega} \tag{5}$$

An extension of Korhonen's model for simulation of stress evolution in a tree had been developed [1]. In this case, the model must consider continuity of atomic flux in internal junctions of the tree. With account of (3), the boundary condition for the i-th junction takes the form

$$\sum_k w_{ik}\kappa_{ik}\left(\left.\frac{\partial\sigma_{ik}}{\partial x}\right|_{x=x_i} - \frac{q^*\rho j_{ik}}{\Omega}\right) = 0 \tag{6}$$

where the indices (ik) denote k-th branch connected to i-th junction; w_{ik} is the width of k-th branch.

Numerical integration of PDE (4) can be performed using the finite difference method, by assigning the stress derivatives to each junction through (6). Backward differentiation formula is used to calculate the time derivative, so the stress evolution $\sigma(t)$ at each discretization point can be obtained with an adaptive time step Δt. If the tensile stress in any junction achieves the critical stress value, which was randomly prescribed to this point, a void nucleation in this location is considered. The continuity equation (6) is no more valid for the voided junction because an outflow of atoms from the emerged free surface of the void into the metal bulk makes the branches connected to the voided junction mutually independent. Immediately after the void formation, the atomic flux near the void surface ($x=x_s$) is caused mainly by the appeared stress gradient. This gradient can be approximated by introducing an effective thickness of the void interfacial layer δ [8]:

$$\left.\frac{\partial\sigma(t)}{\partial x}\right|_{x=x_s} = \frac{\sigma(t)}{\delta} \tag{7}$$

Solving PDE (4) with boundary condition (7) in voided nodes should be accompanied by simulation of void growth and corresponding change of metal resistance.

2.2.2 Simulation of voiding kinetics. In the one-dimensional case under consideration, a void in any junction spans the entire wire cross-section, and its evolution kinetics can be derived by calculating atomic fluxes from each void to the metal bulk. This results in the rate of void surface propagation in any voided branch of the tree

$$v = \Omega\Gamma(x_s) = \frac{D_a\Omega}{k_B T}\left(\left.\frac{\partial\sigma}{\partial x}\right|_{x=x_s} - \frac{q^*\rho}{\Omega}j\right) \tag{8}$$

where the stress derivative near the void surface can be calculated with the finite-difference approach.

2.2.3 Voiding-induced resistance changes and re-calculation of node voltages in the grid. In real interconnects the voiding effect is determined by the impacted electric connectivity of via-metal structures. Though vias are not included in IT structure in the employed model, a possible failure of a via connection in the voided junction must be considered for electric current redistribution analysis. Two via types must be analyzed, corresponding to the electrons flow direction: upstream and downstream.

In the case of downstream via (Fig.3a), a tensile stress generated underneath the via due to depletion of atoms, creates a void in the lower metal layer. Even a slit-like void with small volume, which can be formed immediately after the nucleation, can undercut the via. For this reason, voiding under downstream vias is the main cause of early failure of the grid. In simulations, this voiding event is described by putting the conductance of the undercut via equal to zero: $G_{Via}=0$.

For the structures with upstream via (Fig.3b), large tensile stress is generated inside the via and in the above metal region. Usually, void nuclei appear at the top interface of the copper with capping

dielectric (the dashed semi-circle in figure). The growth rate of this void can be described by (8) applied to each branch connected to the voided junction. A contribution of each branch in the total void growth is calculated by summation of the increment in void length during each time step, $\Delta l_v = v\Delta t$.

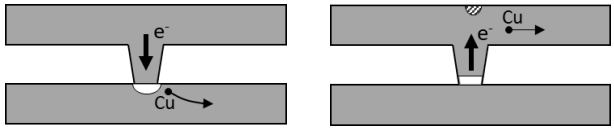

Figure 3: Voiding in via-metal structures: (a) downstream via, and (b) upstream via

The growth is usually accompanied by the void drift in the direction opposite to the electrons flow direction. The latest process is caused by EM-induced migration of atoms along the void surface. This drift results in a propagation of void toward the via bottom, as it was demonstrated in experiments [9] and in FEA simulations [5, 10]. Therefore, an increase in via resistance due to presence of the void with calculated length l_v^{Via} is considered in simulations. Since the electric current in voided via flows through the liners, the resistance change depends on the radius r_{via}, liner resistivity ρ_{liner} and its thickness h_{liner} as

$$\Delta R^{Via}(t) = \frac{\rho_{liner}}{2r_{via}h_{liner} - h_{liner}^2} l_v^{Via} \tag{9}$$

In this case, the conductance evolution of the via is calculated: $G(t)=[R_0+\Delta R(t)]^{-1}$. More accurate modeling requires introduction of a tuning parameter θ, which defines a part of void volume propagated into the via as $l_v^{Via} = \theta l_v$. In this case the resistance growth of the voided branch is

$$\Delta R(t) = \left(\frac{\rho_{liner}}{S_{liner}} - \frac{\rho_{Cu}}{S_{Cu}}\right)(1-\theta) l_v(t) \tag{10}$$

where S_{liner} and S_{Cu} are cross-sectional areas of the liner and Cu wire.

Resistance increase of any grid segment results in overall voltage increase. The initial node voltages U_0 and current densities in the grid are obtained in the standard way, by solving the matrix equation $\mathbf{G_0}\times\mathbf{U_0}=\mathbf{I_s}$, where the matrix $\mathbf{G_0}$ is composed using initial conductance of all metal and via, $\mathbf{I_s}$ is the vector of constant current sources. In the employed assessment methodology, the conductance matrix is updated periodically with a time step T_{step}, using the calculated conductance change of all voided segments. Correspondingly, new voltages at n-th step, $U(n\cdot T_{step})$, should be obtained from the equation $(\mathbf{G}+\Delta\mathbf{G})\times\mathbf{U}=\mathbf{I_s}$ Assuming that $\Delta\mathbf{G}<<\mathbf{G}$, the node voltages can be efficiently updated using the voltage matrix at the previous step [11]. The effect of all voided resistors ultimately causes voltage decrease below a threshold value in a node of power net connected to a circuit port. The corresponding time is considered as TTF. In a similar way, voltage increase above the threshold is considered as failure of ground net.

3 MODEL CALIBRATION: GRID-LIKE TEST STRUCTURE WITH NON-UNIFORM TEMPERATURE DISTRIBUTION

The experimental structure described in [6], was fabricated with a 65 nm technology and consisted of two metal layers, M3 and M4 with orthogonal routing directions (Fig.4a). Each layer contains 9 rails representing ITs (similar to the tree of Fig.2a), with 8 branches and 9 junctions. All the junctions in M3 and M4 layers are connected by V3. The sizes of branches in each layer are: L=20 um, w=0.1 um, and the via diameter is 0.1um. Thicknesses of all metal and via layers are 0.2 um.

The grid was heated for EM experiments by means of 3 poly-heaters, Fig.4b, which can provide very fast temperature control due to their location immediately under the interconnect layers. Also, this structure enabled creation of non-uniform temperature distribution in the grid by changing the feeding currents of the heaters.

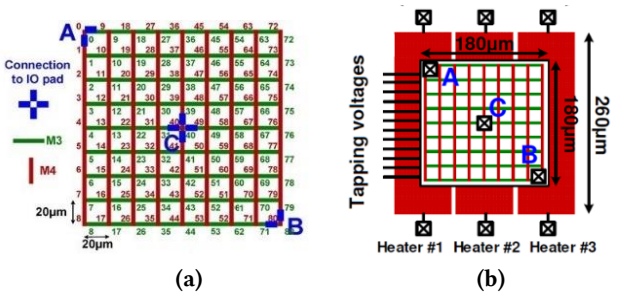

Figure 4: EM test structure, (a); test grid with poly-heaters, (b)

A 3-terminal voltage supply scheme was applied to the grid, with grounded cathode C in the center and two anode ports A and B in the opposite corners. Each of the anodes was source of 5 mA constant current, which provided initial voltage drop of 0.3 V between anode and cathode. Such connection created a symmetrical initial current distribution in upper-left and lower-right sectors of the grid (Fig.5a). Due to high current densities, up to $4\cdot10^{10}$ A/m^2, first voids were generated within several minutes, which forced the current to redistribute through the numerous redundant paths existing in this grid.

Voltage tapping method was used in the experiment for tracking voltage evolution in the grid nodes, caused by EM voiding of vias and wires. From the measurements of voltage evolution in each grid node the locations and growth kinetics of the voids were derived. For study of EM failure statistics, the measurements were performed on 42 identical samples.

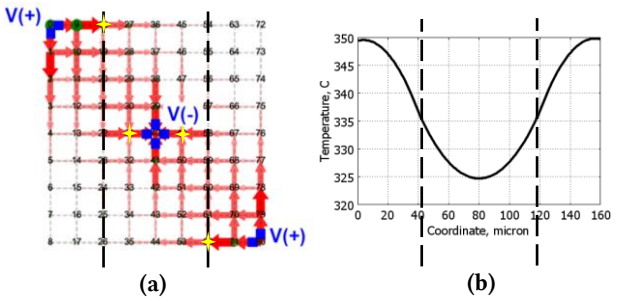

Figure 5: Current distribution in the grid (as depicted by arrows), (a); non-uniform temperature distribution along the horizontal rails, (b). Dashed lines show borders of poly-heaters. Four possible early voiding locations are shown in (a).

The EM assessment methodology has been applied to the test grid for calibration of the voiding model parameters and for validation of the approach. As EM voiding of different segments of the grid causes voltage growth in different nodes (as well as between anodes and cathode), the grid was considered as a ground net in simulations. Comparing the simulated voltage evolution with measurements enabled the model calibration and validation. This procedure was described in detail in previous works [4, 5].

The calibrated model allows to find the kinetics of the voltage drop evolution between anodes and cathode, ΔU(A-C) and ΔU(B-C) (Fig.6), which is caused by resistance increase of all voided segments. The good fit between simulated and measured kinetics of voltage drop between both anodes and cathodes proves the ability of the developed methodology to predict EM TTF of power grids. For quantitative statistical analysis, the criterion of grid failure ΔU(anode-cathode)>0.4V was accepted: the time, when this voltage drop threshold was reached, represents TTF of the grid.

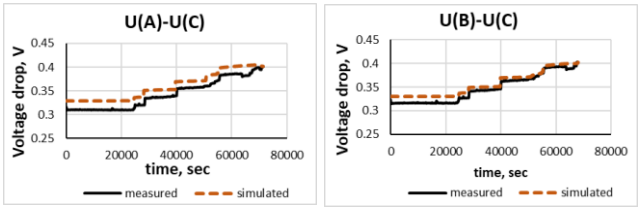

Figure 6: Anode-cathode voltage drop kinetics due to EM voids in the grid

The model parameters were calibrated with measurements performed in the case of uniform temperature of 350 °C across the grid. For diffusivity, the mean activation energy $\bar{Q} = 1.48 \cdot 10^{-19} J$, the standard deviation $\bar{\sigma} = 8 \cdot 10^{-22} J$ and pre-exponential factor $D_0 = 5 \cdot 10^{-11} m^2/s$ were obtained. For PDF (2) of critical stress, the parameters μ =19.5 and η=0.2 were used, in order to have the mean value of critical stress of 300 MPa and the standard deviation of 60 MPa. Note that in this case of uniform T, the first voids were detected in the junctions near the cathode (Fig.5a), where the largest tensile stress was developed. The same calibrated parameters were used for EM simulation in the case of non-uniform temperature distribution of Fig.5b, which was created in experiment by switching off the central heater. In this case the first voids were found in the junctions near two anodes, which are shown in Fig.5a. In these junctions the stress growth due to the existing current divergency is exacerbated by the additional atomic flux divergency caused by the gradient of temperature-dependent diffusivity. Thus, the voiding sequence in the grid is changed, which obviously impacts TTF of the grid.

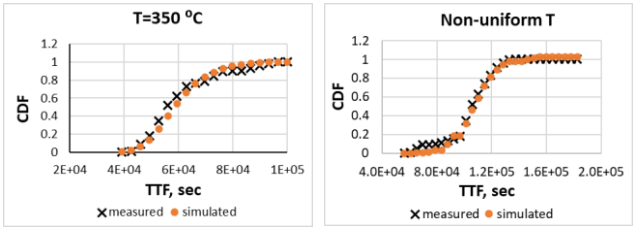

Figure 7: Measured and simulated statistics of EM TTF in the case of uniform and non-uniform temperature in the grid

The obtained good fit of simulated and measured cumulative distribution function (CDF) is shown in Fig.7. MTTF of $6 \cdot 10^4$ sec, obtained in the case of uniform T, has increased to 10^5 sec in the case of decreased temperature or the grid in the region under the central heater. These results prove that the temperature impact is properly captured in the physical model.

4 EXPERIMENTAL VALIDATION OF EM ASSESSMENT METHODOLOGY FOR POWER/GROUND ON-CHIP GRID

As mentioned in the Introduction, a use of a common chip for accelerated EM testing is not feasible, due to inability of transistors to operate at test temperatures above 300 °C. Therefore, a special test design was developed (using a 28 nm technology) for validation of the simulation methodology, where the operational cells were replaced by quasi-cells containing high-resistance meandering poly-resistors. Sets of quasi-cells with different sizes of meanders were used, which created a complicated distribution of electric current in the grid. Overall, 3229 quasi-cells were included in the studied Design-Under-Test (DUT).

A piece of the grid layout is shown in Fig.8a. The grid contains metal layers M1-M4, with vertical connection scheme shown in Fig.8b. The alternate power (VDD) and ground (VSS) M2 rails provide connections to the cells through M1 pads. The connectivity to VDD/VSS external ports through M3 and M4 rails provides high redundancy for voltage supply to the quasi-cells. EM stressing was realized by loading VDD net with 100 mA constant current. The widths of rails in layers M1-M4 were 200 nm, and thicknesses – 100 nm. From the electric circuit simulations, the maximal current density of $2 \cdot 10^{11}$ A/m^2 was

obtained in M4 layer. Metal layer M5 was used for the grid temperature control. The heater temperature of 400 °C created 350 °C in M2 layer, due to intensive heat removal from the silicon substrate.

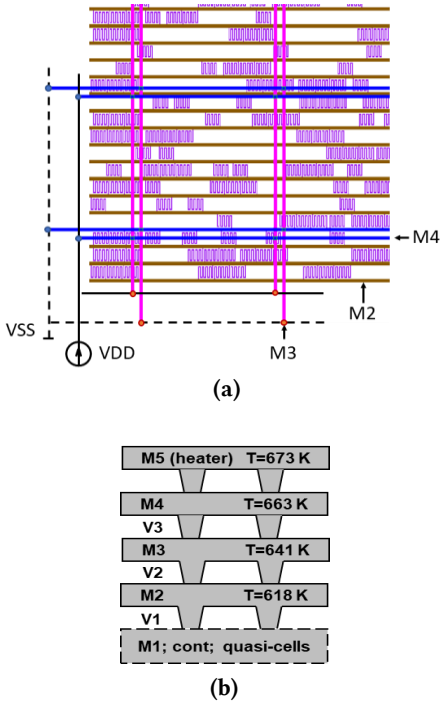

Figure 8: Layout of the test grid, (a); schematics of the metal layers stack, (b).

For EM assessment, the established vertical gradient of temperature was simulated and temperatures in metal layers were extracted (Fig.8b). M1 pads connecting the quasi-cells to the grid were immortal during EM processes due to short length effect and therefore they are not considered in further analysis. In layers M2-M4, EM caused quick degradation of connectivity in numerous junctions, followed by current re-distribution and gradual voltage increase.

Voltage tapping was applied to some selected VDD and VSS nodes, for studying the behavior of voltage evolution in these nets. Also, voltage evolution on VDD external (current supply) port was monitored, which indicated the total increase of the grid resistance due to EM-induced voiding.

For validation of the EM assessment methodology, the flow of Fig.1 was applied to this test grid. Comparison of voltage evolution tendencies with the experiment allowed to deduce the voiding locations and sequence. The diffusivity activation energy and pre-factor, and mean value of critical stress were obtained from calibration: $\bar{Q} = 1.4 \cdot 10^{-19} J$, $D_0 = 5 \cdot 10^{-11} m^2/s$, $\sigma_{crit} = 160\,\text{MPa}$. These parameters allowed to obtain good fit of simulated behavior of voltage increase on VDD port with experiment for a set of 8 samples (Fig.9). The data spread due to EM stochasticity was described by the values of standard deviations: $8 \cdot 10^{-22} J$ for diffusivity and 50 MPa for critical stress. For lognormal PDE (2), the parameters μ =18.88 and η=0.2 were used.

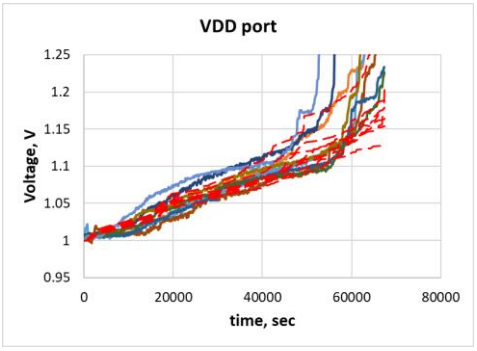

Figure 9: Figure 9: Comparison of simulated voltage evolution (dashed lines) with measured data (bold lines) on VDD port

Analysis of simulation results revealed several representative intervals during EM degradation of the grid (Fig.10). In the initial time interval, corresponding to interval "I", degradation of upstream vias V3 was observed, due to void nucleation in M4. Also voids in M3 were appearing, undercutting downstream V3 vias, and significantly contributing to voltage increase in this interval. In the time interval "II", many voids appeared in M2 undercutting downstream V2 vias, which caused more abrupt voltage increase. In the intervals "III" and "IV" a lot of failures of V3 and V2 were observed, with prevailing number of undercut V2 vias in "IV". The number of via failures for one MC sample is summarized in Table1.

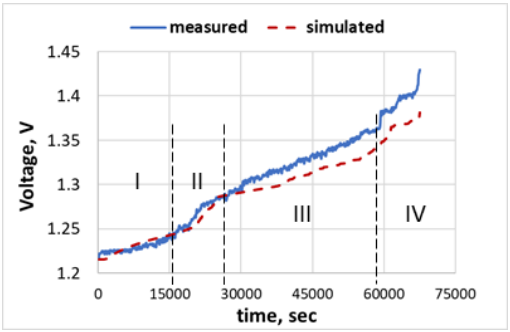

Figure 10: Behavior of voltage evolution for one sample

Via type	Number of voids
V3: M3-M4 upstream vias	86
V3: M4-M3 downstream vias	29
V2: M2-M3 upstream vias	67
V2: M3-M2 downstream vias	136

Table 1. Representative voiding statistics for one sample

As it follows, the largest number of voids is observed in M2 rails under M3-M2 downstream vias, despite of larger current density in layers M3 and M4. Undercutting vias V2 by voids has a crucial impact on the grid degradation, since it results in partial disconnection of the M2 rails and the quasi-cells from the M3/M4 layers.

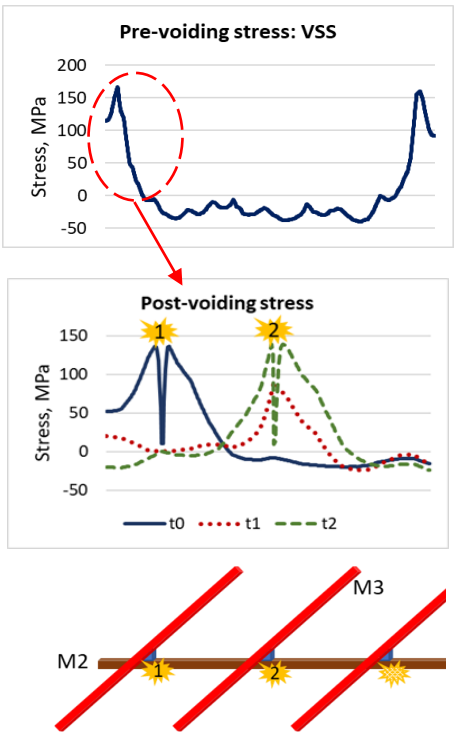

Figure 11: Pre-voiding stress, voiding sequence, and post-voiding stress evolution in M2 layer VSS rail

Analysis of EM stress evolution demonstrates how numerous voids are created in M2. The pre-voiding stress distribution along IT, corresponding to M2 rail in VSS net, is shown in Fig.11. The electrical connection scheme provides the current flow from each edge of M2 rail to the center, so that large tensile stresses are generated at both edges of the studied tree and can cause void nucleation. The subsequent post-voiding stress evolution at the left edge of the M2 rail is demonstrated in the figure. Void nucleation and growth under the first via (at time t=t0) is accompanied by local stress relaxation in M2, and also disconnects V2 via and causes current re-distribution. The resulting current growth through the next via increases the local stress (demonstrated by the plot corresponding to t=t1) and creates the second void (t=t2). As a result, up to 3 voids were observed in simulations near each (left/right) edge of the rail. For the existing 41 M2 rails, ~130 failures of M3-M2 downstream vias were obtained.

A similar analysis demonstrated sequential void nucleation in VDD rails in M3 layer, which caused degradation of M2-M3 upstream vias. Thus, EM failure of VSS net is caused mainly by undercutting the downstream vias, which result in abrupt voltage changes, while more gradual voltage increase in VDD nodes displays degradation of VDD net due to voiding in upstream vias. The predicted difference in degradation behaviors of these two nets was confirmed by the measurements, Fig.12, which also validates the simulation methodology.

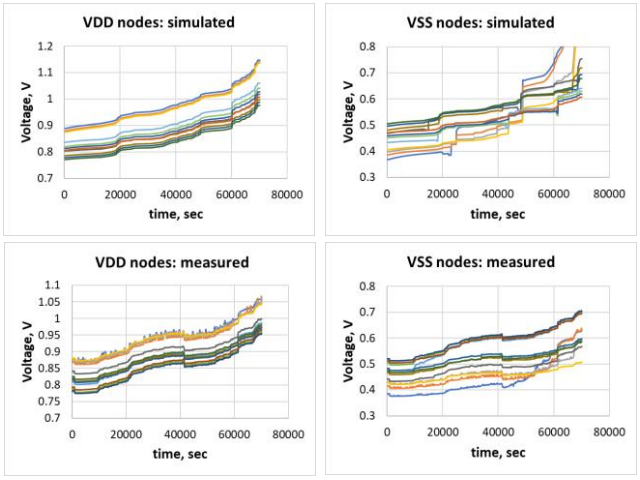

Figure 12: Simulated and measured voltage evolution in VDD and VSS nets for selected nodes

By defining the grid failure as 10% voltage increase on VDD port, TTF distribution was extracted from MC simulations, and compared with the results for 15 measured samples (Fig.12). The obtained MTTF and standard deviations are in good agreement, as summarized in Table2.

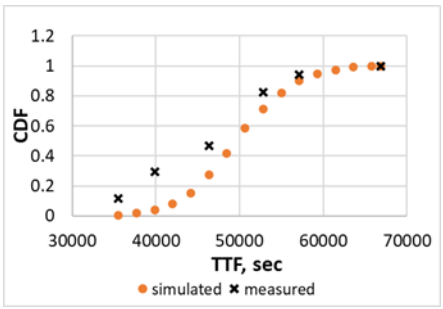

Figure 13: Experimental and simulated cumulative distribution function of TTF

	measured	simulated
MTTF	50418 sec	50368 sec
Stddev of TTF	9410 sec	5670 sec

Table2. Measured and simulated characteristics of TTF distribution

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